

## TC74LVQ74F/FN/FS

### QUAD D - Type Flip Flop With Preset and Clear

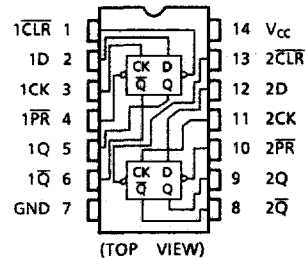
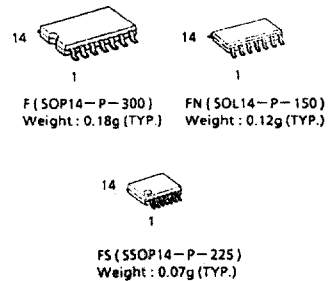
The TC74LVQ74 is a high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{\text{CLR}}$  and  $\overline{\text{PR}}$  are independent of the CK and are accomplished by setting the appropriate input to an "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

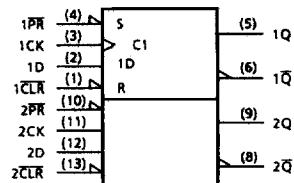
- High Speed:  $f_{\text{MAX}} = 147\text{MHz}$  (Typ.) at  $V_{\text{CC}} = 3.3\text{V}$
- Low Power Dissipation:  $I_{\text{CC}} = 2.5\mu\text{A}$  (Max.) at  $T_a = 25^\circ\text{C}$
- Input Voltage Level:
  - $V_{\text{IL}} = 0.8\text{V}$  (Max.) at  $V_{\text{CC}} = 3\text{V}$
  - $V_{\text{IH}} = 2.0\text{V}$  (Min.) at  $V_{\text{CC}} = 3\text{V}$
- Symmetrical Output Impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 12\text{mA}$  (Min.)
- Balanced Propagation Delays:  $t_{\text{pLH}} = t_{\text{pHL}}$
- Pin and Function Compatible with 74HC74



Pin Assignment

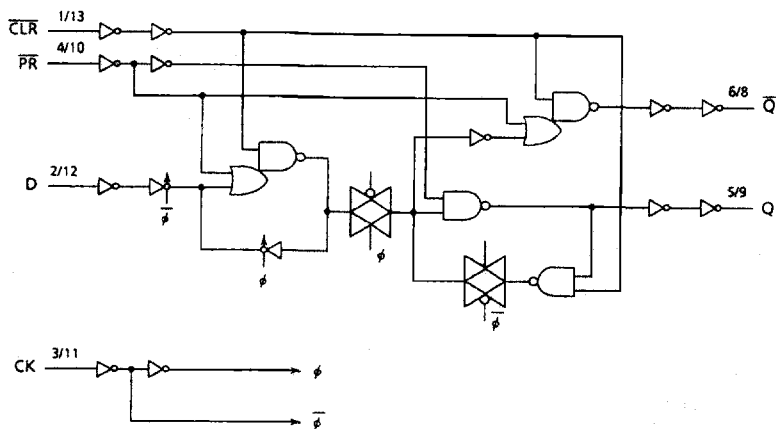
Inputs				Outputs		Function
CLR	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	-
H	H	L	$\int$	L	H	-
H	H	H	$\int$	H	L	-
H	H	X	$\overline{\text{L}}$	Qn	$\overline{\text{Qn}}$	NO CHANGE

X: Don't Care



IEC Logic Symbol

## System Diagram



## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	$V_{CC}$	-0.5 - 7.0	V
DC Input Voltage	$V_{IN}$	-0.5 - $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5 - $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 50$	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 100$	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65 - 150	$^{\circ}C$
Lead Temperature 10sec	$T_L$	300	$^{\circ}C$

## Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	2.0 - 3.6	V
Input Voltage	$V_{IN}$	0 - $V_{CC}$	V
Output Voltage	$V_{OUT}$	0 - $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40 - 85	$^{\circ}C$
Input Rise and Fall Time	$dt/dv$	0 - 100	ns/V

**DC Electrical Characteristics**

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max.	Min.		Max.
High-Level Input Voltage	V <sub>IH</sub>	--		3.0	2.0	--	--	2.0	--	V
Low-Level Input Voltage	V <sub>IL</sub>	--		3.0	--	--	0.8	--	0.8	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50µA	3.0	2.9	3.0	--	2.9	--	
			I <sub>OH</sub> = -12mA	3.0	2.58	--	--	2.48	--	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50µA	3.0	--	0.0	0.1	--	0.1	
			I <sub>OL</sub> = 12mA	3.0	--	--	0.36	--	0.44	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		3.6	--	--	±0.1	--	±1.0	µA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		3.6	--	--	2.5	--	25.0	

**Timing Requirements (Input tr = tr = 3ns)**

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V <sub>CC</sub> (V)	Limit	Limit	Limit	Limit	
Minimum Pulse Width (CK)	t <sub>w(L)</sub> t <sub>w(H)</sub>		2.7	9.0	10.0			
			3.3 ± 0.3	7.0	7.0			
Minimum Pulse Width (CLR, PR)	t <sub>w(L)</sub>		2.7 3.3 ± 0.3	9.0 7.0	10.0 7.0	ns		
Minimum Set-up Time	t <sub>s</sub>		2.7 3.3 ± 0.3	7.5 6.0	8.5 6.0			
Minimum Hold Time	t <sub>h</sub>		2.7 3.3 ± 0.3	1.0 1.0	1.0 1.0			
Minimum Removal Time (CLR, PR)	t <sub>rem</sub>		2.7	6.0	6.0			
			3.3 ± 0.3	4.0	4.0			

**AC Electrical Characteristics (Input  $t_r = t_f = 3ns$ ,  $C_L = 50pF$ ,  $R_L = 500\Omega$ )**

Parameter	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 ~ 85°C		Unit
				Min	Typ.	Max.	Min.	Max.	
Propagation Delay Time (CK - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	-	2.7	-	9.0	19.7	1.0	23.0	ns
			3.3±0.3	-	7.5	14.0	1.0	16.0	
Propagation Delay Time (CLR, PR - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	-	2.7	-	8.4	16.9	1.0	19.0	ns
			3.3±0.3	-	7.0	12.0	1.0	13.5	
Maximum Clock Frequency	$f_{MAX}$	-	2.7 3.3±0.3	55 70	110 130	- -	45 65	- -	MHz
Output to Output Skew	$t_{osLH}$ $t_{osHL}$	(Note 1)	2.7 3.3±0.3	- -	- -	1.5 1.5	- -	1.5 1.5	ns
Input Capacitance	$C_{IN}$	(Note 2)	-	-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}$	(Note 3)	-	-	39	-	-	-	

Note (1) Parameter guaranteed by design.  $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

**Noise Characteristics (Input  $t_r = t_f = 3ns$ ,  $C_L = 50pF$ ,  $R_L = 500\Omega$ )**

Parameter	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub>	Typ.	Max.	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	-	3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	-	3.3	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>	-	3.3	-	2.0	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>	-	3.3	-	0.8	V

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