



3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH16952A

FEATURES:

- Typical $t_{SK(O)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16952A:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

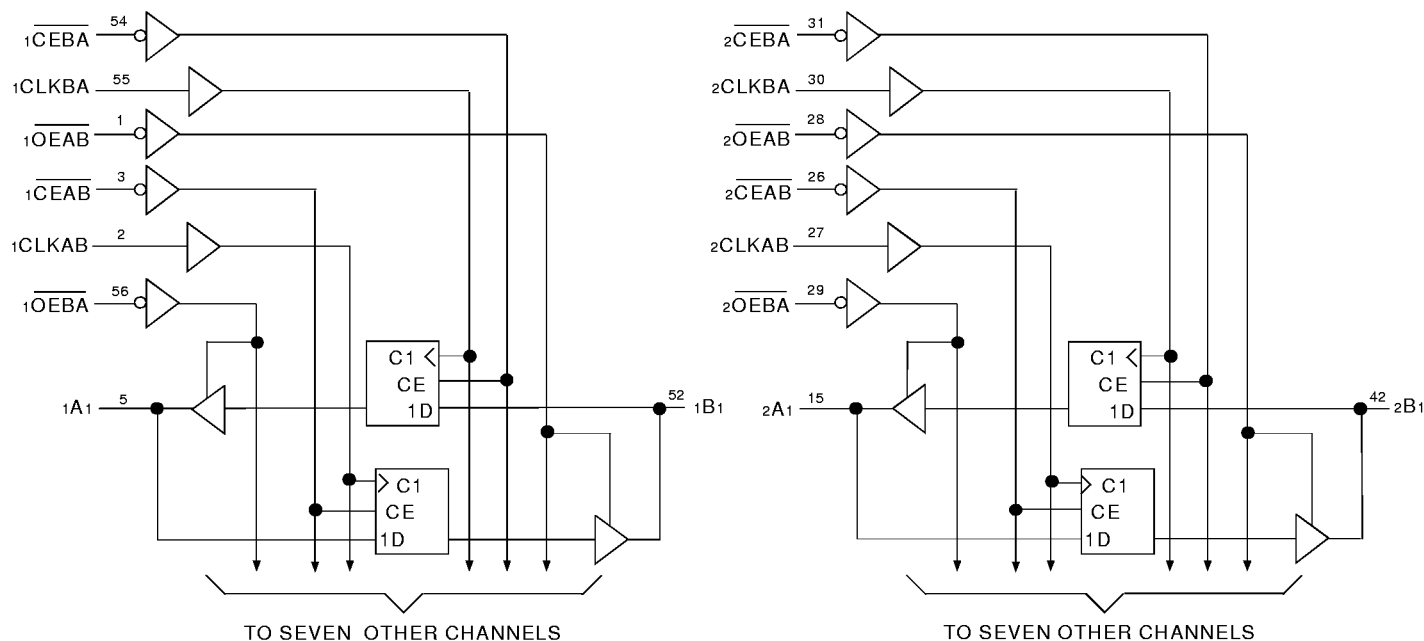
DESCRIPTION

This 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable (\overline{CEAB}) must be LOW to enter data from the A port. CLKAB controls the clocking function. When CLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. \overline{OEAB} performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using \overline{CEBA} , CLKBA, and \overline{OEBA} inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

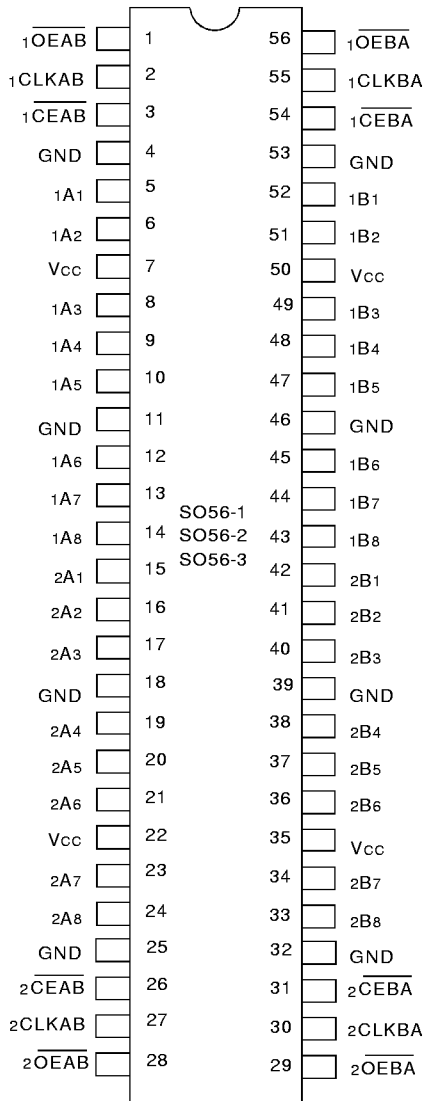
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16952A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
\overline{xOEAB}	A-to-B Output Enable Inputs (Active LOW)
\overline{xOEBA}	B-to-A Output Enable Inputs (Active LOW)
\overline{xCEAB}	A-to-B Clock Enable Inputs (Active LOW)
\overline{xCEBA}	B-to-A Clock Enable Inputs (Active LOW)
xCLKAB	A-to-B Clock Inputs
xCLKBA	B-to-A Clock Inputs
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current	- 50 to +50	mA
IIK	Continuous Clamp Current, Vi < 0 or Vo < 0	- 50	mA
ICC	Continuous Current through each Vcc or GND	±100	mA

LVC Link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COU	Output Capacitance	VOU = 0V	6.5	8	pF
CIO	I/O Port Capacitance	VIN = 0V	6.5	8	pF

LVC Link

NOTE:

- As applicable to the device type.

FUNCTION TABLE (1, 2)

Inputs				Outputs
\overline{xCEAB}	xCLKAB	\overline{xOEAB}	xAx	xBx
H	X	L	X	B ₀
X	L	L	X	B ₀
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
B₀ = Level of B before the indicated steady-state input conditions were established.
- A-to-B data flow is shown; B-to-A data flow is similar but uses \overline{xCEBA} , xCLKBA, and \overline{xOEBA} .

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	VCC = 3.6V	VI = 0 to 5.5V	—	—	±5	µA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = 0 to 5.5V	—	—	±10	µA
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5V		—	—	±50	µA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V	VIN = GND or VCC	—	—	10	µA
			3.6 ≤ VIN ≤ 5.5V ⁽²⁾	—	—	10	
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V other inputs at VCC or GND		—	—	500	µA

LVC Link

NOTES:

1. Typical values are at VCC = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 3.0V	VI = 2.0V	-75	—	—	µA
			VI = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 2.3V	VI = 1.7V	—	—	—	µA
			VI = 0.7V	—	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	VCC = 3.6V	VI = 0 to 3.6V	—	—	±500	µA

LVC Link

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VoH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
V _{CC} = 3.0V	I _{OH} = -24mA	2.2	—			
VoL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

LVC Link

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	C _L = 0pF, f = 10MHz	87	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		43	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	—	7.6	1.6	6.6	ns
t _{PZH} t _{PZL}	Output Enable Time x $\overline{OE}A\overline{B}$, x $\overline{OE}A\overline{B}$ to xAx, xBx	—	8	1.1	6.6	ns
t _{PHZ} t _{PLZ}	Output Disable Time x $\overline{OE}A\overline{B}$, x $\overline{OE}A\overline{B}$ to xAx, xBx	—	7.1	1.9	6.7	ns
t _{SU}	Set-up Time, Data Before xCLKAB \uparrow , xCLKBA \uparrow	3.4	—	2.8	—	ns
t _H	Hold Time, Data After xCLKAB \uparrow , xCLKBA \uparrow	0.5	—	0.5	—	ns
t _{SU}	Set-up Time, x $\overline{CE}A\overline{B}$, x $\overline{CE}B\overline{A}$ Before xCLKAB \uparrow , xCLKBA \uparrow	1.8	—	1.4	—	ns
t _H	Hold Time, x $\overline{CE}A\overline{B}$, x $\overline{CE}B\overline{A}$ After xCLKAB \uparrow , xCLKBA \uparrow	1.1	—	1.9	—	ns
t _w	Pulse Duration, xCLKAB or xCLKBA HIGH or LOW	3.3	—	3.3	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	1	ns

NOTES:

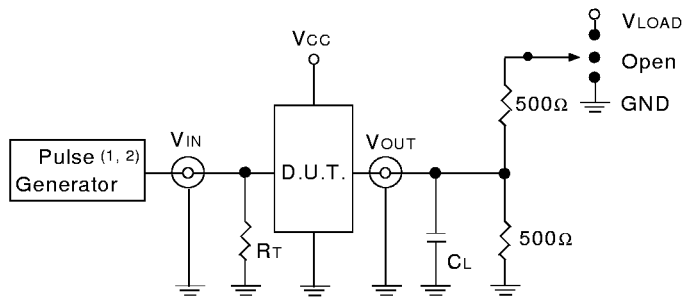
- See test circuits and waveforms. T_A = -40°C to +85°C.
- Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	Vcc(1) = 3.3V ± 0.3V	Vcc(1) = 2.7V	Vcc(2) = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{cc}	V
V _{IH}	2.7	2.7	V _{cc}	V
V _T	1.5	1.5	V _{cc} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

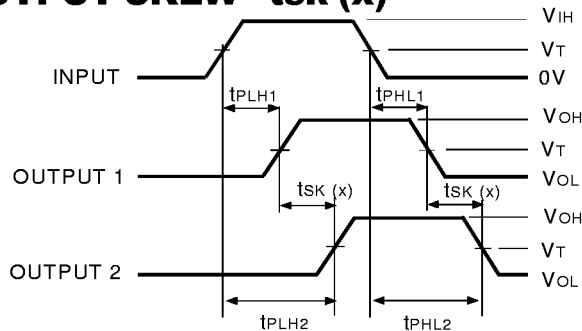
NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain	V _{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

OUTPUT SKEW - t_{SK} (x)

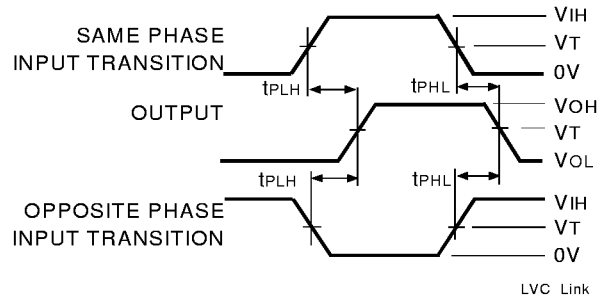


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

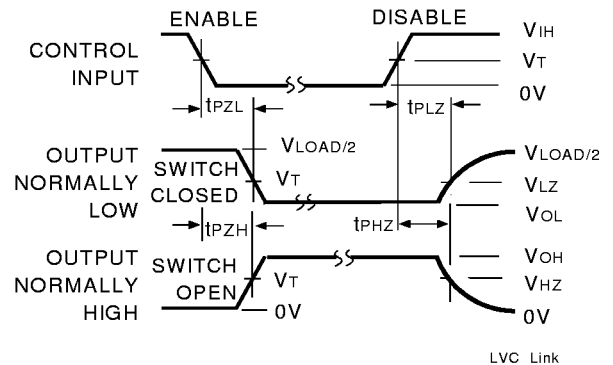
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



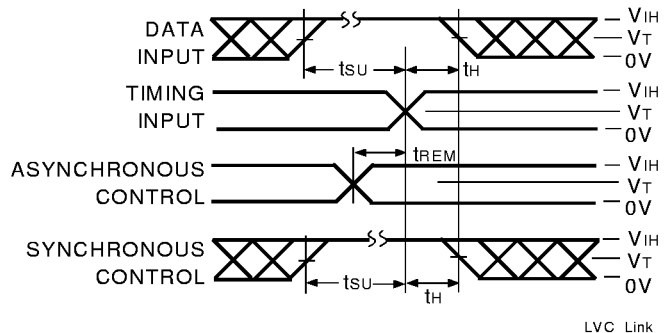
ENABLE AND DISABLE TIMES



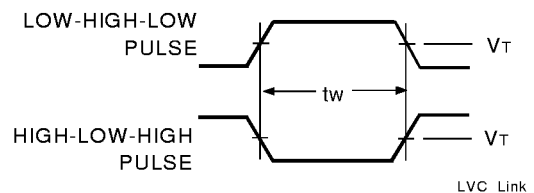
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

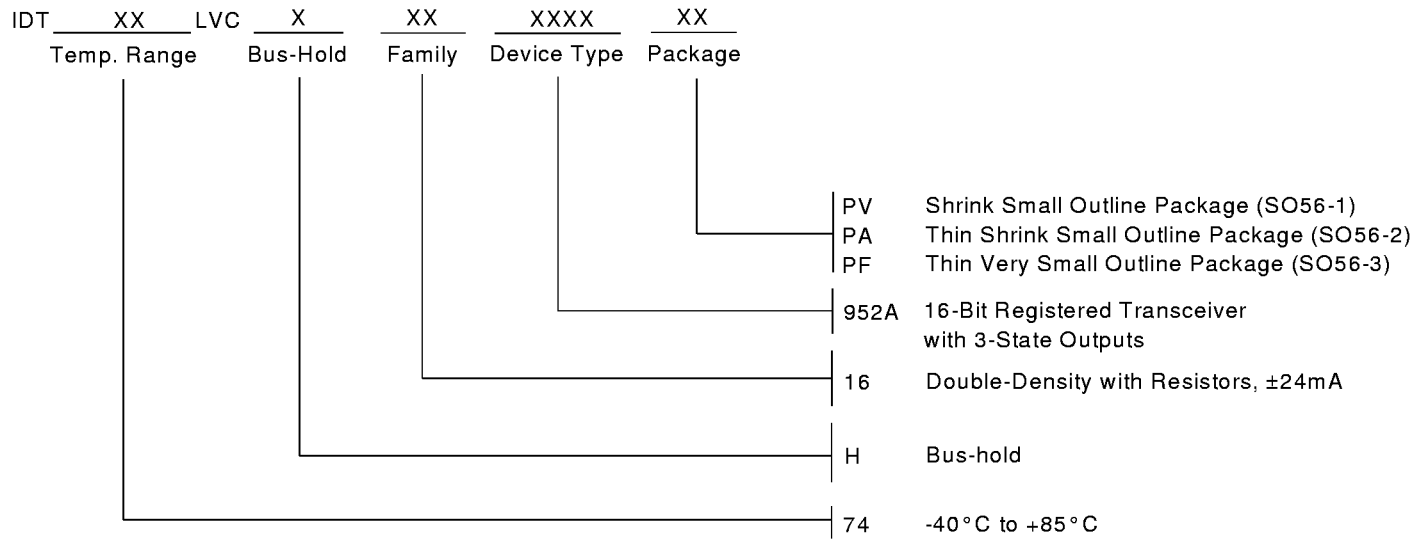
SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



ORDERING INFORMATION



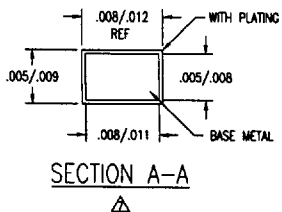
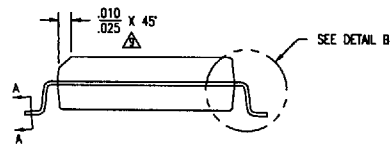
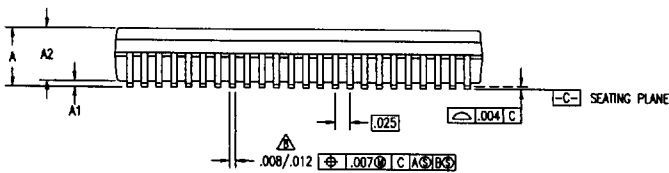
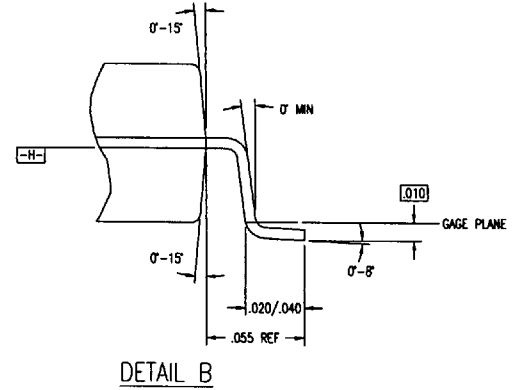
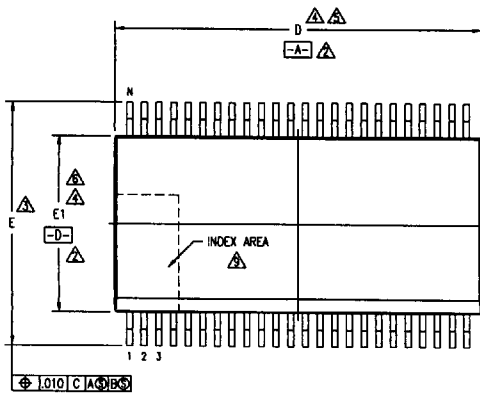
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PACKAGE DIAGRAM OUTLINES
SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 462-8874 TWC: 910-338-2070	
DECIMAL	ANGULAR	TITLE PV PACKAGE OUTLINE	
XXX	±	.300" BODY WIDTH SSOP	
XXXX		.025" PITCH	
XXXXX		APPROVALS	DATE
		DRWN <i>AA</i>	08/15/90
CHECKED		SIZE	DRAWING No.
		C	PSC-4029
		REV	02
DO NOT SCALE DRAWING			

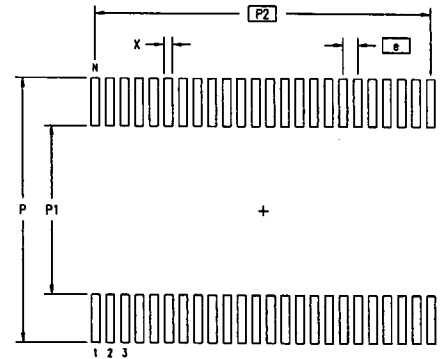
PACKAGE DIAGRAM OUTLINES

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

SYMBOL	DWG # S048-1				DWG # S056-1			
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AA				AB			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

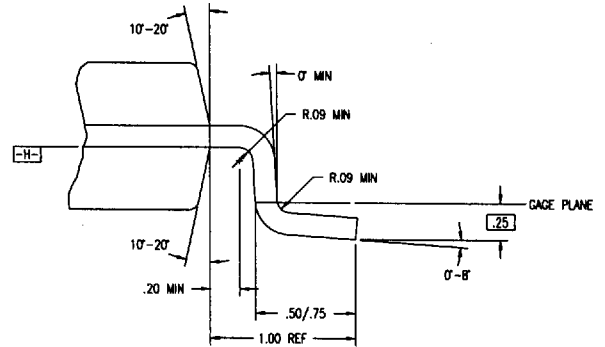
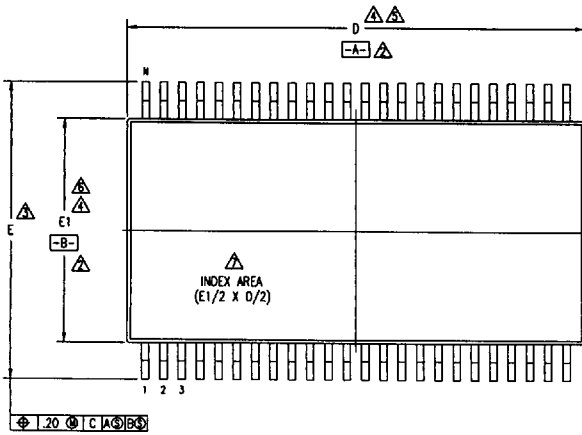
- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stander Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 482-8874 TWC: 810-338-2070	
DECIMAL	ANGULAR		
X.XX	±		
X.XXX	±		
X.XXX	±		
APPROVALS	DATE	TITLE	
DRAWN <i>Ad</i>	08/15/90	PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
CHECKED		SIZE	REV
		C	02
		DRAWING No.	
		PSC-4029	
DO NOT SCALE DRAWING			

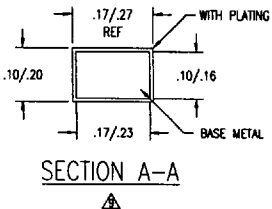
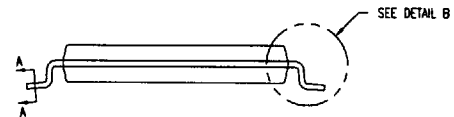
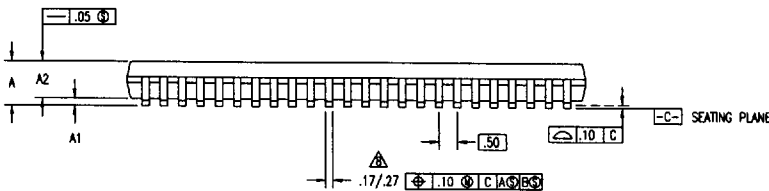
PACKAGE DIAGRAM OUTLINES

TSSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/06/95	



DETAIL B



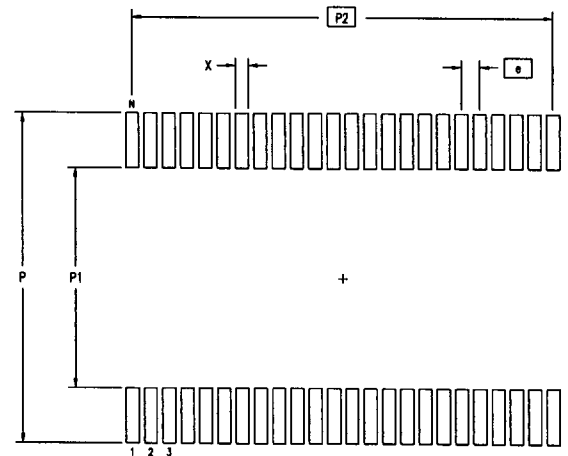
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 492-8674 TWC: 910-338-2070
DECIMAL	ANGULAR	
XXX.X	±	
APPROVALS		TITLE PA PACKAGE OUTLINE
DRAWN	DATE 01/15/93	6.10 mm BODY WIDTH TSSOP
CHECKED		.50 mm PITCH
SIZE C	DRAWING No. PSC-4039	REV 03
DO NOT SCALE DRAWING		

PACKAGE DIAGRAM OUTLINES
TSSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. WU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. WU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

SYMBOL	DWG # S048-2			NOTE	DWG # S056-2			NOTE	
	JEDEC VARIATION				JEDEC VARIATION				
	ED	EE			ED	EE			
MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	1.10		-	-	1.10		
A1	.05	-	.15		.05	-	.15		
A2	.85	1.00	1.05		.85	1.00	1.05		
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5	
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3	
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6	
N	48				56				

LAND PATTERN DIMENSIONS



NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ DATUMS \square -A- AND \square -B- TO BE DETERMINED AT DATUM PLANE \square -H-
- △ DIMENSION E TO BE DETERMINED AT SEATING PLANE \square -C-
- △ DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE \square -H-
- △ DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- △ DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- △ DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- △ LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

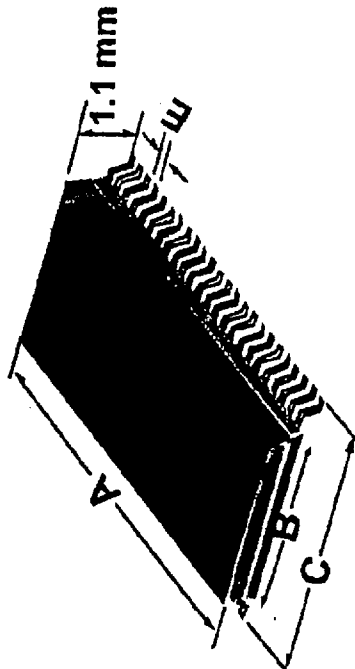
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50	BSC	13.50	BSC
X	.30	.40	.30	.40
e	.50	BSC	.50	BSC
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
±	±	PHONE: (408) 727-8118	
±	±	FAK: (408) 482-8874	TWC: 910-338-2070
±	±		
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE
DRAWN	01/19/93	6.10 mm BODY WIDTH TSSOP	
CHECKED		.50 mm PITCH	
		SIZE	DRAWING No.
		C	PSC-4039
			REV 03
DO NOT SCALE DRAWING			



TVSOP

The Most Compact Double Density Package

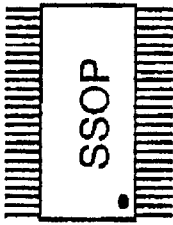


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50

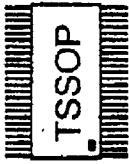


Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

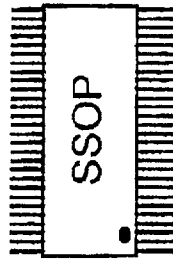


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²



9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0