

# SN54HC375, SN74HC375 4-BIT BISTABLE LATCHES

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

The SN54HC375 and SN74HC375 bistable latches are electrically and functionally identical to the SN54HC75 and SN74HC75, respectively. Only the arrangement of the terminals has been changed in the SN54HC375 and SN74HC375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

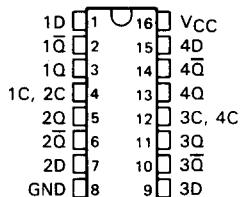
The SN54HC375 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC375 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(EACH LATCH)

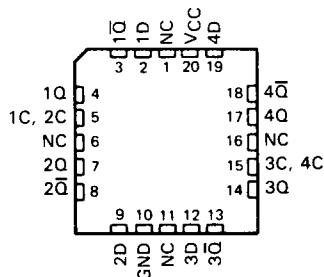
INPUTS		OUTPUTS	
D	C	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	$Q_0$	$\bar{Q}_0$

H = high level, L = low level. X = irrelevant.

SN54HC375 . . . J PACKAGE  
SN74HC375 . . . D OR N PACKAGE  
(TOP VIEW)

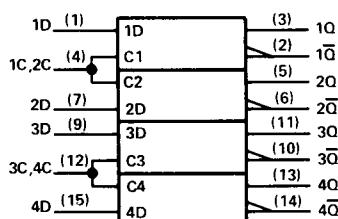


SN54HC375 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J and N packages.

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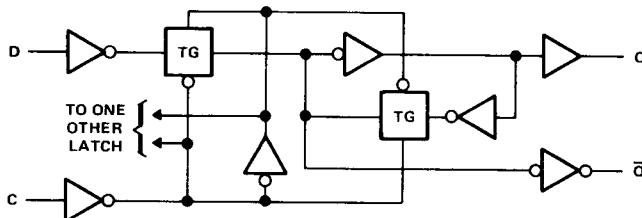
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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range<sup>†</sup>

Supply voltage, V <sub>CC</sub> .....	-0.5 V to 7 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> ) .....	± 20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) .....	± 20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> ) .....	± 25 mA
Continuous current through V <sub>CC</sub> or GND pins .....	± 50 mA
Lead temperature 1.6 mm (1/16 in) from case for 60 s: FK or J package .....	300°C
Lead temperature 1.6 mm (1/16 in) from case for 10 s: D or N package .....	260°C
Storage temperature range .....	- 65°C to 150°C

<sup>†</sup>Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

			SN54HC375			SN74HC375			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6 V	1.5 3.15 4.2			1.5 3.15 4.2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6 V	0 0 0	0.3 0.9 1.2		0 0 0	0.3 0.9 1.2		V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>t</sub>	Input transition (rise and fall) times	V <sub>CC</sub> = 2 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6 V	0 0 0	1000 500 400		0 0 0	1000 500 400		ns
T <sub>A</sub>	Operating free-air temperature		- 55		125	- 40		85	°C

**SN54HC375, SN74HC375  
4-BIT BISTABLE LATCHES**

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC375		SN74HC375		UNIT
			MIN	typ	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.80		5.2		5.34		
		2 V	0.002	0.1		0.1		0.1		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 20 μA	4.5 V	0.001	0.1		0.1		0.1		V
		6 V	0.001	0.1		0.1		0.1		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26		0.4		0.33		
I <sub>l</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	0.15	0.26		0.4		0.33		nA
	I <sub>CC</sub>	6 V	-	-	-	4		80		
	C <sub>i</sub>	2 to 6 V	-	-	-	3	10	10	10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC375		SN74HC375		UNIT
			MIN	MAX		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, C high	2 V	80			120		100		ns
		4.5 V	16			24		20		
		6 V	14			20		17		
t <sub>su</sub>	Setup time, data before C↓	2 V	100			150		125		ns
		4.5 V	20			30		25		
		6 V	17			26		21		
t <sub>h</sub>	Hold time, data after C↓	2 V	5			5		5		ns
		4.5 V	5			5		5		
		6 V	5			5		5		

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C<sub>L</sub> = 50 pF (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC375		SN74HC375		UNIT
				MIN	typ	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q or $\bar{Q}$	2 V	-	40	120	-	180	-	150	ns
			4.5 V	-	14	24	-	36	-	30	
			6 V	-	11	20	-	31	-	26	
t <sub>pd</sub>	C	Q or $\bar{Q}$	2 V	-	42	130	-	195	-	165	ns
			4.5 V	-	15	26	-	39	-	33	
			6 V	-	12	22	-	33	-	28	
t <sub>t</sub>		Any Q or $\bar{Q}$	2 V	-	38	75	-	110	-	95	ns
			4.5 V	-	8	15	-	22	-	19	
			2 V	-	6	13	-	19	-	16	

C <sub>pd</sub>	Power dissipation capacitance	No load, T <sub>A</sub> = 25°C	48 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.