

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC240F, TC74VHC240FW, TC74VHC240FT
TC74VHC244F, TC74VHC244FW, TC74VHC244FT

OCTAL BUS BUFFER
TC74VHC240F/FW/FT INVERTED, 3 - STATE OUTPUTS
TC74VHC244F/FW/FT NON - INVERTED, 3 - STATE OUTPUTS

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74VHC240 and 244 are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

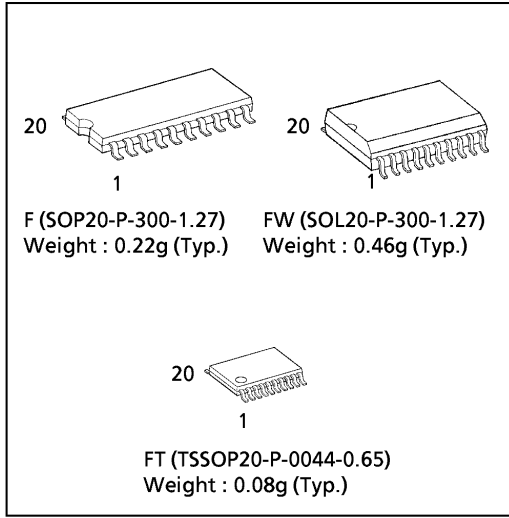
The 74VHC240 is an inverting 3 - state buffer having two active - low output enables. The TC74VHC244 is a non - inverting 3 - state buffer, and has two active - low output enables.

These devices are designed to be used with 3 - state memory address drivers, etc.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

- High Speed..... $t_{pd} = 3.9ns(\text{typ.})$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A(\text{Max.})$ at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr}) = 2V \sim 5.5V$
- Low Noise..... $V_{OLP} = 0.9V (\text{Max.})$
- Pin and Function Compatible with 74ALS240/244

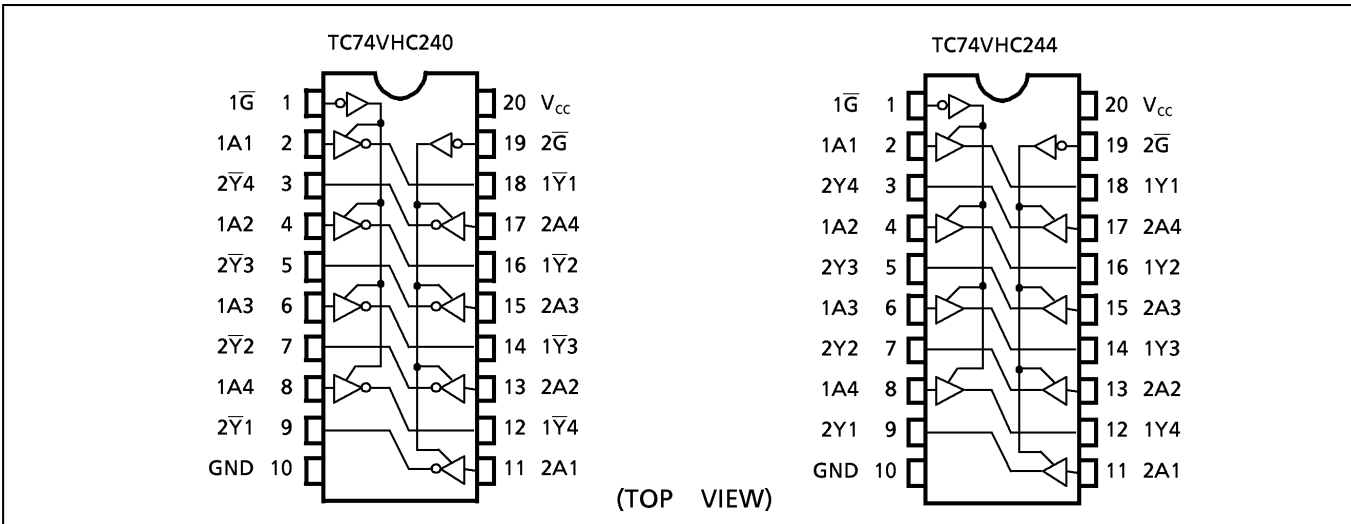


TRUTH TABLE

INPUTS		OUTPUTS	
\bar{G}	A_n	Y_n	\bar{Y}_n
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't Care
 Z : High Impedance
 Y_n : TC74VHC244
 \bar{Y}_n : TC74VHC240

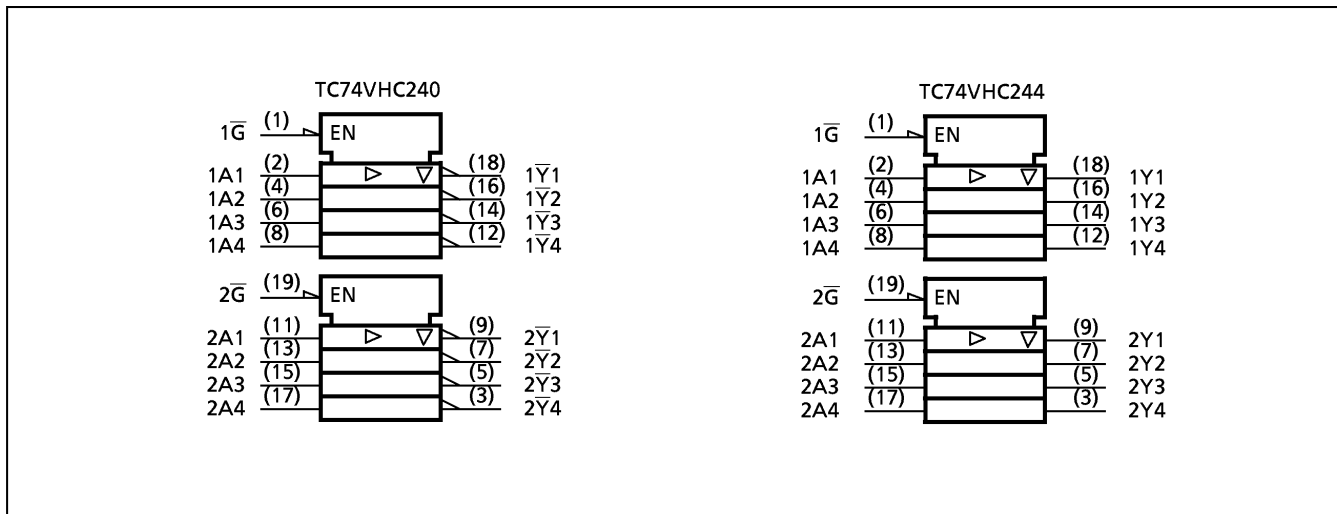
PIN ASSIGNMENT



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IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	- 0.5~7.0	V
DC Input Voltage	V_{IN}	- 0.5~7.0	V
DC Output Voltage	V_{OUT}	- 0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	- 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	- 65~150	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	- 40~85	$^{\circ}C$
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	—	V	
Low - Level Input Voltage	V _{IL}		2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			I _{OH} = -4mA I _{OH} = -8mA	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4mA I _{OL} = 8mA	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	± 0.25	—	± 2.50	μA	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	0~5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0		

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time (TC74VHC240)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	5.3	7.5	1.0	9.0	ns
				50	—	7.8	11.0	1.0	12.5	
			5.0 ± 0.5	15	—	3.6	5.5	1.0	6.5	
				50	—	5.1	7.5	1.0	8.5	
Propagation Delay Time (TC74VHC244)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	
				50	—	8.3	11.9	1.0	13.5	
			5.0 ± 0.5	15	—	3.9	5.5	1.0	6.5	
				50	—	5.4	7.5	1.0	8.5	
3-State Output Enable Time	t _{pZL} t _{pZH}	RL = 1kΩ	3.3 ± 0.3	15	—	6.6	10.6	1.0	12.5	
				50	—	9.1	14.1	1.0	16.0	
			5.0 ± 0.5	15	—	4.7	7.3	1.0	8.5	
				50	—	6.2	9.3	1.0	10.5	
3-State Output Disable Time	t _{pLZ} t _{pHZ}	RL = 1kΩ	3.3 ± 0.3	50	—	10.3	14.0	1.0	16.0	
			5.0 ± 0.5	50	—	6.7	9.2	1.0	10.5	
Output to Output Skew	t _{OSLH} t _{OSHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{IN}				—	4	10	—	pF	
Output Capacitance	C _{OUT}				—	6	—	—		
Power Dissipation Capacitance (Note 2)	C _{PD}	TC74VHC240			—	17	—	—		—
		TC74VHC244			—	19	—	—	—	

Note (1) Parameter guaranteed by design. t_{OSLH} = |t_{pLHm} - t_{pLHn}|, t_{OSHL} = |t_{pHLm} - t_{pHLn}|

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

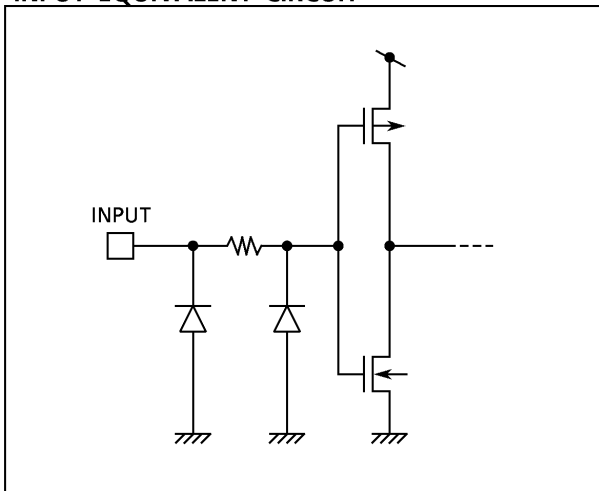
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT	
			V _{CC} (V)	TYP.		LIMIT
Quiet Output Maximum Dynamic VOL	V _{OLP}	CL = 50pF	5.0	0.5 (0.6)	0.8 (0.9)	V
Quiet Output Minimum Dynamic VOL	V _{OLV}	CL = 50pF	5.0	-0.5 (-0.6)	-0.8 (-0.9)	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	CL = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	CL = 50pF	5.0	—	1.5	V

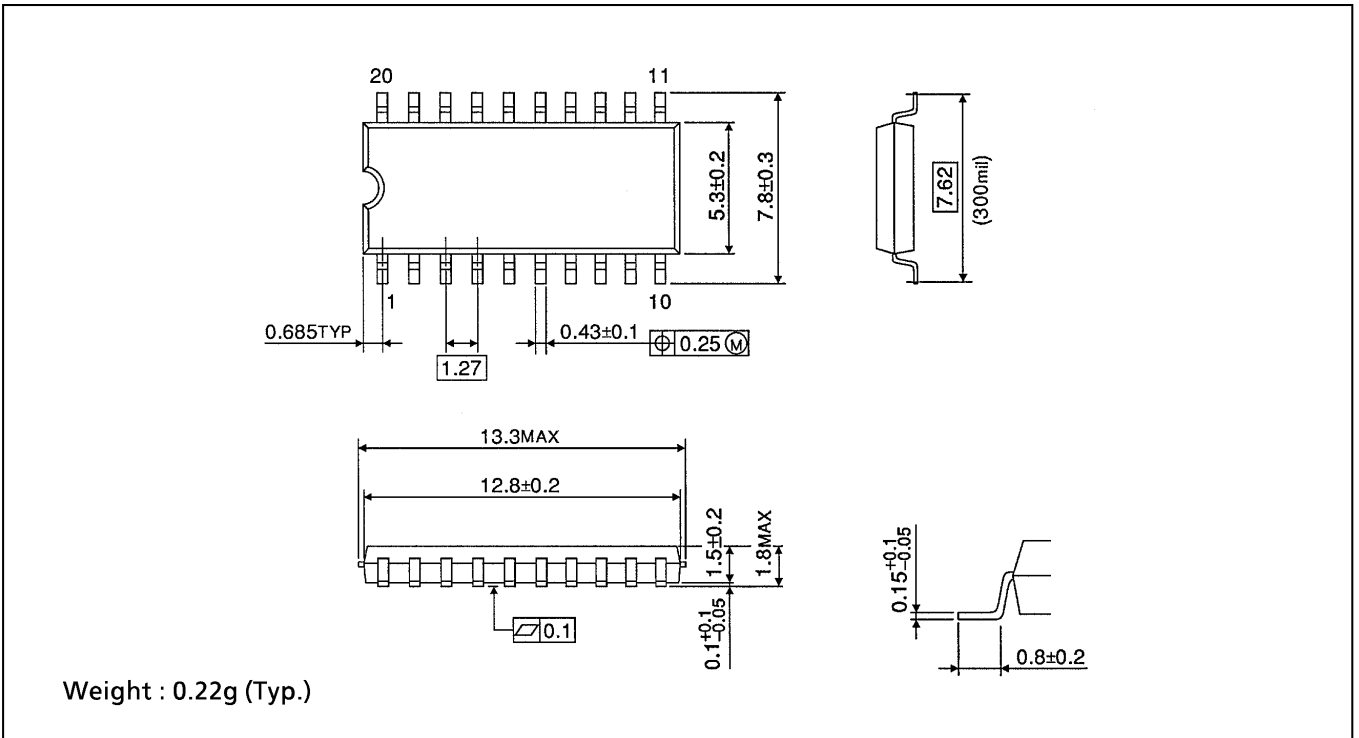
(Note) The value in () only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT



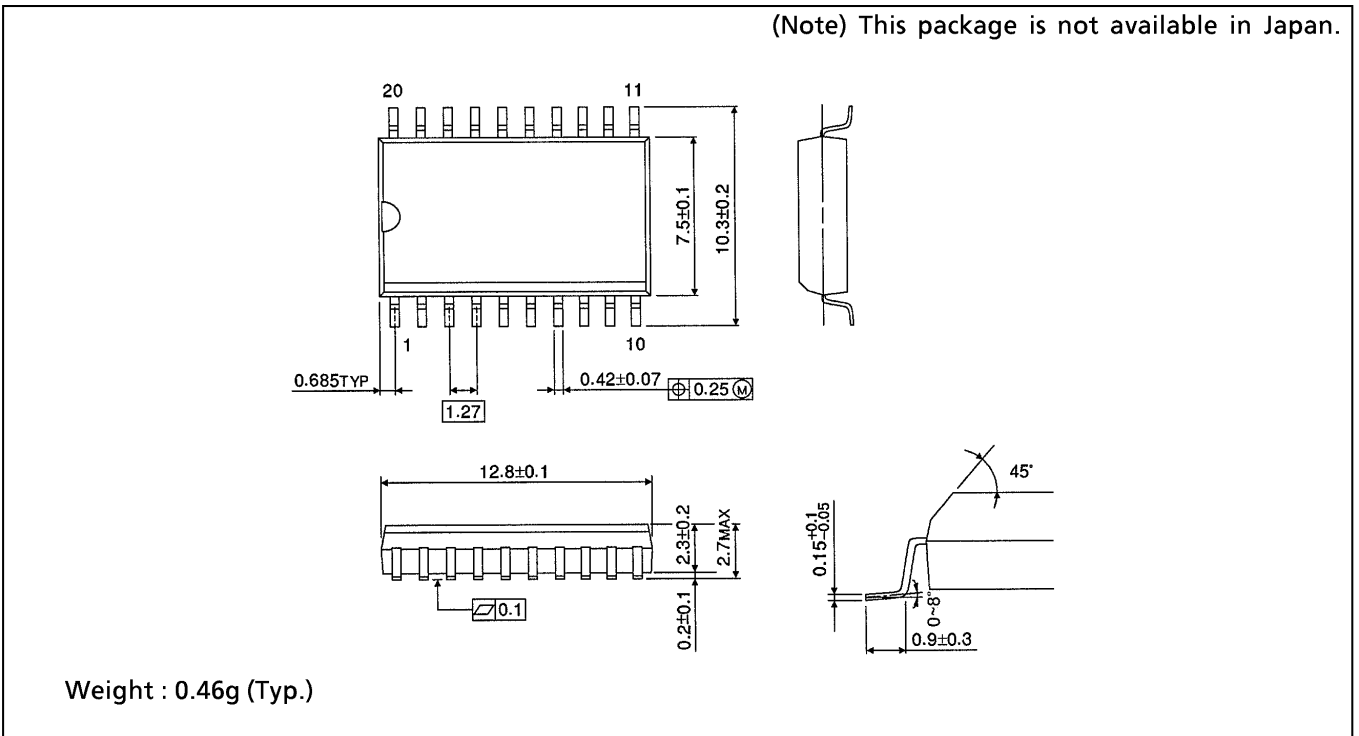
SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm

