Siliconix incorporated

DG5040-5045

Monolithic General Purpose CMOS Analog Switches

FEATURES

- ± 15 Volt Input Range
- ON Resistance < 50 Ω
- Break–Before–Make Switching
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Sample and Hold Circuits

DESCRIPTION

The DG5040 family of solid state analog switches are recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS 40 high voltage CMOS monolithic process, these devices provide ease-of-use and performance advantages to the system designer. Key performance features of the 5040 series are 1 µs switching, low power supply requirements, and break-before-make switching which guarantees that an ON channel will be turned OFF before an OFF channel can turn ON. Each switch conducts equally in either direction, when ON, and blocks up to 30 volts peak-to-peak when OFF. OFF leakage current is 1 nA maximum. A epitaxial layer prevents latch up.

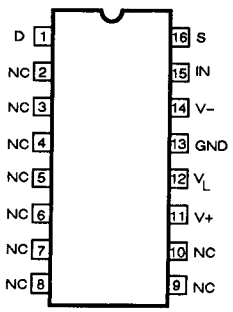
There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and CerDIP. Temperature grades include commercial, C suffix (0 to 70°C), and military, A suffix (–55 to 125°C). For new designs, upgrade to the DG400-405 devices.

5

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE

Dual-In-Line Package



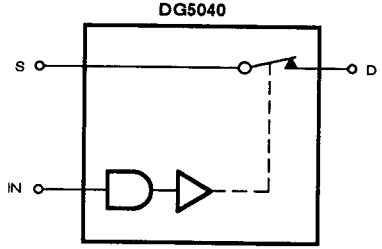
Top View

Order Numbers:

CerDIP: DG5040AK
DG5040CK

Plastic: DG5040CJ

DG5040



One SPST Switch per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON

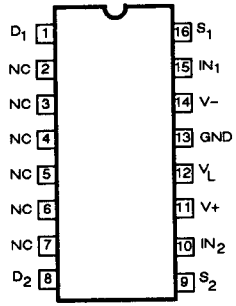
Logic " 0 " ≤ 0.8 V

Logic " 1 " ≥ 2.0 V

*Switches Shown for Logic "1" Input.

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)

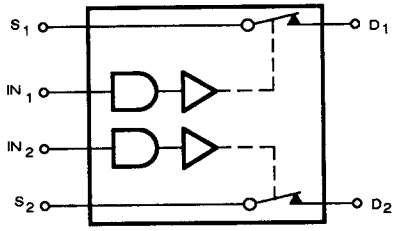
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG5041AK
DG5041CK
Plastic: DG5041CJ

DG5041



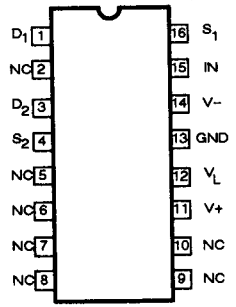
Two SPST Switches per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

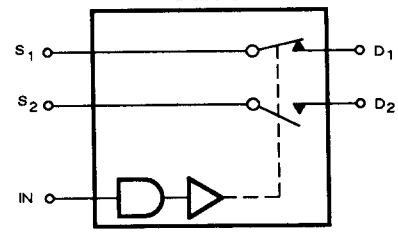
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG5042AK
DG5042CK
Plastic: DG5042CJ

DG5042



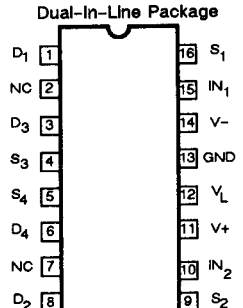
One SPDT Switch per Package

Truth Table*

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

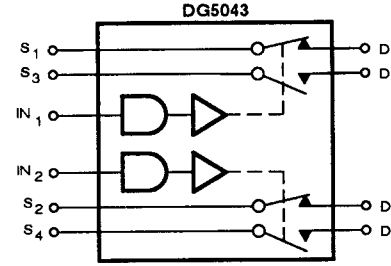
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG5043AK
DG5043CK
Plastic: DG5043CJ

DG5043



Two SPDT Switches per Package*

Truth Table*

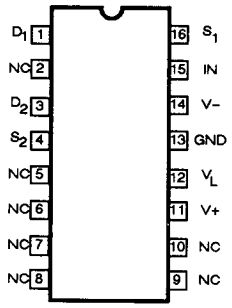
LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)

Dual-In-Line Package



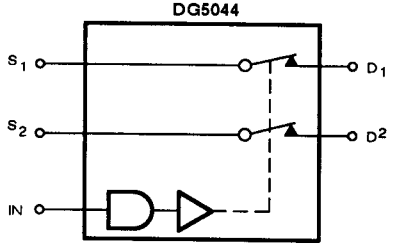
Top View

Order Numbers:

CerDIP: DG5044AK
DG5044CK

Plastic: DG5044CJ

DG5044



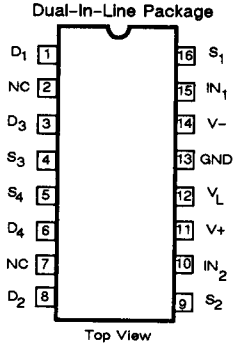
One DPST Switch per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 2.0 V

Dual-In-Line Package



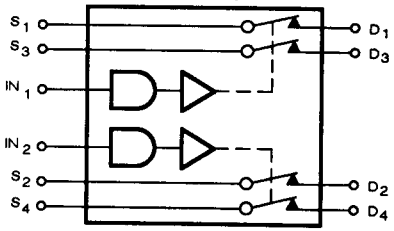
Top View

Order Numbers:

CerDIP: DG5045AK
DG5045CK

Plastic: DG5045CJ

DG5045



Two DPST Switches per Package

Truth Table*

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44V

V_L ..... (GND - 0.3 V) to 44 V

GND 25V

Digital Inputs[f] V_S, V_D ... (V- minus 2 V) to (V+ plus 2 V) or 30 mA, whichever occurs first

Current (any terminal except S or D) ..... 30 mA

Continuous Current (S or D) ..... 30 mA

Peak Current (S or D)
Pulsed 1 ms 10% duty cycle max ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(C Suffix) ..... 0 to 70°C

Power Dissipation*
16-Pin Plastic DIP** ..... 450 mW
16-Pin Ceramic DIP*** ..... 900 mW

* All leads welded or soldered to PC board.
** Derate 6 mW/°C above 75°C
*** Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.0 V, 0.8 V [e]	LIMITS 1=25°C 2=125,70°C 3=−55,0°C		A SUFFIX −55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SWITCH									
Analog Signal Range [c]	V_{ANALOG}		1,2,3		−15	15	−15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = −10 mA, V_D = ±10 V	1,3 2			50 75		50 75	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V_D = −14 V, V_S = 14 V V_D = 14 V, V_S = −14 V	1 2		−1 −100	1 100	−1 −100	1 100	nA
	$I_{D(OFF)}$		1 2		−1 −100	1 100	−1 −100	1 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 14 V	1 2			2 200		2 200	
		V_S = V_D = −14 V	1 2		−2 −200		−2 −200		
INPUT									
Input Current with V_{IN} LOW	I_{IL}	V_{IN} under test = 0.8 V	1,2		−1.0	1.0	−1.0	1.0	µA
Input Current with V_{IN} HIGH	I_{IH}	V_{IN} under test = 2.0 V	1,2		−1.0	1.0	−1.0	1.0	
DYNAMIC									
Turn-ON Time	t_{ON}	V_S = ±10 V, R_L = 1 kΩ, C_L = 35 pF, See Figure 1A	1			1000		1200	ns
Turn-OFF Time	t_{OFF}		1			500		700	
Charge Injection [c]	Q	C_L = 10,000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	1	30					pC
Off Isolation [c]		R_L = 75 Ω, C_L = 5 pF, f = 1 MHz	1	75					dB
Crosstalk [c] (Channel-to-Channel)		R_L = 75 Ω, V_S = 2 Vp-p, f = 1 MHz	1	89					
Source-OFF Capacitance [c]	$C_{S(OFF)}$	V_D = V_S = 0 V, f = 1 MHz	1	15					pF
Drain-OFF Capacitance [c]	$C_{D(OFF)}$		1	17					
Channel ON Capacitance [c]	$C_{D(ON)}$ + $C_{S(ON)}$		1	45					

ELECTRICAL CHARACTERISTICS [a]

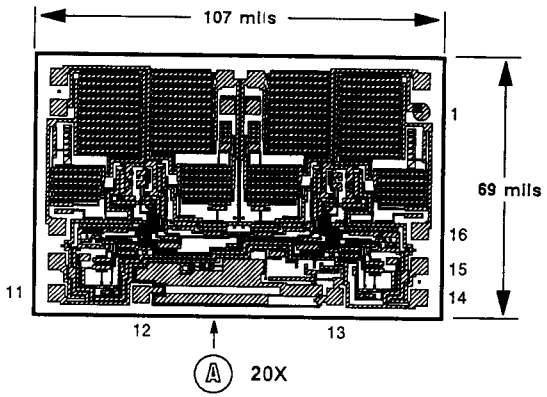
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_+ = 15 V, V_- = -15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.0 V, 0.8 V [e]	LIMITS 1=25°C 2=125,70°C 3=-55,0°C TEMP	TYP [d]	A SUFFIX -55 to 125°C MIN [b]	A SUFFIX -55 to 125°C MAX [b]	C SUFFIX 0 to 70°C MIN [b]	C SUFFIX 0 to 70°C MAX [b]	UNIT
SUPPLY									
Positive Supply Current	I_+	V_{IN} = 0.0 or 2.4 V	1,2			300		300	µA
Negative Supply Current	I_-		1,2		-300		-300		
Logic Supply Current	I_L		1,2			300		300	
Ground Current	I_{GND}		1,2		-300		-300		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = Input voltage to perform proper function.
f. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to 30 mA.

5

DIE TOPOGRAPHY

DG5040

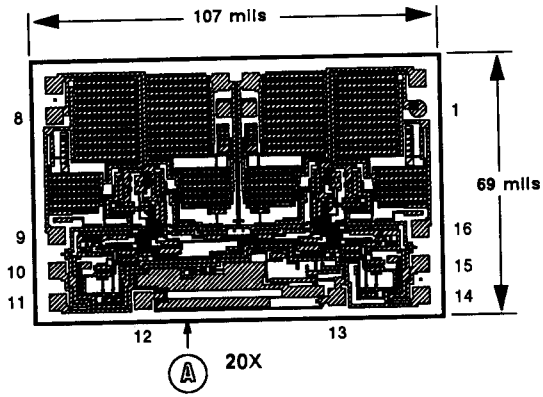


ICMKA
3 Capacitors
5 Resistors
13 P-channel enhancement MOSFET
12 N-channel enhancement MOSFET
7 Diodes

Pad No.	Function
1	Drain
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input
16	Source

DIE TOPOGRAPHY (Cont'd)

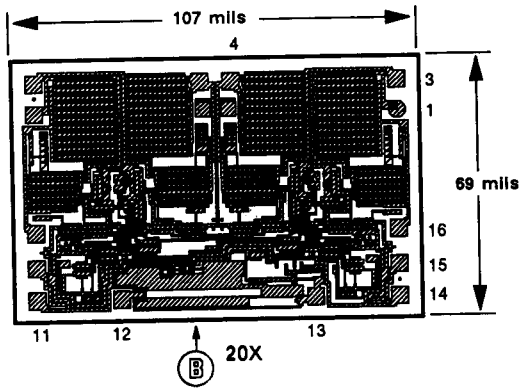
DG5041



ICMKA
5 Capacitors
6 Resistors
25 P-channel enhancement MOSFET
23 N-channel enhancement MOSFET
9 Diodes

Pad No.	Function
1	Drain 1
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input 1
16	Source 1

DG5042

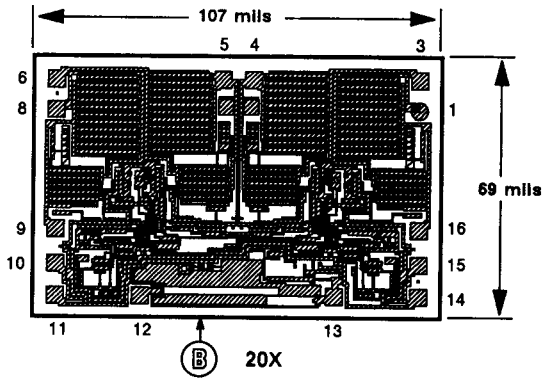


ICMKB
4 Capacitors
5 Resistors
16 P-channel enhancement MOSFET
17 N-channel enhancement MOSFET
7 Diodes

Pad No.	Function
1	Drain 1
3	Drain 2
4	Source 2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input 1
16	Source 1

DIE TOPOGRAPHY (Cont'd)

DG5043



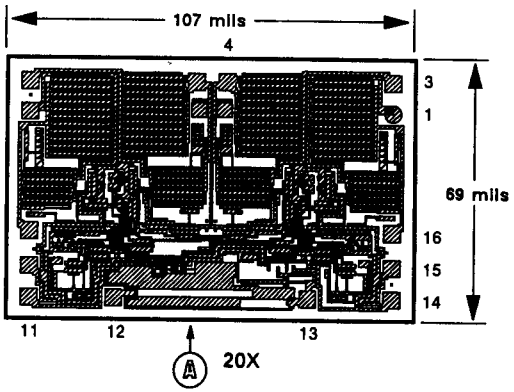
ICMKB

7 Capacitors
6 Resistors
31 P-channel enhancement MOSFET
33 N-channel enhancement MOSFET
9 Diodes

Pad No.	Function
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Souce 2
10	Input 2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input 1
16	Source 1

5

DG5044



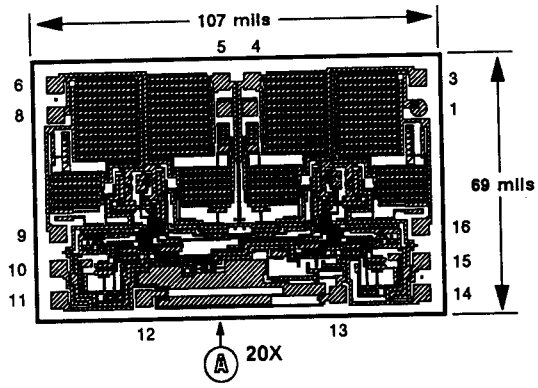
ICMKA

4 Capacitors
5 Resistors
16 P-channel enhancement MOSFET
17 N-channel enhancement MOSFET
7 Diodes

Pad No.	Function
1	Drain 1
3	Drain 2
4	Source 2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input 1
16	Source 1

DIE TOPOGRAPHY (Cont'd)

DG5045

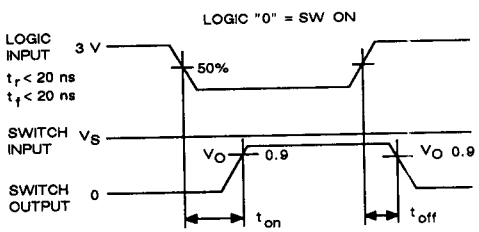


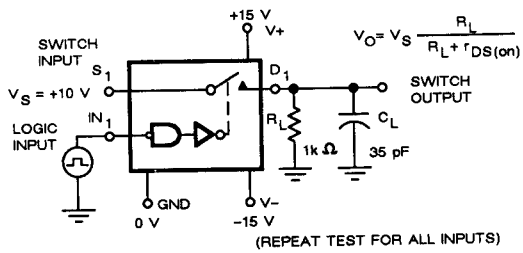
Pad No.	Function
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input 1
16	Source 1

ICMKA
7 Capacitors
6 Resistors
31 P-channel enhancement MOSFET
33 N-channel enhancement MOSFET
9 Diodes

SWITCHING TIME TEST CIRCUIT

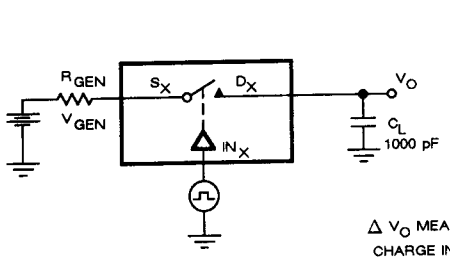
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

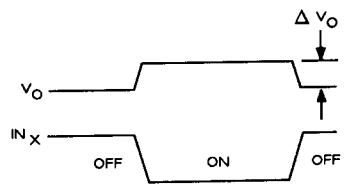




(REPEAT TEST FOR ALL INPUTS)

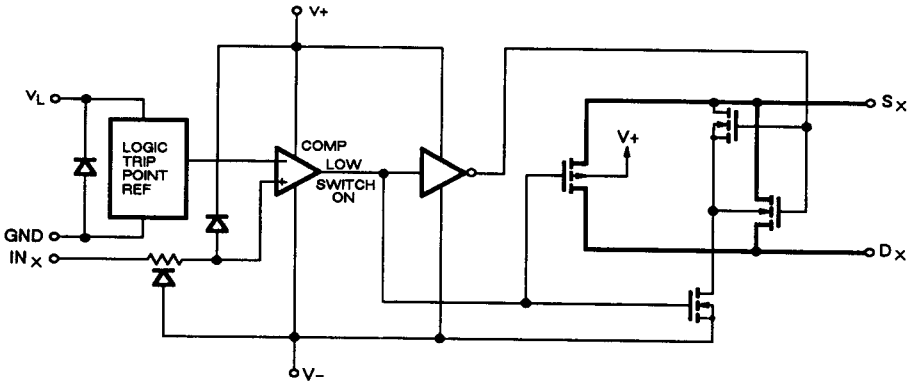
CHARGE INJECTION TEST CIRCUIT





Δ V_O MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION.
CHARGE INJECTION (IN COULOMBS) IS $\Delta Q = C_L \times \Delta V_O$.

SCHEMATIC DIAGRAM (Typical Channel)



DG5140-5145
Low-Power – High-Speed CMOS Analog Switches

Siliconix incorporated

FEATURES

- ± 15 Volt Input Range
- ON Resistance < 50 Ω
- Very Fast Switching Action
  (t_{ON} < 100 ns)
  (t_{OFF} < 75 ns)
- Ultra Low Power Requirements
  (I_S < 1 μA)
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Low Signal Errors
- Break-Before-Make Switching Action
- Reduced Power Consumption
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Precision Switching
- High-Speed Switching
- Battery-Operated Systems

DESCRIPTION

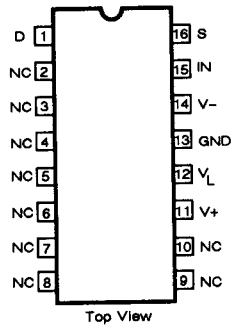
The DG5140 family of solid state analog switches is built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch time ON/OFF performance. Key performance features of the DG5140 series are break-before-make switching action to guarantee that an ON channel will be turned OFF before the OFF channel can turn ON, ultra-low power supply requirements, and TTL and CMOS compatibility. Each switch conducts equally well in both directions when ON and blocks up to 30 Volts peak-to-peak when OFF. With switch OFF leakage less than 100 pA and maximum power supply current of 1 μA (A Suffix), these switches are ideal for battery powered industrial and military applications. An epitaxial layer prevents latchup.

There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and ceramic DIP. Temperature grades include commercial, C suffix (0 to 70°C), and military, A suffix (-55 to 125°C).

PIN CONFIGURATION

Dual-In-Line Package

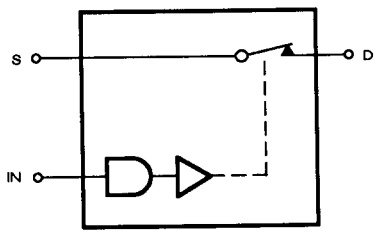


Top View

Order Numbers:
CerDIP: DG5140AK, DG5140AK/883, DG5140CK
Plastic: DG5140CJ

FUNCTIONAL BLOCK DIAGRAM

DG5140



One SPST Switch per Package

Truth Table *

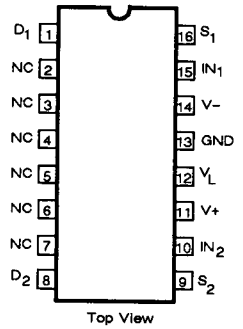
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switches Shown for Logic "1" Input

PIN CONFIGURATION (Cont'd)

Dual-In-Line Package

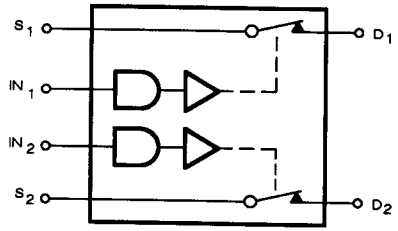


Top View

Order Numbers:
CerDIP: DG5141AK, DG5141AK/883, DG5141CK
Plastic: DG5141CJ

FUNCTIONAL BLOCK DIAGRAM (Cont'd)

DG5141



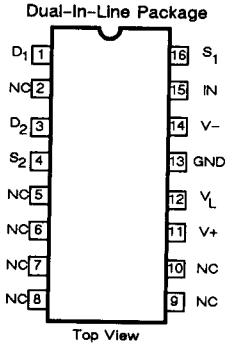
Two SPST Switches per Package

Truth Table *

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 2.4 V

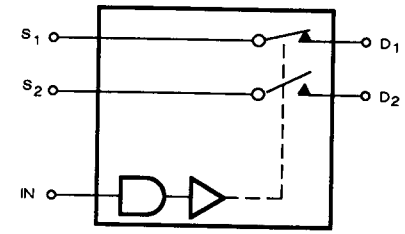
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG5142AK, DG5142AK/883, DG5142CK
Plastic: DG5142CJ

DG5142



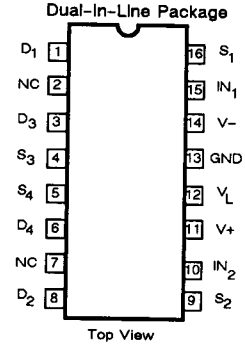
One SPDT Switch per Package

Truth Table *

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 2.4 V

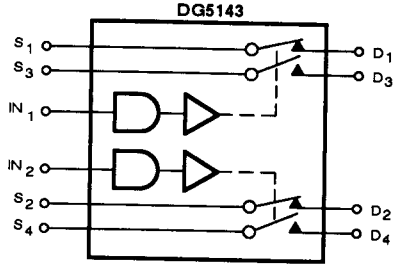
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG5143AK, DG5143AK/883 DG5143CK
Plastic: DG5143CJ

DG5143



Two SPDT Switches per Package

Truth Table *

LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

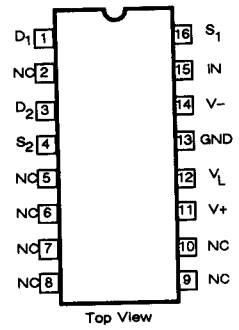
Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 2.4 V

* Switches Shown for Logic "1" Input

5

PIN CONFIGURATION (Cont'd)

Dual-In-Line Package



Top View

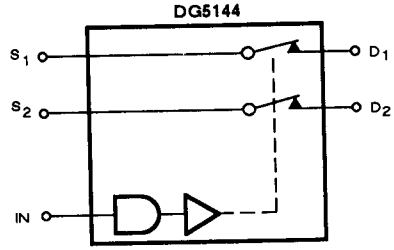
Order Numbers:

CerDIP: DG5144AK, DG5144AK/883, DG5144CK

Plastic: DG5144CJ

FUNCTIONAL BLOCK DIAGRAM (Cont'd)

DG5144



One DPST Switch per Package

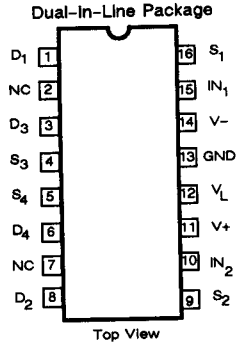
Truth Table *

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " ≤ 0.8 V

Logic " 1 " ≥ 2.4 V

Dual-In-Line Package



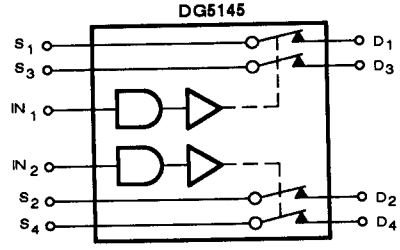
Top View

Order Numbers:

CerDIP: DG5145AK, DG5145AK/883, DG5145CK

Plastic: DG5145CJ

DG5145



Two DPST Switches per Package

Truth Table *

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " ≤ 0.8 V

Logic " 1 " ≥ 2.4 V

* Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

(V+) - (V-) ..... < 36 V

(V+) - (V_D) ..... < 30 V

(V_D) - (V-) ..... < 30 V

(V_D) - (V_S) ..... < ±22 V

(V_L) - (V-) ..... < 33 V

(V_L) - (V_{IN}) ..... < 30 V

V_L ..... < 20 V

V_{IN} ..... < 20 V

Continuous Current, Any Terminal ..... 30 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(C Suffix) ..... 0 to 70°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin CerDIP*** ..... 900 mW

* All leads welded or soldered to PC board.
** Derate 6 mW/°C above 75°C.
*** Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]	LIMITS 1=25°C 2=125,70°C 3=−55,0°C		A SUFFIX −55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SWITCH									
Analog Signal Range [c]	V_{ANALOG}		1,2,3		−14	14	−14	14	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V+ = 15 V, V− = −15 V, I_S = −10 mA, V_D = ±10 V	1 2, 3			50 75		75 100	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V_D = −10 V, V_S = 10 V	1 2			0.5 20		5 20	nA
	$I_{D(OFF)}$	V_D = 10 V, V_S = −10 V	1 2			0.5 20		5 20	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = −10 to 10 V	1 2			1 40		2 40	
INPUT									
Input Current with V_{IN} LOW	I_{IL}	V_{IN} under test = 0.8 V, All Other = 2.4 V	1,2			1		1	µA
Input Current with V_{IN} HIGH	I_{IH}	V_{IN} under test = 2.4 V, All Other = 0.8 V	1,2			1		1	
DYNAMIC									
Turn-ON Time	t_{ON}	R_L = 300Ω, C_L = 35 pF, See Figure 1, DG5140–DG5145	1			150		175	ns
Turn-OFF Time	t_{OFF}		1			125		150	
Switch ON Time [c]	t_{ON}	DG5140, DG5141 — Figure 2	1			100		150	
		DG5140, DG5141 — Figure 3	1			150		175	
		DG5142, DG5143 — Figure 2 and 4	1			175		250	
		DG5142, DG5143 — Figure 5	1			200		300	
		DG5144, DG5145 — Figure 2	1			175		250	
Switch OFF Time [c]	t_{OFF}	DG5140, DG5141 — Figure 2	1			75		125	
		DG5140, DG5141 — Figure 3	1			125		150	
		DG5142, DG5143, DG5144, DG5145 — Figures 2,3,4 and 5	1			125		150	
			1			125		150	

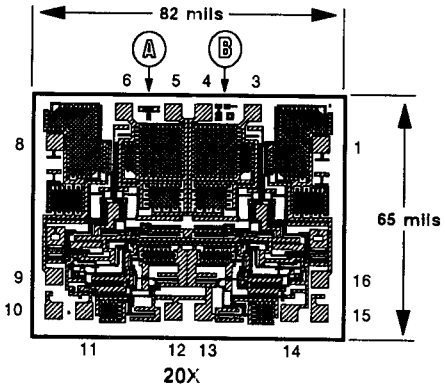
5

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]	LIMITS 1=25°C 2=125,70°C 3=−55,0°C		A SUFFIX −55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC									
Break-Before-Make Time	t_{ON} − t_{OFF}	See Figure 2	1		10		5		ns
			1		10		5		
Charge Injection [c]	Q	C_L = 10,000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	1			100		150	pC
Off Isolation [c]		R_L = 100 Ω, C_L ≤ 5 pF, f = 1 MHz	1		−54		−50		dB
Crosstalk [c] (Channel-to-Channel)		Any Other Channel Switches, R_L = 100 Ω, C_L ≤ 5 pF, f = 1 MHz	1			−54		−50	
SUPPLY									
Positive Supply Current	I+	V_{IN} = 0 V or 5 V, Switch Duty Cycle < 10%	1			1		10	µA
Negative Supply Current	I−		1		−1		−10		
Logic Supply Current	I_L		1			1		10	
Ground Current	I_{GND}		1		−1		−10		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to 30 mA.

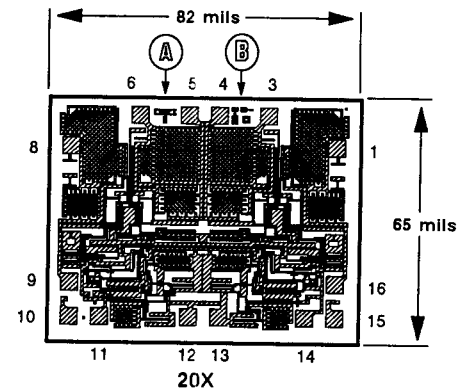
DG5140



CSHCA/B
2 Capacitors
2 Resistors
8 P-channel enhancement MOSFETS
10 N-channel enhancement MOSFETS
2 Diodes

Pad No.	Function
1	D
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	V+ (substrate)
12	V_L
13	GND
14	V-
15	IN
16	S

DG5141



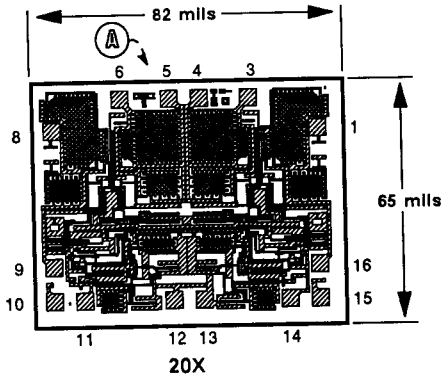
CSHCA/B
4 Capacitors
4 Resistors
16 P-channel enhancement MOSFETS
20 N-channel enhancement MOSFETS
4 Diodes

Pad No.	Function
1	D_1
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	D_2
9	S_2
10	IN_2
11	V+ (substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

5

DIE TOPOGRAPHY (Cont'd)

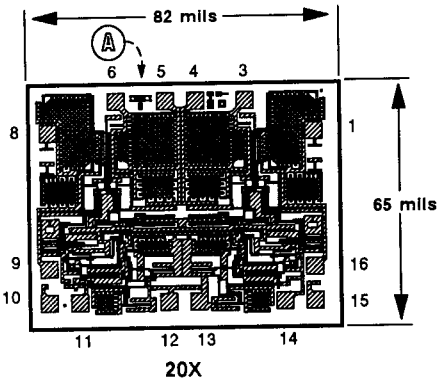
DG5142



CSHCA
2 Resistors
4 Capacitors
11 P-channel enhancement MOSFETS
15 N-channel enhancement MOSFETS
2 Diodes

Pad No.	Function
1	D_1
2	NC
3	D_2
4	S_2
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	V+ (substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

DG5143

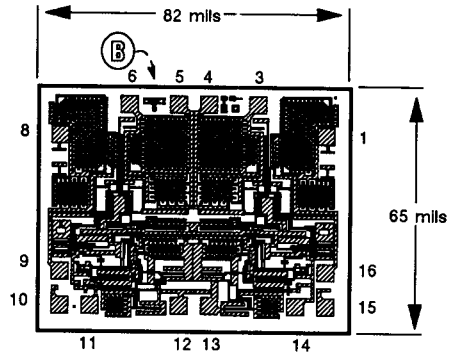


CSHCA
8 Capacitors
4 Resistors
22 P-channel enhancement MOSFETS
30 N-channel enhancement MOSFETS
4 Diodes

Pad No.	Function
1	D_1
2	NC
3	D_3
4	S_3
5	S_4
6	D_4
7	NC
8	D_2
9	S_2
10	IN_2
11	V+ (substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

DIE TOPOGRAPHY (Cont'd)

DG5144

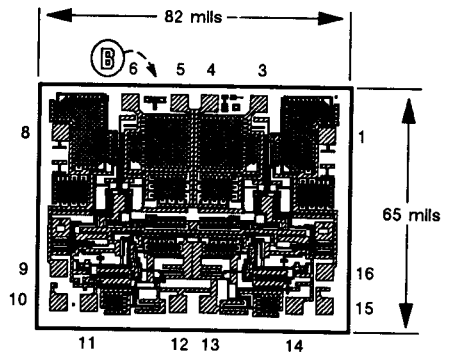


20X

CSHCB
2 Resistors
4 Capacitors
11 P-channel enhancement MOSFETS
15 N-channel enhancement MOSFETS
2 Diodes

Pad No.	Function
1	D_1
2	NC
3	D_2
4	S_2
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	V+ (substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

DG5145



20X

CSHCB
8 Capacitors
4 Resistors
22 P-channel enhancement MOSFETS
30 N-channel enhancement MOSFETS
4 Diodes

Pad No.	Function
1	D_1
2	NC
3	D_3
4	S_3
5	S_4
6	D_4
7	NC
8	D_2
9	S_2
10	IN_2
11	V+ (substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

5

SWITCHING TIME TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

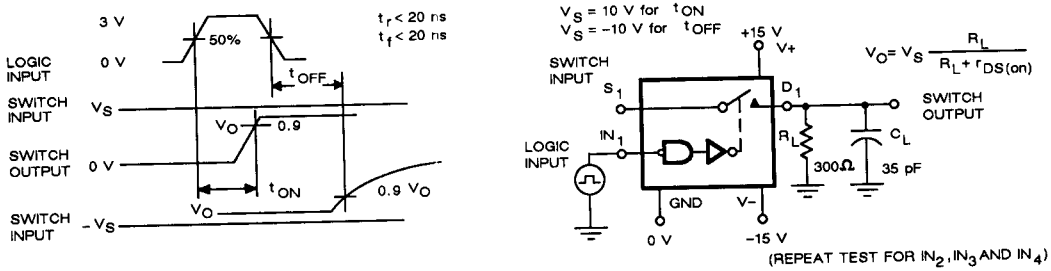


Figure 1.

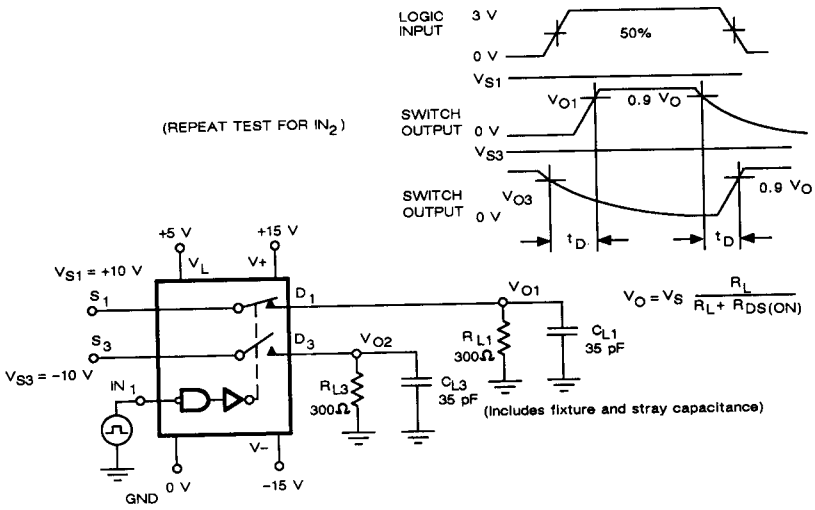


Figure 2.