



HIGH-SPEED CMOS DUAL 4-INPUT MULTIPLEXER

IDTQS74FCT253AT

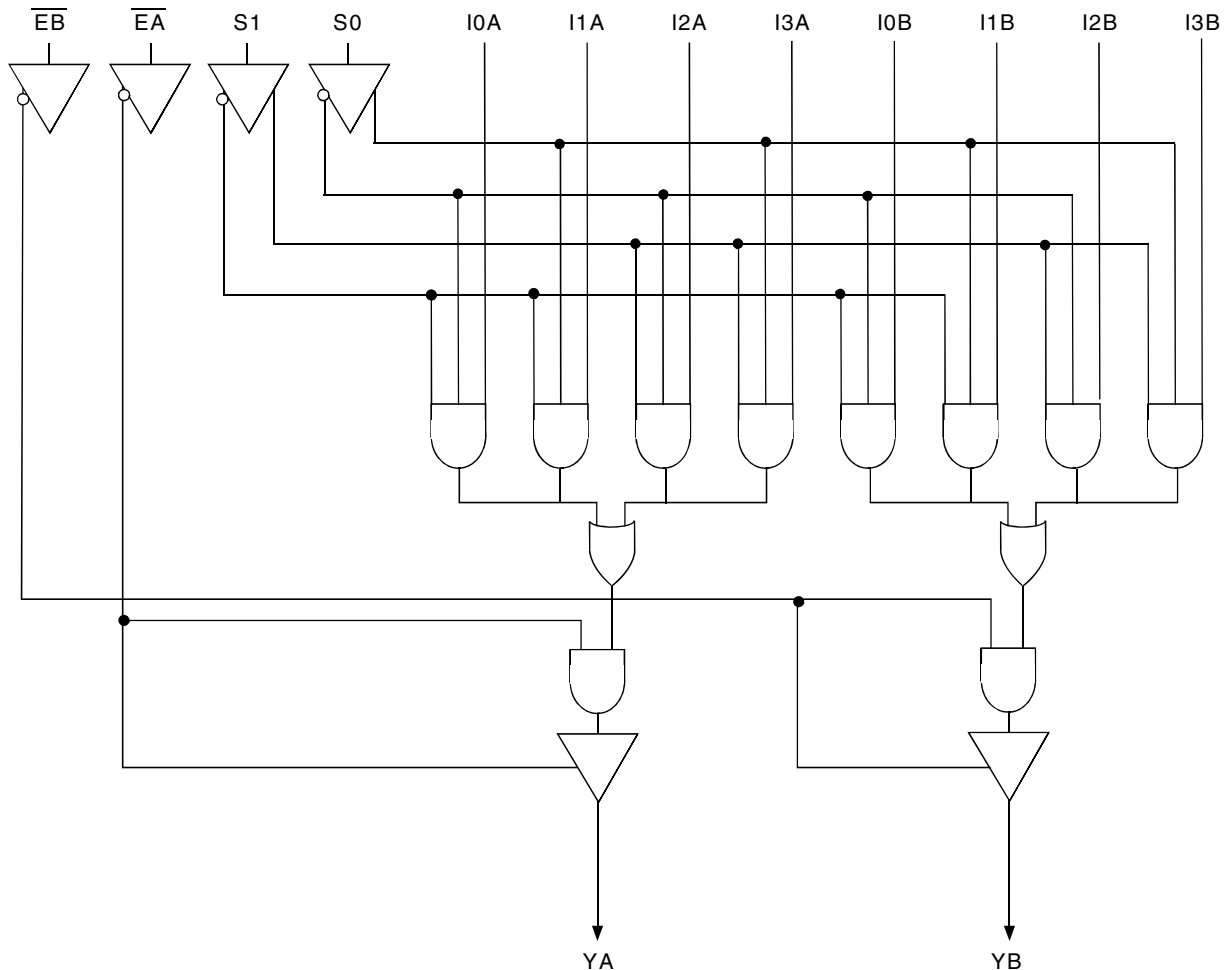
FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- $I_{OL} = 48mA$
- Available in SOIC, QSOP, and S1 packages

DESCRIPTION:

The IDTQS74FCT253AT is a high-speed CMOS TTL-compatible dual 4-input multiplexer with 3-state outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

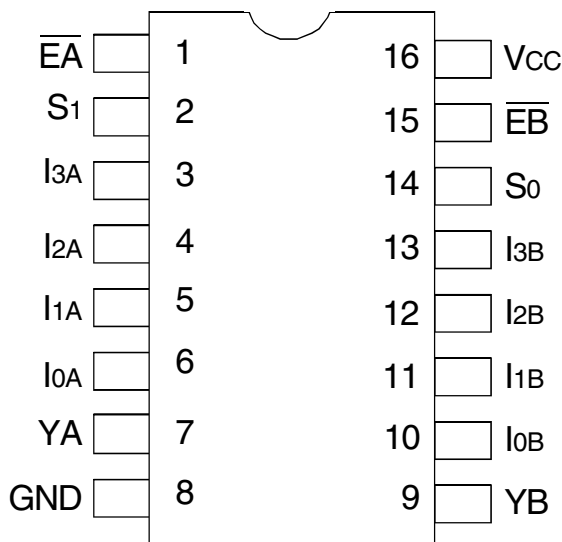


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INDUSTRIAL TEMPERATURE RANGE

MARCH 2001

PIN CONFIGURATION



SOIC/ QSOP/ S1
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current Max Current Sink/Pin	+120	mA
I _{IK}	Input Diode Current, V _{IN} < 0	-20	mA
I _{OK}	DC Output Current, V _{OUT} < 0	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4	—	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	—	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
I _x	I	Data In
S _x	I	Select
\overline{EA} , \overline{EB}	I	Enable
YA, YB	O	Data Out

FUNCTION TABLE⁽¹⁾

Enable		Select		Outputs		Function
\overline{EA}	\overline{EB}	S ₀	S ₁	YA	YB	
H	X	X	X	Z	Z	Disable A
X	H	X	X	X	Z	Disable B
L	L	L	L	I _{0A}	I _{0B}	S ₁ - 0 = 0
L	L	L	H	I _{1A}	I _{1B}	S ₁ - 0 = 1
L	L	H	L	I _{2A}	I _{2B}	S ₁ - 0 = 2
L	L	H	H	I _{3A}	I _{3B}	S ₁ - 0 = 3

NOTE:

1. H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	± 5	μA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2)}$		-60	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^{\circ}\text{C}$		—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	—	—	0.5	V

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
2. This parameter is guaranteed but not tested

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ $\text{freq} = 0$	—	2	mA
I_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under DC Electrical Characteristics.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$).
3. For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Output Frequency
 N_i = Number of Outputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

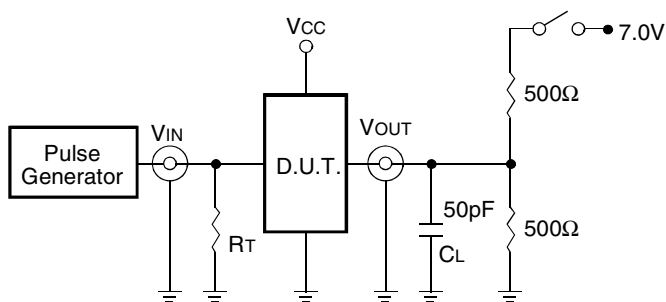
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Min.	Max.	Unit
t _{IV}	Propagation Delay I _x to Y	1.5	5.2	ns
t _{SY}	Propagation Delay S _x to Y	1.5	6.6	ns
t _{PZH} t _{PZL}	Output Enable Time \bar{E} to Y	1.5	6	ns
t _{PHZ} t _{PLZ}	Output Disable Time \bar{E} to Y	1.5	6	ns

NOTES:

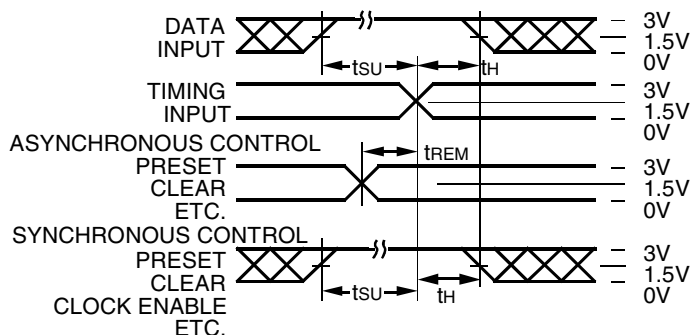
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

TEST CIRCUITS AND WAVEFORMS



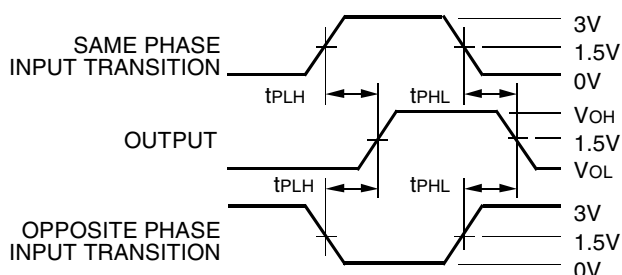
FCTL Link

Test Circuits for All Outputs



FCTL Link

Set-Up, Hold, and Release Times



FCTL Link

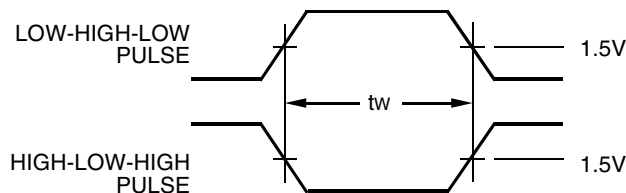
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

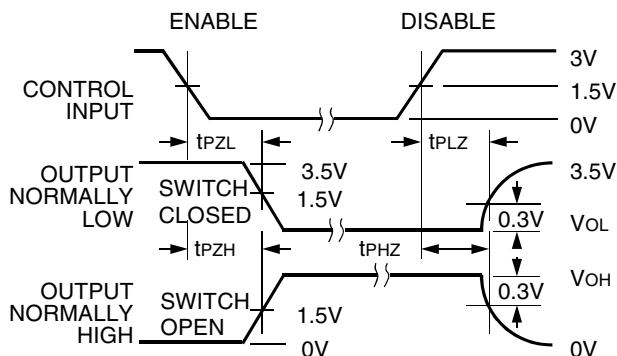
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



FCTL Link

Pulse Width



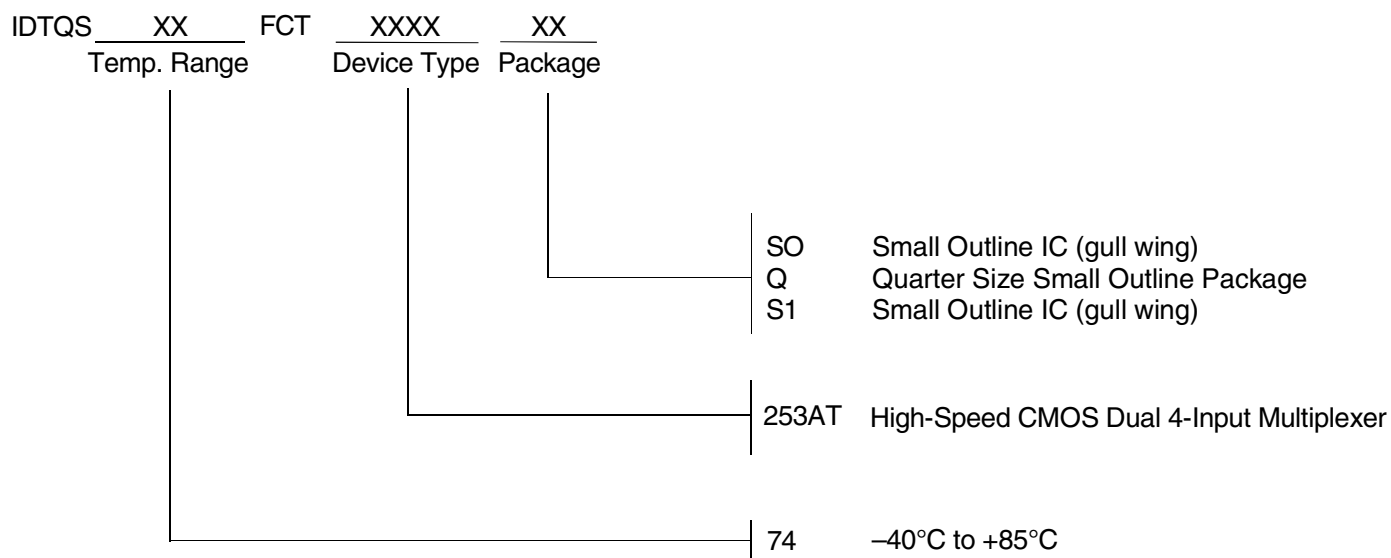
FCTL Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



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