



### 3.3V CMOS OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCH573A**

#### FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-rail output swing for increased noise margin
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SOIC, SSOP, QSOP, and TSSOP packages

#### DRIVE FEATURES:

- High Output Drivers: ±24mA
- Reduced system switching noise

#### APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

#### DESCRIPTION:

The LVCH573A octal transparent D-type latch is built using advanced dual metal CMOS technology. The device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads, and is particularly suitable for implementing buffer registers, input-output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

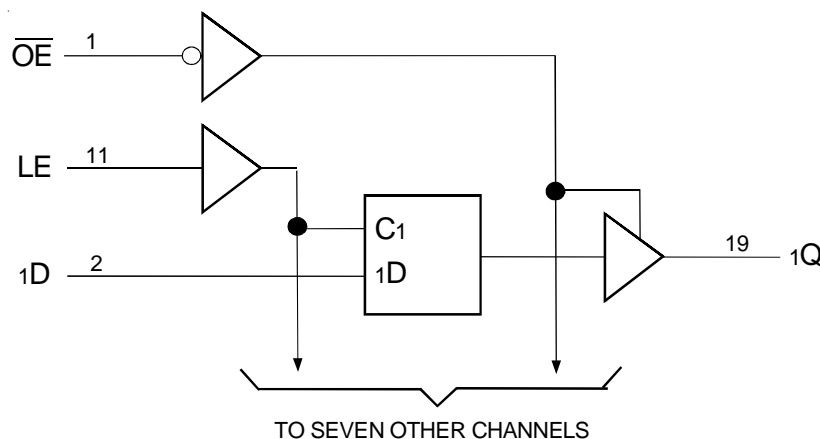
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.  $\overline{OE}$  does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The LVCH573A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

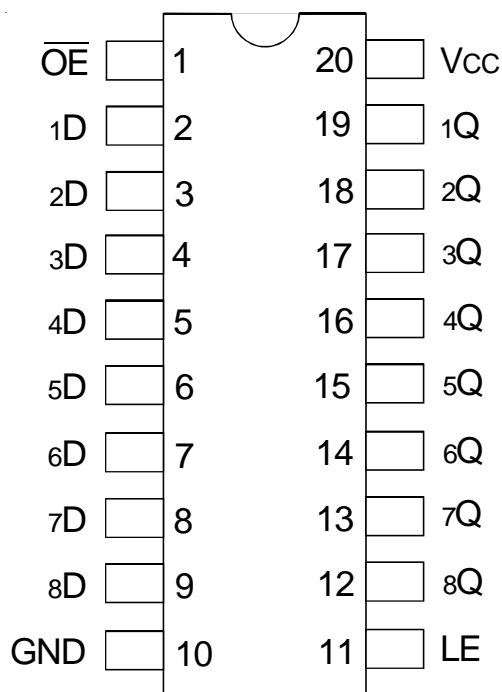
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVCH573A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

#### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                             | Description   | Max          | Unit |
|------------------------------------|---|--------------|------|
| V <sub>TERM</sub>                  | Terminal Voltage with Respect to GND                                  | -0.5 to +6.5 | V    |
| T <sub>STG</sub>                   | Storage Temperature   | -65 to +150  | °C   |
| I <sub>OUT</sub>                   | DC Output Current   | -50 to +50   | mA   |
| I <sub>IK</sub><br>I <sub>OK</sub> | Continuous Clamp Current,<br>V <sub>I</sub> < 0 or V <sub>O</sub> < 0 | -50          | mA   |
| I <sub>CC</sub><br>I <sub>SS</sub> | Continuous Current through each<br>V <sub>CC</sub> or GND             | ±100         | mA   |

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 4.5  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 5.5  | 8    | pF   |
| C <sub>I/O</sub> | I/O Port Capacitance     | V <sub>IN</sub> = 0V  | 6.5  | 8    | pF   |

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

| Pin Names       | Description                       |
|-----------------|-----------------------------------|
| $\overline{OE}$ | Output Enable Inputs (Active LOW) |
| LE              | Latch Enable Input                |
| xD              | Data Inputs <sup>(1)</sup>        |
| xQ              | 3-State Outputs                   |

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH LATCH)<sup>(1)</sup>

| Inputs |    |                 | Outputs          |
|--------|----|-----------------|------------------|
| xD     | LE | $\overline{OE}$ | xQ               |
| H      | H  | L               | H                |
| L      | H  | L               | L                |
| X      | L  | L               | Q <sup>(2)</sup> |
| X      | X  | H               | Z                |

### NOTES:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High-Impedance
- Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

| Symbol   | Parameter  | Test Conditions   |   | Min. | Typ. <sup>(1)</sup> | Max. | Unit |
|--|--|---|---|------|---------------------|------|------|
| V <sub>IH</sub>  | Input HIGH Voltage Level                               | V <sub>CC</sub> = 2.3V to 2.7V  |   | 1.7  | —                   | —    | V    |
|  |  | V <sub>CC</sub> = 2.7V to 3.6V  |   | 2    | —                   | —    |      |
| V <sub>IL</sub>  | Input LOW Voltage Level                                | V <sub>CC</sub> = 2.3V to 2.7V  |   | —    | —                   | 0.7  | V    |
|  |  | V <sub>CC</sub> = 2.7V to 3.6V  |   | —    | —                   | 0.8  |      |
| I <sub>IH</sub><br>I <sub>IL</sub>                       | Input Leakage Current                                  | V <sub>CC</sub> = 3.6V  | V <sub>I</sub> = 0 to 5.5V                  | —    | —                   | ±5   | μA   |
| I <sub>OZH</sub><br>I <sub>OZL</sub>                     | High Impedance Output Current<br>(3-State Output pins) | V <sub>CC</sub> = 3.6V  | V <sub>O</sub> = 0 to 5.5V                  | —    | —                   | ±10  | μA   |
| I <sub>OFF</sub>   | Input/Output Power Off Leakage                         | V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 5.5V              |   | —    | —                   | ±50  | μA   |
| V <sub>IK</sub>  | Clamp Diode Voltage                                    | V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA                             |   | —    | -0.7                | -1.2 | V    |
| V <sub>H</sub>   | Input Hysteresis                                       | V <sub>CC</sub> = 3.3V  |   | —    | 100                 | —    | mV   |
| I <sub>CC1</sub><br>I <sub>CC2</sub><br>I <sub>CC3</sub> | Quiescent Power Supply Current                         | V <sub>CC</sub> = 3.6V  | V <sub>IN</sub> = GND or V <sub>CC</sub>    | —    | —                   | 10   | μA   |
|  |  |   | 3.6 ≤ V <sub>IN</sub> ≤ 5.5V <sup>(2)</sup> | —    | —                   | 10   |      |
| ΔI <sub>CC</sub>   | Quiescent Power Supply Current Variation               | One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND |   | —    | —                   | 500  | μA   |

### NOTES:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

| Symbol                                 | Parameter <sup>(1)</sup>         | Test Conditions        |                            | Min. | Typ. <sup>(2)</sup> | Max. | Unit |
|--|----------------------------------|------------------------|----------------------------|------|---------------------|------|------|
| I <sub>BHH</sub><br>I <sub>BHL</sub>   | Bus-Hold Input Sustain Current   | V <sub>CC</sub> = 3V   | V <sub>I</sub> = 2V        | -75  | —                   | —    | μA   |
|  |                                  |                        | V <sub>I</sub> = 0.8V      | 75   | —                   | —    |      |
| I <sub>BHH</sub><br>I <sub>BHL</sub>   | Bus-Hold Input Sustain Current   | V <sub>CC</sub> = 2.3V | V <sub>I</sub> = 1.7V      | —    | —                   | —    | μA   |
|  |                                  |                        | V <sub>I</sub> = 0.7V      | —    | —                   | —    |      |
| I <sub>BHHO</sub><br>I <sub>BHLO</sub> | Bus-Hold Input Overdrive Current | V <sub>CC</sub> = 3.6V | V <sub>I</sub> = 0 to 3.6V | —    | —                   | ±500 | μA   |

### NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol          | Parameter           | Test Conditions <sup>(1)</sup> |                           | Min.                     | Max. | Unit |
|-----------------|---------------------|--------------------------------|---------------------------|--------------------------|------|------|
| V <sub>OH</sub> | Output HIGH Voltage | V <sub>CC</sub> = 2.3V to 3.6V | I <sub>OH</sub> = - 0.1mA | V <sub>CC</sub> - 0.2    | —    | V    |
|                 |                     | V <sub>CC</sub> = 2.3V         | I <sub>OH</sub> = - 6mA   | 2                        | —    |      |
|                 |                     | V <sub>CC</sub> = 2.3V         | I <sub>OH</sub> = - 12mA  | 1.7                      | —    |      |
|                 |                     | V <sub>CC</sub> = 2.7V         |                           | 2.2                      | —    |      |
|                 |                     | V <sub>CC</sub> = 3V           |                           | 2.4                      | —    |      |
|                 |                     | V <sub>CC</sub> = 3V           |                           | I <sub>OH</sub> = - 24mA | 2.2  |      |
| V <sub>OL</sub> | Output LOW Voltage  | V <sub>CC</sub> = 2.3V to 3.6V | I <sub>OL</sub> = 0.1mA   | —                        | 0.2  | V    |
|                 |                     | V <sub>CC</sub> = 2.3V         | I <sub>OL</sub> = 6mA     | —                        | 0.4  |      |
|                 |                     |                                | I <sub>OL</sub> = 12mA    | —                        | 0.7  |      |
|                 |                     | V <sub>CC</sub> = 2.7V         | I <sub>OL</sub> = 12mA    | —                        | 0.4  |      |
|                 |                     | V <sub>CC</sub> = 3V           | I <sub>OL</sub> = 24mA    | —                        | 0.55 |      |

**NOTE:**  
1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 25°C

| Symbol | Parameter  | Test Conditions                 | Typical | Unit |
|--------|--|---------------------------------|---------|------|
| CPD    | Power Dissipation Capacitance per Latch Outputs enabled  | C <sub>L</sub> = 0pF, f = 10Mhz | 37      | pF   |
| CPD    | Power Dissipation Capacitance per Latch Outputs disabled |                                 | 4       |      |

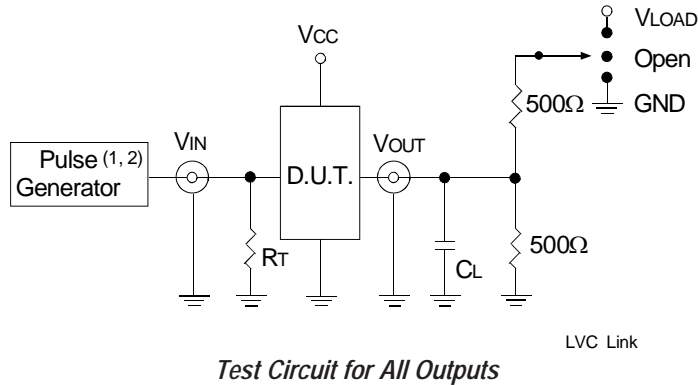
## SWITCHING CHARACTERISTICS<sup>(1)</sup>

| Symbol                               | Parameter                                    | V <sub>CC</sub> = 2.7V |      | V <sub>CC</sub> = 3.3V ± 0.3V |      | Unit |
|--------------------------------------|--|------------------------|------|-------------------------------|------|------|
|                                      |  | Min.                   | Max. | Min.                          | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>xD to xQ                | —                      | 7.7  | 1.5                           | 6.9  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>LE to xQ                | —                      | 8.4  | 2                             | 7.7  | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>$\overline{OE}$ to xQ  | —                      | 8.5  | 1.5                           | 7.5  | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>$\overline{OE}$ to xQ | —                      | 7    | 1.6                           | 6.5  | ns   |
| t <sub>w</sub>                       | Pulse Duration LE HIGH                       | 3.3                    | —    | 3.3                           | —    | ns   |
| t <sub>SU</sub>                      | Set-up Time, data before LE↓                 | 2                      | —    | 2                             | —    | ns   |
| t <sub>H</sub>                       | Hold Time, data after LE↓                    | 1.5                    | —    | 1.5                           | —    | ns   |
| t <sub>sk(o)</sub>                   | Output Skew <sup>(2)</sup>                   | —                      | —    | —                             | 500  | ps   |

**NOTES:**  
1. See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = - 40°C to + 85°C.  
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS  
TEST CONDITIONS

| Symbol            | V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V | V <sub>CC</sub> <sup>(1)</sup> =2.7V | V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V | Unit |
|-------------------|---|--------------------------------------|---|------|
| V <sub>LOAD</sub> | 6   | 6                                    | 2 x V <sub>CC</sub>                       | V    |
| V <sub>IH</sub>   | 2.7                                       | 2.7                                  | V <sub>CC</sub>                           | V    |
| V <sub>T</sub>    | 1.5                                       | 1.5                                  | V <sub>CC</sub> / 2                       | V    |
| V <sub>LZ</sub>   | 300                                       | 300                                  | 150                                       | mV   |
| V <sub>HZ</sub>   | 300                                       | 300                                  | 150                                       | mV   |
| C <sub>L</sub>    | 50  | 50                                   | 30  | pF   |



Test Circuit for All Outputs

DEFINITIONS:

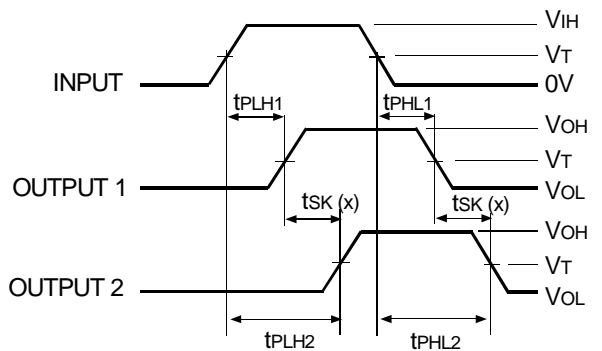
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

SWITCH POSITION

| Test                                    | Switch            |
|---|-------------------|
| Open Drain<br>Disable Low<br>Enable Low | V <sub>LOAD</sub> |
| Disable High<br>Enable High             | GND               |
| All Other Tests                         | Open              |

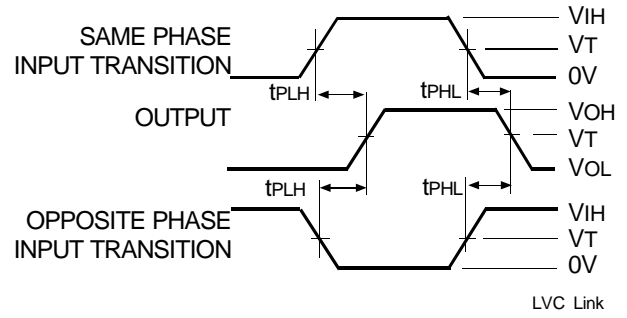


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

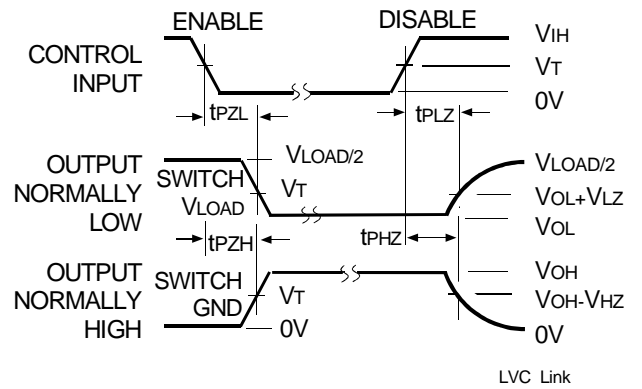
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



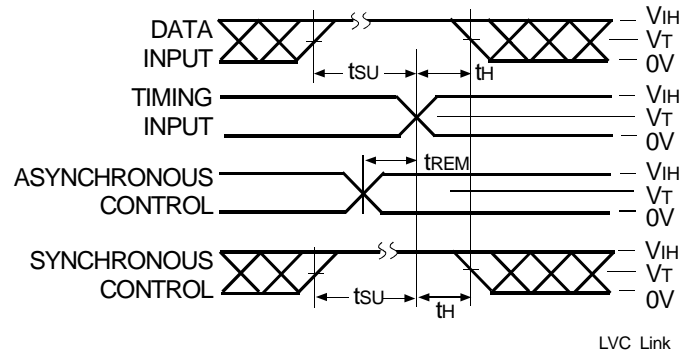
Propagation Delay



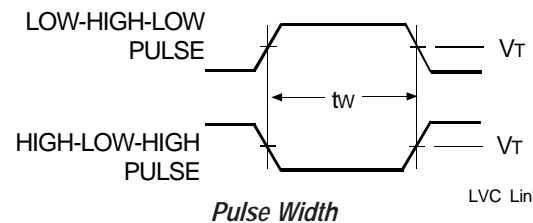
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

| IDT         | XX       | LVC         | X       | XXXX | XX |  |
|-------------|----------|-------------|---------|------|----|--|
| Temp. Range | Bus-Hold | Device Type | Package |      |    |  |
|             |          |             |         |      |    | SO Small Outline IC (gull wing)  |
|             |          |             |         |      |    | PY Shrink Small Outline Package  |
|             |          |             |         |      |    | Q Quarter Size Small Outline Package                                   |
|             |          |             |         |      |    | PG Thin Shrink Small Outline Package                                   |
|             |          |             |         | 573A |    | Octal Transparent D-Type Latch with 3-State Outputs, $\pm 24\text{mA}$ |
|             |          |             | H       |      |    | Bus-hold   |
|             |          |             |         |      | 74 | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$                         |



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