CS-3524A

Voltage Mode PWM Control Circuit with 200mA Output Drivers

Description

The CS-3524A PWM control circuit retains the same versatile architecture of the industry standard CS-3524 (SG3524) while adding substantial improvements.

The CS-3524 is pin-compatible with "non-A" versions, and in most applications can be directly interchanged. The CS-3524A, however, eliminates many of the design restrictions which had previously required additional external circuitry.

The CS-3524A includes a precision 5V reference trimmed to ±1% accuracy (eliminating the need for potentiometer adjustments), an error amplifier with an output voltage swing extending to 5V, and a current sense amplifier useful in either the ground or power supply output lines. The uncommitted 60V, 200mA NPN output pair greatly enhances the output drive capability.

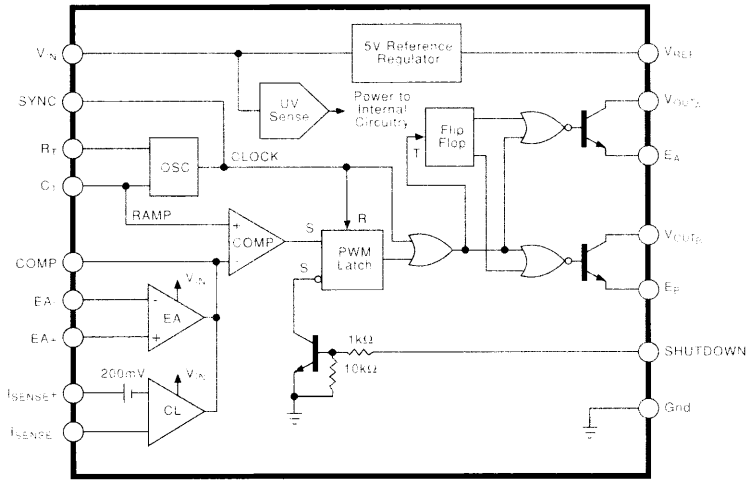
The CS-3524A features an undervoltage lockout circuit which disables all internal circuitry (except the reference) until the input voltage has risen to 8V. This holds standby current low until turn-on, and greatly simplifies the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter free activation.

Other improvements include a PWM latch that insures freedom from multiple pulsing within a period, even in noisy environments; logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit is usable to 500kHz and is easier to synchronize with an external clock pulse.

Features

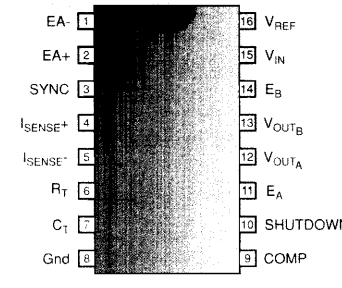
- **Precision Reference Internally Trimmed to ±1%**
- **Current Limit**
- **Undervoltage Lockout**
- **Start-up Supply Current < 4mA**
- **Output to 200mA**
- **60V Output Capability**
- **Wide Common-mode Input Range for Error and Current Limit Amplifiers**
- **PWM Latch Insures Single Pulse per Period**
- **Double Pulse Suppression**
- **200ns Shutdown**
- **Guaranteed Frequency**
- **Thermal Shutdown**

Block Diagram



Package Options

16 Lead PDIP & SO Wide



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Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_{CC}) 60V
Output Current (Each Output) 200mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_J=+25°C 2000mW
Derate for Case Temperature above +25°C ..... 16mW/°C
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Soldering: Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

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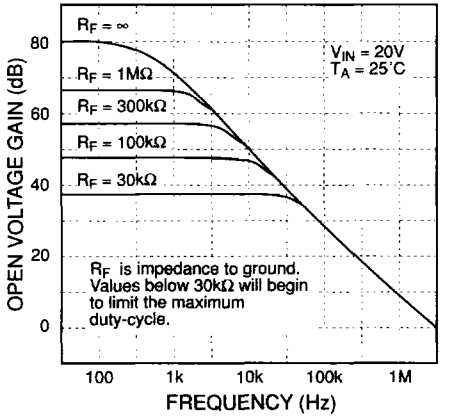
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Turn-on Characteristics					
Input Voltage	Operating range after Turn-on	8		40	V
Turn-on Threshold		**5.5**	**7.5**	**8.5**	**V**
Turn-on Current	V_{IN} Turn-on - 100mV		2.5	4.0	mA
Operating Current	**V_{IN}=8 to 40V**		**5**	**10**	**mA**
Turn-on Hysteresis*			0.6		V
■ Reference Section					
Output Voltage	T_A=25°C	4.90	5.00	5.20	V
Line Regulation	**V_{IN}=10 to 40V**		**10**	**30**	**mV**
Load Regulation	I_L=0 to 20mA		20	50	mA
Temperature Stability*	**Over Operating Range**		**20**	**50**	**mV**
Short Circuit Current	V_{REF}=0, TA=25°C		80	100	mA
Output Noise Voltage*	**10Hz≤f≤10kHz, T_A=25°C**		**40**		**μVrms**
Long Term Stability*	T_A=125°C; 1000 Hrs.		20	50	mV
■ Oscillator Section (Unless otherwise specified, R_T=2700Ω, C_T=0.01μF)					
Initial Accuracy	T_A=25°C	39	43	47	kHz
Temperature Stability*	**Over Operating Temperature Range**		**1**	**2**	**%**
Minimum Frequency	R_T=150kΩ, C_T=0.1μF			120	Hz
Maximum Frequency	**R_T=2.0kΩ, C_T=470pF**	**500**			**kHz**
Output Amplitude*	T_A=25°C		3.5		V
Output Pulse Width*	**T_A=25°C**		**0.5**		**μs**
Ramp Peak		3.3	3.5	3.7	V
Ramp Valley		**0.7**	**0.9**	**1.0**	**V**
■ Error Amplifier Section (Unless otherwise specified, VCM=2.5V)					
Input Offset Voltage			2	10	mV
Input Bias Current			**1**	**10**	**μA**
Input Offset Current			0.5	1.0	μA
Common Mode Rejection Ratio	**V_{CM}=1.5 to 5.5V**	**60**	**75**		**dB**
Power Supply Rejection Ratio	V_{IN}=10 to 40V	50	60		dB
Output Swing	**Minimum Total Range**	**0.5**		**5.0**	**V**

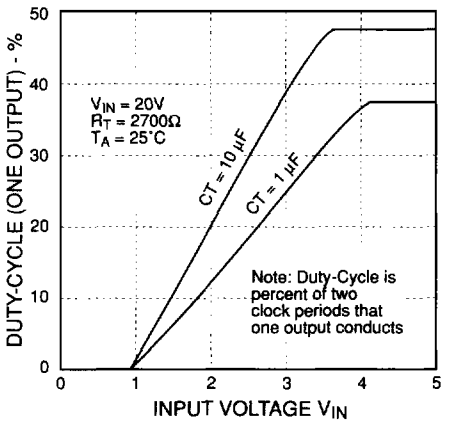
* These parameters are guaranteed by design but not 100% tested in production.

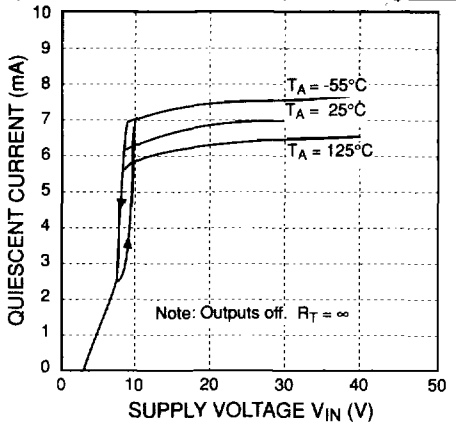
■ Error Amplifier Section (Unless otherwise specified, V_{CM}=2.5V): continued					
Open Loop Voltage Gain	$\Delta_{V_{OUT}}$=1 to 4V, $R_L \geq 10$ MΩ	60	80		dB
Gain Bandwidth*	T_A=25°C, A_V=0dB		3		MHz
■ Current Limit Amplifier (Unless otherwise specified, $V_{SENSE}=V_O$)					
Input Offset Voltage	T_A=25°C, EA Set for Max. Output	180	200	220	mV
Input Offset Voltage	Over Operating Temperature Range	170		250	mV
Input Bias Current			-1	-10	µA
Common Mode Rejection Ratio	V_{SENSE}=0 to 15V	50	60		dB
Power Supply Rejection Ratio	V_{IN}=10 to 40V	50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	V
Open Loop Voltage Gain	$\Delta_{V_{OUT}}$=1 to 4V, $R_L \geq 10$MΩ	70	80		dB
Delay Time*	ΔV_{IN}=300mV		300		ns
■ Output Section (Each Output)					
Collector Emitter Voltage	I_C=100µA	60	80		V
Collector Leakage Current	V_{CE}=50V		0.1	20.0	µA
Saturation	I_C=20mA		0.2	0.4	V
	I_C=200mA		1.0	2.2	V
Emitter Output Voltage	I_E=50mA	17	18		V
Rise Time*	T_A=25°C, R=2kΩ		200		ns
Fall Time*	T_A=25°C, R=2kΩ		100		ns
Comparator Delay*	T_A=25°C, V_{COMP} to V_{OUT}		300		ns
Shutdown Delay*	T_A=25°C, V_{SHUT} to V_{OUT}		200		ns
Shutdown Threshold	T_A=25°C, R_C=2kΩ	0.5	0.7	1.0	V
Thermal Shutdown*			165		°C

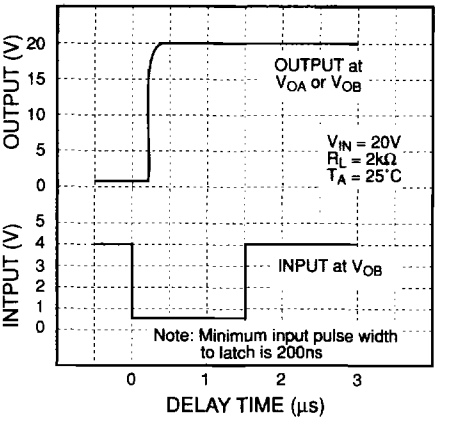
* These parameters are guaranteed by design but not 100% tested in production.

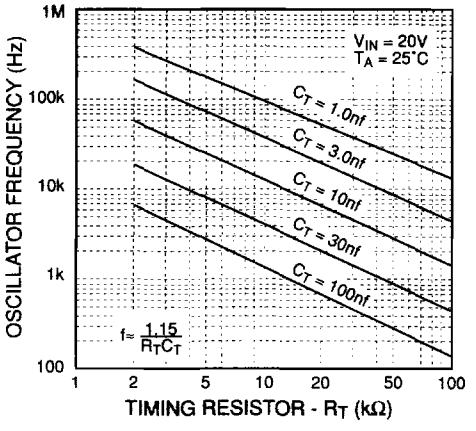
Typical Performance Characteristics

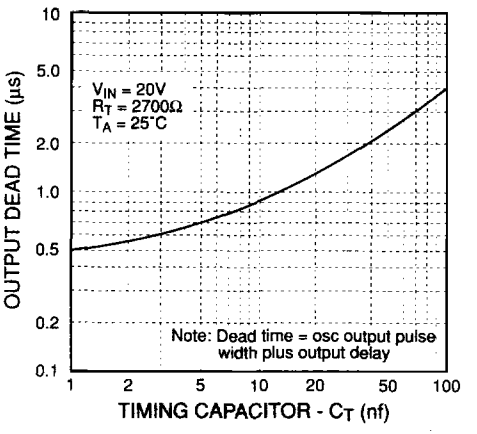


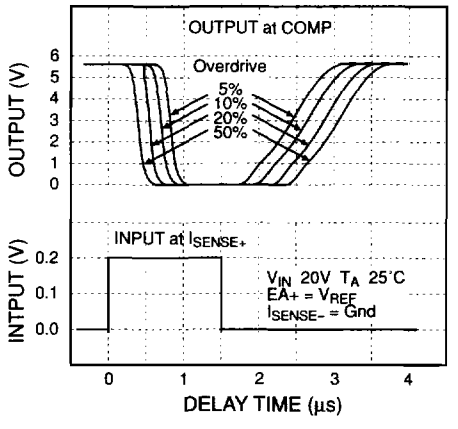


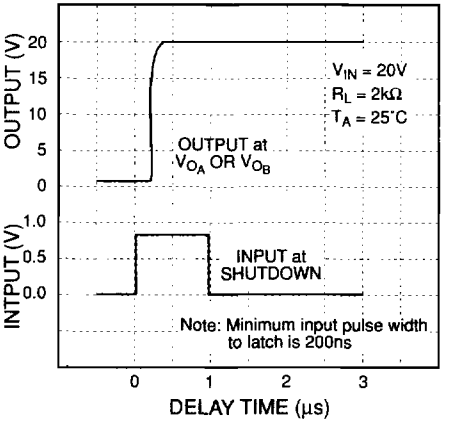

QUIESCENT CURRENT (mA)
SUPPLY VOLTAGE V_{IN} (V)
T_A = -55°C
T_A = 25°C
T_A = 125°C
Note: Outputs off. $R_T = \infty$

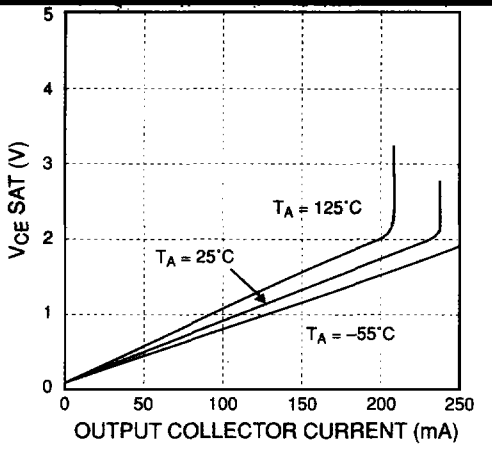

OUTPUT (V)
INTPUT (V)
DELAY TIME (µs)
OUTPUT at V_{OA} or V_{OB}
V_{IN} = 20V
R_L = 2kΩ
T_A = 25°C
INPUT at V_{OB}
Note: Minimum input pulse width to latch is 200ns

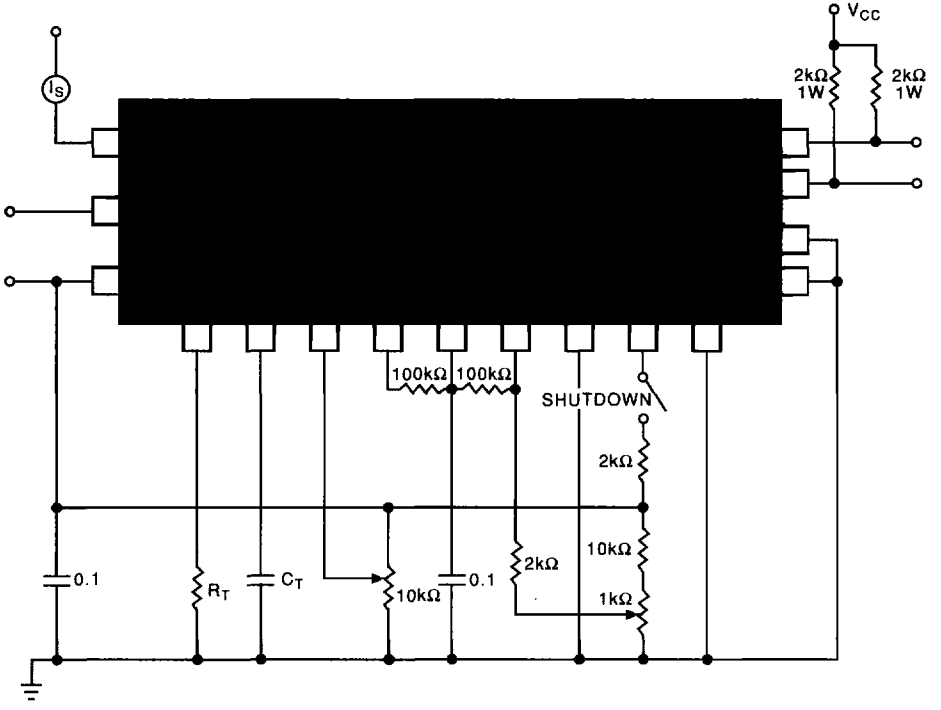

OSCILLATOR FREQUENCY (Hz)
TIMING RESISTOR - R_T (kΩ)
V_{IN} = 20V
T_A = 25°C
C_T = 1.0nf
C_T = 3.0nf
C_T = 10nf
C_T = 30nf
C_T = 100nf
$f \approx \frac{1.15}{R_T C_T}$


OUTPUT DEAD TIME (µs)
TIMING CAPACITOR - C_T (nf)
V_{IN} = 20V
R_T = 2700Ω
T_A = 25°C
Note: Dead time = osc output pulse width plus output delay


OUTPUT (V)
INTPUT (V)
DELAY TIME (µs)
OUTPUT at COMP
Overdrive
5%
10%
20%
50%
INPUT at I_{SENSE+}
V_{IN} 20V T_A 25°C
EA+ = V_{REF}
I_{SENSE-} = Gnd


OUTPUT (V)
INTPUT (V)
DELAY TIME (µs)
V_{IN} = 20V
R_L = 2kΩ
T_A = 25°C
OUTPUT at V_{O_A} OR V_{O_B}
INPUT at SHUTDOWN
Note: Minimum input pulse width to latch is 200ns



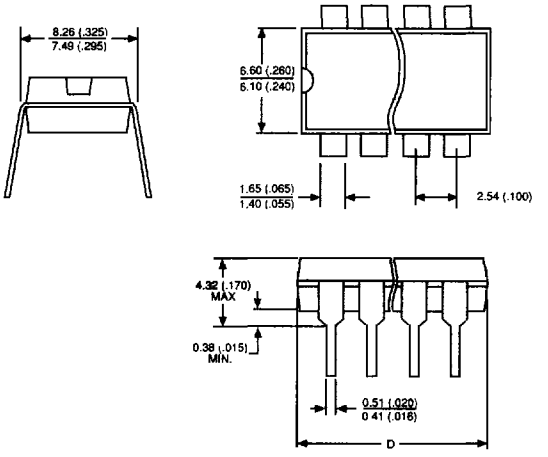


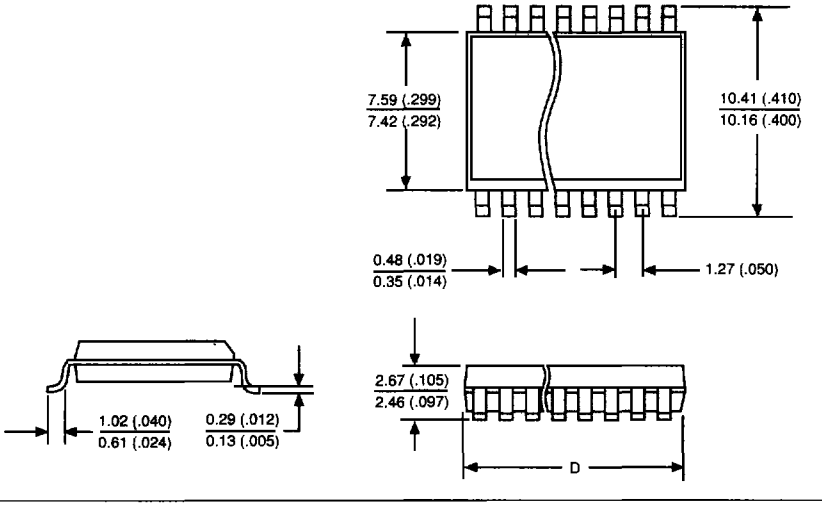
Note: The CS3524A should be able to be tested in any 3524 test circuit with two possible exceptions:

1. The higher gain-bandwidth of the current limit amplifier in the CS 3524A may cause oscillations in an uncompensated 3524 test circuit.
2. The effect of the shutdown, cannot be seen at the compensation terminal, but must be observed at the outputs.

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 Lead PDIP	19.94	19.15	.785	.754
16L SO Wide	10.46	10.21	.412	.402

Thermal Data		16 Lead PDIP	16L SO Wide	
$R_{\Theta JC}$	typ	42	23	°C/W
$R_{\Theta JA}$	typ	80	105	°C/W





Part Number	Description
CS-3524AN16	16 Lead PDIP
CS-3524ADW16	16 Lead SO Wide