# CMOS Quad 'D'-Type Flip-Flop

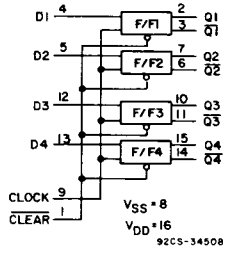
High-Voltage Types (20-Volt Rating)

**Features:**

- *100% tested for quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *Noise margin (full package-temperature range) =*
  *1 V at $V_{DD}$ = 5 V*
  *2 V at $V_{DD}$ = 10 V*
  *2.5 V at $V_{DD}$ = 15 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*
- *Output compatible with two HTL loads, two low power TTL loads, or one low power Schottky TTL load*
- *Functional equivalent to TTL 74175*
- *Standardized symmetrical output characteristics*

**Applications:**

- *Shift registers*
- *Buffer/storage registers*
- *Pattern generators*

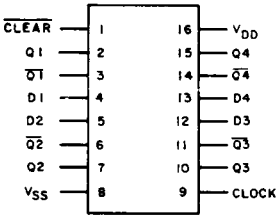



**CD40175B FUNCTION DIAGRAM**

■ CD40175B consists of four identical D-type flip-flops. Each flip-flop has an independent DATA D input and complementary Q and $\overline{Q}$ outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive-going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175B is supplied in hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).




$V_{DD}$ = PIN 16
$V_{SS}$ = PIN 8

92CS-34507

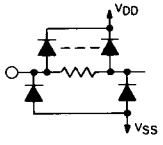
**TERMINAL ASSIGNMENT**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = 25°C, Except as Noted.**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | | $V_{DD}$ (V) | LIMITS MIN. | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | | — | 3 | 18 | V |
| Data Setup Time | $t_{SU}$ | 5 | 120 | — | ns |
| | | 10 | 50 | — | |
| | | 15 | 40 | — | |
| Data Hold Time | $t_H$ | 5 | 80 | — | ns |
| | | 10 | 40 | — | |
| | | 15 | 30 | — | |
| Clock Input Frequency | $f_{CL}$ | 5 | — | 2 | MHz |
| | | 10 | dc | 5 | |
| | | 15 | — | 6.5 | |
| Clock Input Rise or Fall Time | $t_{rCL}$, $t_{fCL}$ | 5 | — | 15 | μs |
| | | 10 | — | 15 | |
| | | 15 | — | 15 | |
| Clock Input Pulse Width | $t_{WL}$, $t_{WH}$ | 5 | 250 | — | ns |
| | | 10 | 100 | — | |
| | | 15 | 75 | — | |
| $\overline{\text{Clear}}$ Pulse Width | $t_{WL}$ | 5 | 200 | — | ns |
| | | 10 | 80 | — | |
| | | 15 | 60 | — | |
| $\overline{\text{Clear}}$ Removal Time | $t_{REM}$ | 5 | 250 | — | ns |
| | | 10 | 100 | — | |
| | | 15 | 80 | — | |




* Inputs Protected by CMOS Protection Network

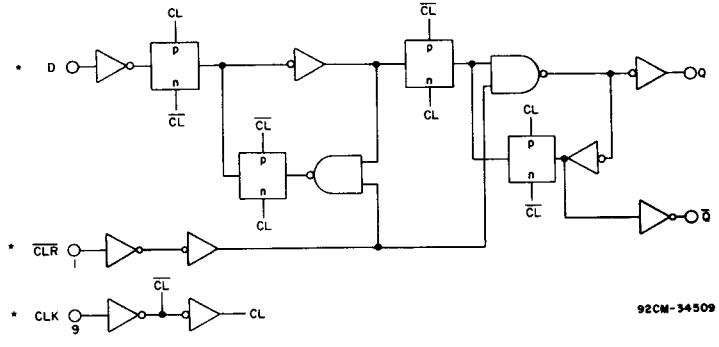



*Fig. 1 - Logic diagram (1 of 4 flip-flops).*

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | +25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent | — | 0, 5 | 5 | 1 | 1 | 30 | 30 | — | 0.02 | 1 | |
| Device | — | 0, 10 | 10 | 2 | 2 | 60 | 60 | — | 0.02 | 2 | |
| Current | — | 0, 15 | 15 | 4 | 4 | 120 | 120 | — | 0.02 | 4 | μA |
| Max. $I_{DD}$ | — | 0, 20 | 20 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| Output Low | 0.4 | 0, 5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | |
| (Sink) Current | 0.5 | 0, 10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| Min. $I_{OL}$ | 1.5 | 0, 15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High | 4.6 | 0, 5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA |
| (Source) | 2.5 | 0, 5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| Current | 9.5 | 0, 10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| Min. $I_{OH}$ | 13.5 | 0, 15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| Output Voltage: | — | 0, 5 | 5 | 0.05 | | | | — | 0 | 0.05 | |
| Low-Level | — | 0, 10 | 10 | 0.05 | | | | — | 0 | 0.05 | |
| Max. $V_{OL}$ | — | 0, 15 | 15 | 0.05 | | | | — | 0 | 0.05 | |
| Output Voltage: | — | 0, 5 | 5 | 4.95 | | | | 4.95 | 5 | — | V |
| High-Level | — | 0, 10 | 10 | 9.95 | | | | 9.95 | 10 | — | |
| Min. $V_{OH}$ | — | 0, 15 | 15 | 14.95 | | | | 14.95 | 15 | — | |
| Input Low | 0.5,4.5 | — | 5 | 1.5 | | | | — | — | 1.5 | |
| Voltage | 1, 9 | — | 10 | 3 | | | | — | — | 3 | |
| Max. $V_{IL}$ | 1.5,13.5 | — | 15 | 4 | | | | — | — | 4 | |
| Input High | 0.5,4.5 | — | 5 | 3.5 | | | | 3.5 | — | — | V |
| Voltage | 1, 9 | — | 10 | 7 | | | | 7 | — | — | |
| Min. $V_{IH}$ | 1.5,13.5 | — | 15 | 11 | | | | 11 | — | — | |
| Input Current Max. $I_{IN}$ | — | 0, 18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | $\pm 10^{-5}$ | ±0.1 | μA |

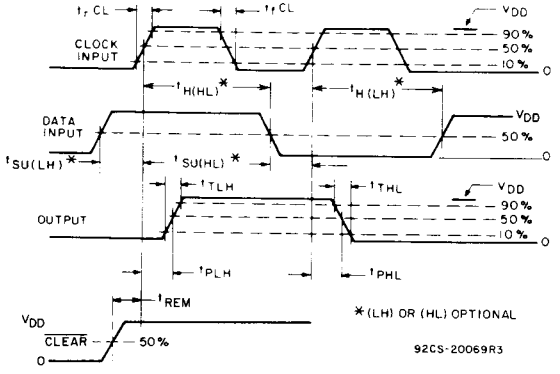



*Fig. 2 - Definition of setup, hold, propagation delay, and removal times.*

**TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLOCK | DATA | $\overline{\text{CLEAR}}$ | Q | $\overline{Q}$ |
| ⌐ | 0 | 1 | 0 | 1 |
| ⌐ | 1 | 1 | 1 | 0 |
| ¬ | X | 1 | Q | $\overline{Q}$ |
| X | X | 0 | 0 | 1 |

1=High Level X=Don't Care 0=Low Level

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = 25° C; Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ**

| CHARACTERISTIC | | TEST CONDITIONS $V_{DD}$ (V) | LIMITS MIN. | LIMITS TYP. | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|---|
| Transition Time | tTHL, tTLH | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Propagation Delay Time Clock to Q Output | tPHL, tPLH | 5 | — | 220 | 400 | |
| | | 10 | — | 90 | 160 | |
| | | 15 | — | 70 | 120 | |
| Propagation Delay Time $\overline{\text{CLEAR}}$ to Q Output | tPHL | 5 | — | 325 | 500 | |
| | | 10 | — | 130 | 200 | |
| | | 15 | — | 100 | 150 | |
| Minimum Pulse Width Clock | tWH | 5 | — | 110 | 250 | |
| | | 10 | — | 45 | 100 | |
| | | 15 | — | 35 | 75 | |
| $\overline{\text{Clear}}$ | tWL | 5 | — | 100 | 200 | |
| | | 10 | — | 40 | 80 | |
| | | 15 | — | 30 | 60 | |
| Maximum Clock Frequency | fCL | 5 | 2 | 4.5 | — | MHz |
| | | 10 | 5 | 11 | — | |
| | | 15 | 6.5 | 14 | — | |
| Maximum Clock Rise or Fall Time | trCL, tfCL | 5 | 15 | — | — | μs |
| | | 10 | 15 | — | — | |
| | | 15 | 15 | — | — | |
| Minimum Data Setup Time | tSU | 5 | — | 60 | 120 | ns |
| | | 10 | — | 25 | 50 | |
| | | 15 | — | 20 | 40 | |
| Minimum Data Hold Time | tH | 5 | — | 40 | 80 | |
| | | 10 | — | 20 | 40 | |
| | | 15 | — | 15 | 30 | |
| Minimum $\overline{\text{Clear}}$ Removal Time ‡ | tREM | 5 | — | 125 | 250 | |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Input Capacitance | CIN | — | — | 5 | 7.5 | pF |

‡ $\overline{\text{CLEAR}}$ signal must be high prior to positive-going transition of CLOCK pulse.

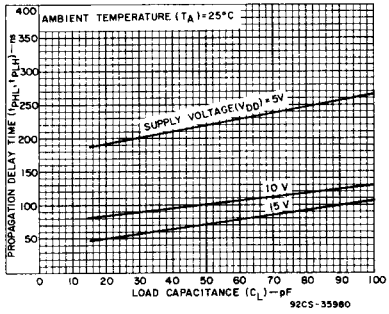



*Fig. 3 - Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.*

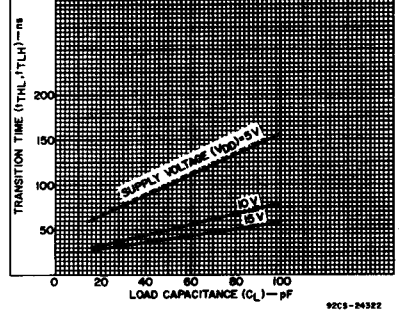



*Fig. 4 - Typical transition time as a function of load capacitance.*

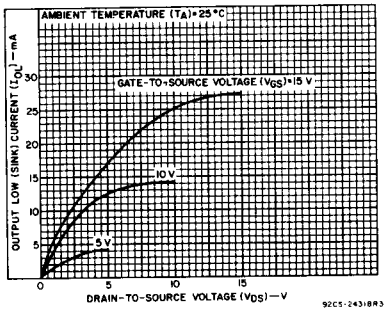



*Fig. 5 – Typical output low (sink) current characteristics.*

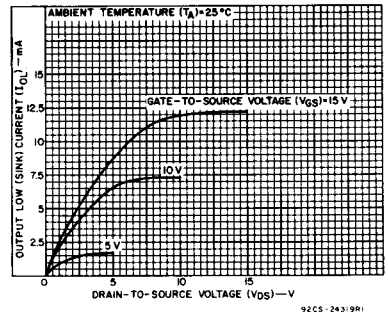



*Fig. 6 – Minimum output low (sink) current characteristics.*

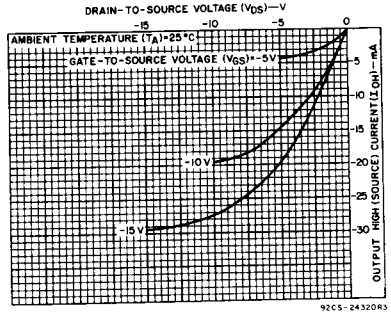



*Fig. 7 – Typical output high (source) current characteristics.*

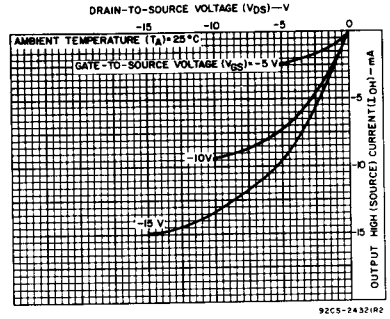



*Fig. 8 – Minimum output high (source) current characteristics.*

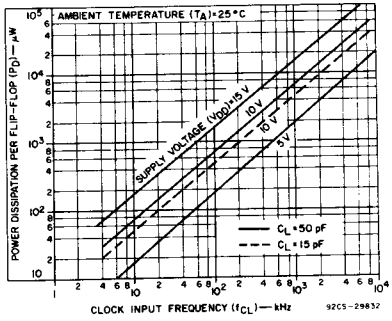



*Fig. 9 – Typical dynamic power dissipation as a function of CLOCK frequency.*

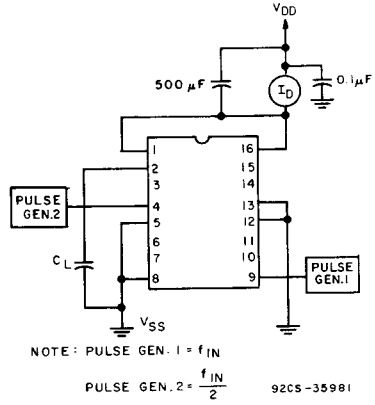



*Fig. 10 – Dynamic power dissipation test circuit.*

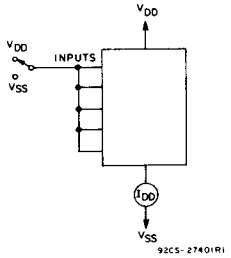



Fig. 11 - Quiescent device current test circuit.

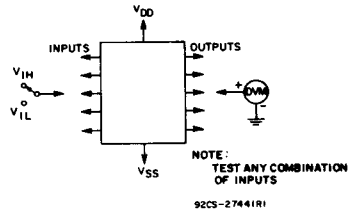



Fig. 12 - Noise immunity test circuit.

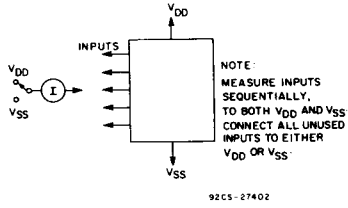
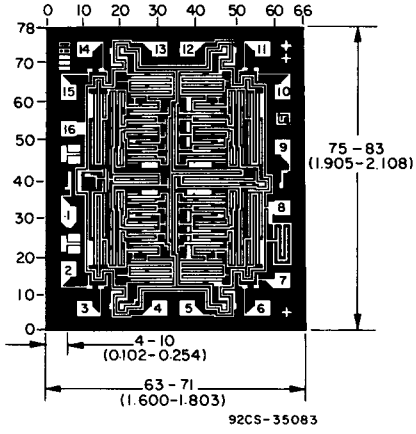



Fig. 13 - Input leakage current test circuit.




*Dimensions and pad layout for CD40175BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*