National Semiconductor

ADVANCE INFORMATION

74LCX109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear with 5V Tolerant Inputs

General Description

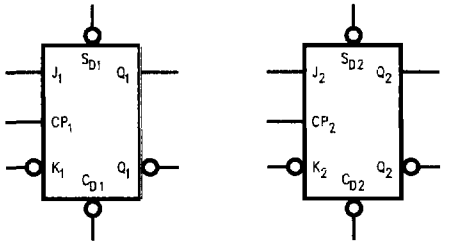
The 74LCX109 are dual J-$\overline{K}$ flip-flops. Each flip-flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q, $\overline{Q}$ outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX109 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs
- 7.0 ns tpd max, 10 μA I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 109
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Logic Symbols



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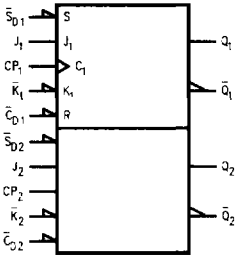
IEEE/IEC



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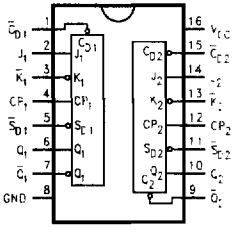
Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Information	74LCX109M 74LCX109MX	74LCX109SJ 74LCX109SJX	74LCX109MTC 74LCX109MTCX
See NS Package Number	M16A	M16D	MTC16

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