FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT74FCT2240AT/CT

FEATURES:

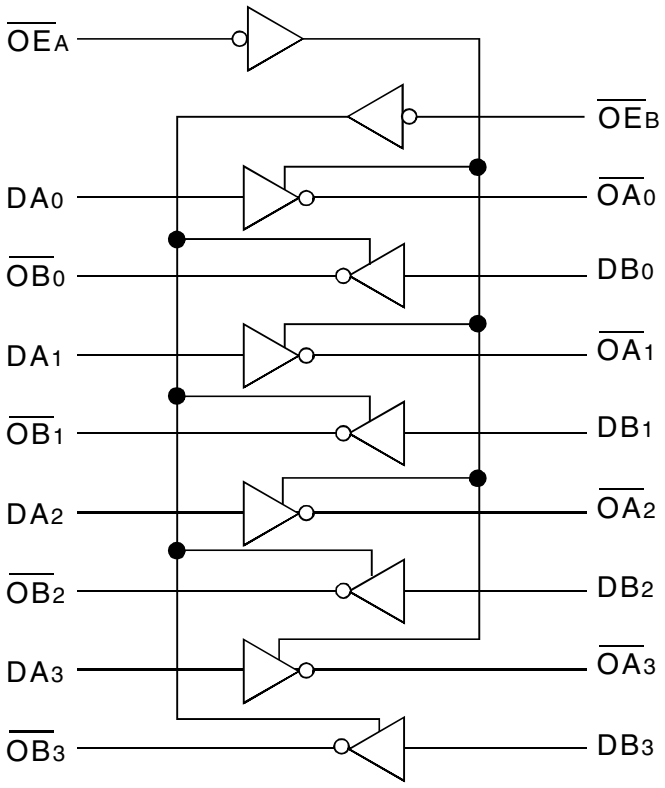
- **A and C grades**
- **Low input and output leakage ≤1µA (max.)**
- **CMOS power levels**
- **True TTL input and output compatibility:**
  - *V_{OH} = 3.3V (typ.)*
  - *V_{OL} = 0.3V (typ.)*
- **Meets or exceeds JEDEC standard 18 specifications**
- **Resistor outputs (-15mA I_{OH}, 12mA I_{OL})**
- **Reduced system switching noise**
- **Available in SOIC and QSOP packages**

DESCRIPTION:

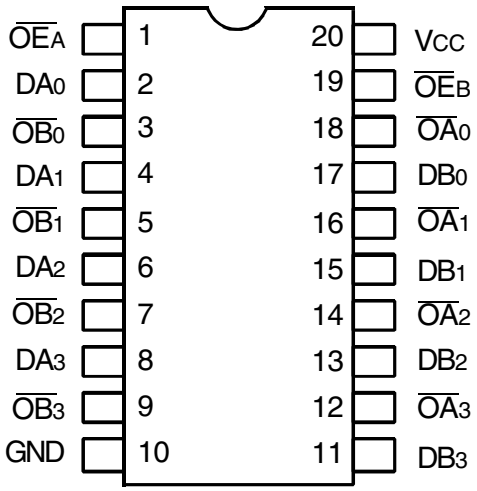
The IDT octal buffer/line driver is built using an advanced dual metal CMOS technology. The FCT2240T is designed to be employed as a memory and address driver, clock driver, and bus-oriented transmitter/receiver which provides improved board density.

The FCT2240T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors. The FCT2240T is a plug-in replacement for the FCT240T.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
Dxx	Inputs
$\overline{O}$xx	Outputs

FUNCTION TABLE(1)

Inputs			Outputs
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output Pins)		V_I = 0.5V	—	—	±1	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		-16	-48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.5	V

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	2.2	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	3.2	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Four Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	3.4[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	3.2	11.4[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Output Frequency
   N_i = Number of Outputs at f_i

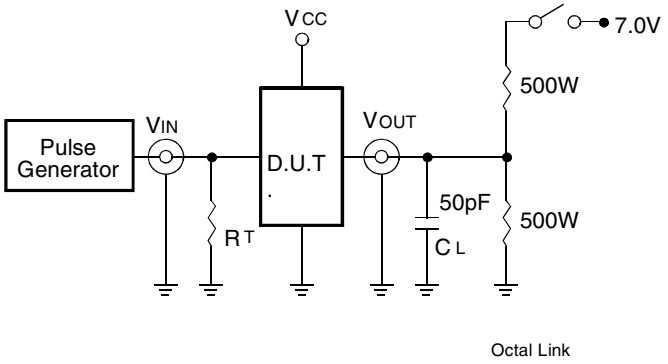
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT2240AT		FCT2240CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Dx to $\overline{Ox}$	C_L = 50pF R_L = 500Ω	1.5	4.8	1.5	4.3	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.6	1.5	5.2	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



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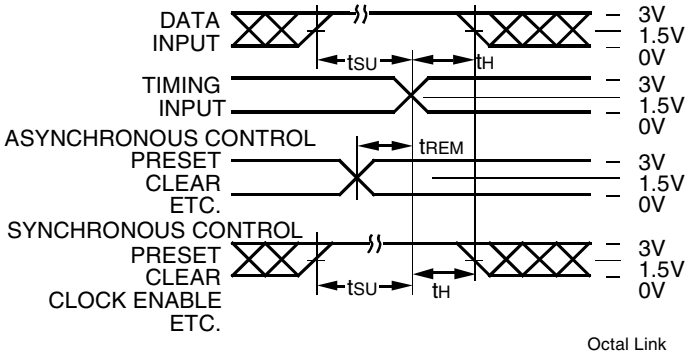
Test Circuits for All Outputs



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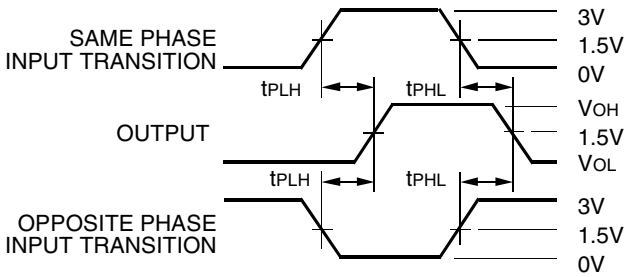
Set-Up, Hold, and Release Times



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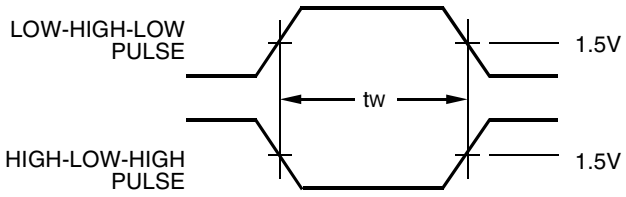
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

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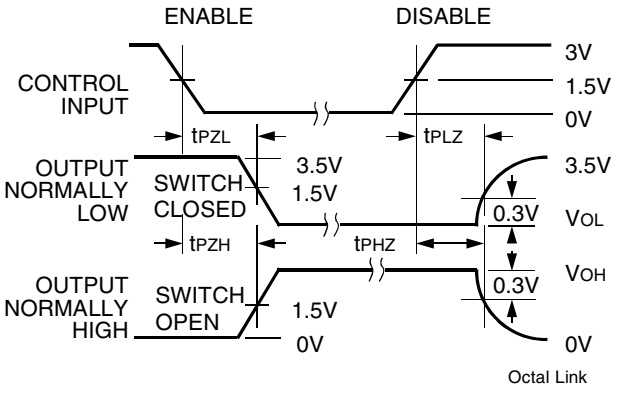

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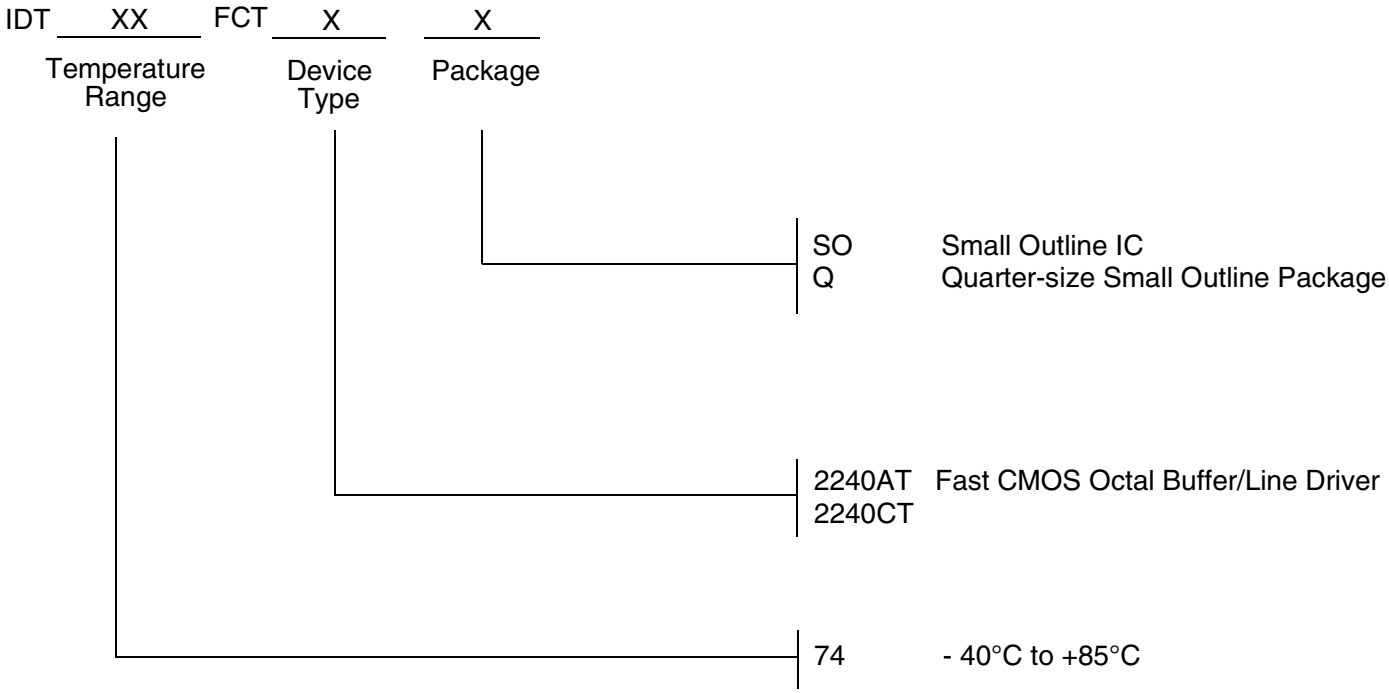
Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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