QUALITY SEMICONDUCTOR, INC.

Low Skew CMOS PLL Clock Driver With Integrated Loop Filter

FEATURES

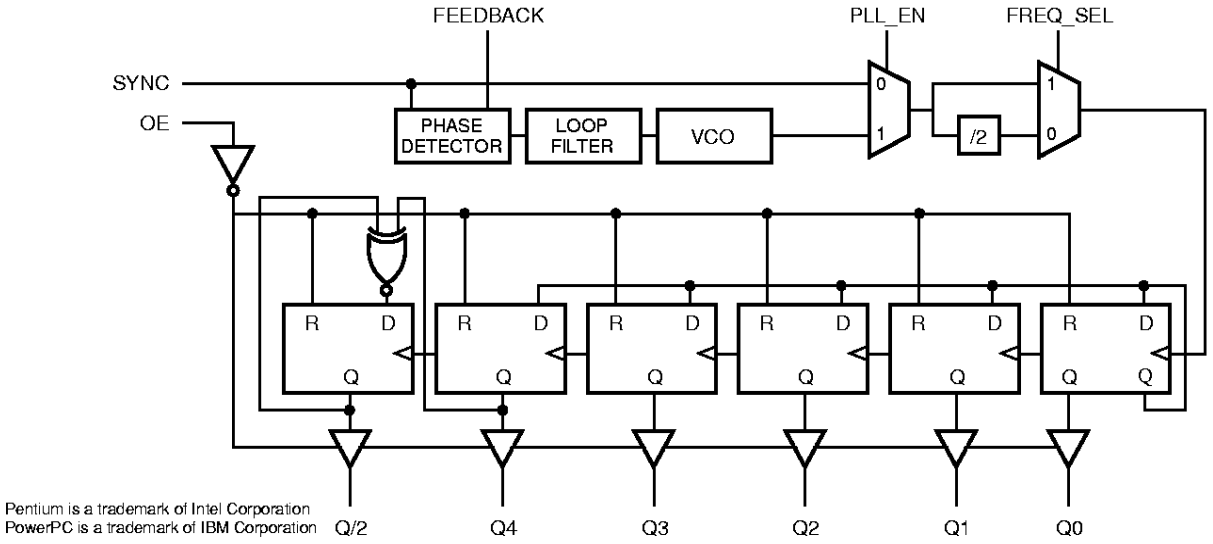
- Q/2 output, 5 Q outputs
- Useful for Pentium, PowerPC, PCI systems
- Internal loop filter RC network
- Low noise TTL level outputs
- < 250ps rising edge output skew
- Balanced Drive Outputs ± 24mA
- PLL bypass feature for low frequency testing
- Internal VCO/2 option for wider frequency range
- Outputs tri-state and reset while OE LOW
- Space saving 20-pin QSOP(Q)
- ESD > 2000V
- Latch-up > –300mA

DESCRIPTION

The QS5930 Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to a reference clock input. Six outputs are available: Q4-Q0, and Q/2. Careful layout and design insures less than 250ps skew between outputs. The QS5930 includes an internal RC loop filter to eliminate the need for external components, and TTL level output signals for lower noise. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The VCO can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The QS5930 is designed for use in cost sensitive high-performance computing systems such as Pentium™, PowerPC™, PCI and other high performance applications. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. In the QSOP package, the QS5930 clock driver represents the best value in small form factor, high-performance clock management products.

For more information on PLL clock driver products, see Application Note AN-22A.

Figure 1. Functional Block Diagram



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PowerPC is a trademark of IBM Corporation

Figure 2. Pin Configuration (All Pins Top View)

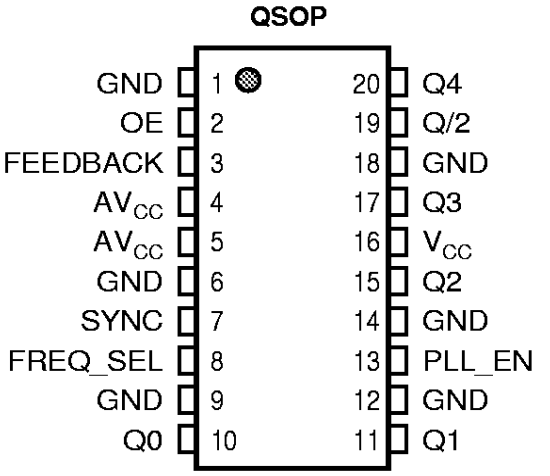


Table 1. Pin Descriptions

Pin Name	I/O	Functional Description
SYNC	I	Reference clock input
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency. HIGH is for higher frequencies, LOW is for lower frequencies.
FEEDBACK	I	PLL feedback input which is connected to either a Q or a Q/2 output. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q4-Q0	O	Clock outputs
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
OE	I	Output enable. When HIGH, outputs are active (normal operation). When LOW, all outputs are held in a tri-stated condition and output registers are reset.
PLL_EN	I	PLL enable. PLL is enabled when HIGH (normal operation), and disabled when LOW (allows the SYNC input to be single-stepped for system debug).

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
Maximum Power Dissipation	1.0 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Output Frequency Specifications

Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%.

Symbol	Description	–50	–66	Units
FQ	Maximum frequency, Q4-Q0	50	66.6	MHz
FQ/2	Maximum frequency, Q/2 output	25	33.3	MHz

Table 4. Frequency Selection Table

FREQ_SEL	Output Used for Feedback	Allowable SYNC[1] Range (MHz) Min	Max	Output Frequency Relationships Q Outputs	Q/2
1	Q/2	5	FQ ÷ 2	SYNC x 2	SYNC
1	Q4-Q0	10	FQ	SYNC	SYNC ÷ 2
0	Q/2	2.5	FQ ÷ 4	SYNC x 2	SYNC
0	Q4-Q0	5	FQ ÷ 2	SYNC	SYNC ÷ 2

Note:
1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in optimal range of 20MHz to 150MHz. Operation with SYNC input outside specified frequency ranges may result in invalid or out-of-lock outputs. FREQ_SEL only affects VCO frequency and does not affect output frequencies.

Table 5. Capacitance

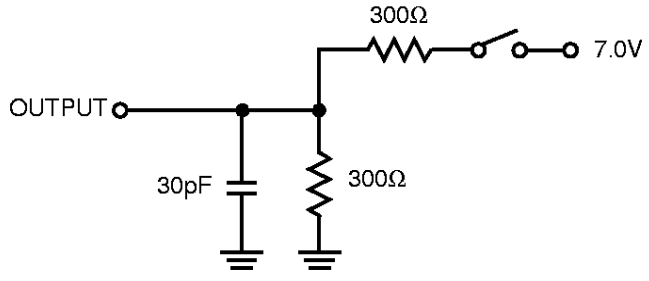
T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	QSOP Typ	Max	Unit
C_{IN}	3	4	pF
C_{OUT}	7	9	pF

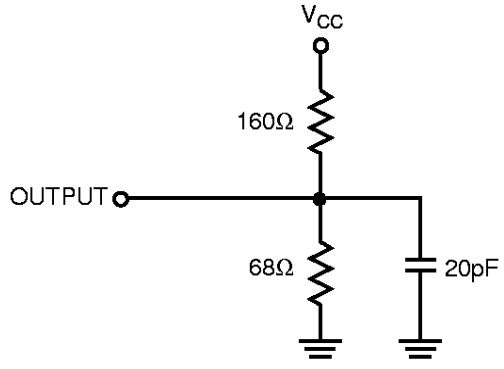
Note: Capacitance is characterized but not tested.

Figure 3. Test Load

Test Circuit 1 is used for output enable/disable parameters.
Test Circuit 2 is used for all other timing parameters.



Test Circuit 1



Test Circuit 2

Table 6. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	—	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –24mA	2.4	—	V
		V_{CC} = Min., I_{OH} = –100µA	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 24mA	—	0.55	V
		V_{CC} = Min., I_{OL} = 100µA	—	0.2	V
$\|I_{OZ}\|$	Output Leakage Current	V_{OUT} = V_{CC} or V_{OUT} = GND, V_{CC} = Max.	—	5	µA
$\|I_{IN}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = V_{CC} or V_{IN} = GND	—	5	µA

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]	Typ.	Max	Unit
ΔI_{CC}	Input Power Supply Current per TTL Input HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V	0.7	1.5	mA
I_{CCD}	Dynamic Power Supply Current per Output[3]	V_{CC} = Max.	—	0.1	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. This specification does not apply to the PLL_EN input.
3. Guaranteed but not tested.
4. For all DC parameters, test conditions also assume no output loading.

Table 8. Input Timing Requirements

Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Description[1]	QS5930 Min	QS5930 Max	Unit
t_R, t_F	Maximum Input Rise and Fall Times, 0.8V to 2.0V	—	3.0	ns
F_I	Input Clock Frequency, SYNC[3]	5	F_Q	MHz
t_{PWC}	Input Clock Pulse, HIGH or LOW	2	—	ns
D_H	Duty Cycle, SYNC	25%	75%	%

Table 9. Switching Characteristics Over Operating Range

Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Description[1]	QS5930 Min	QS5930 Max	Unit
t_{SKR}	Output Skew Between Rising Edges, Q4-Q0 and Q/2[2,4]	—	250	ps
t_{SKF}	Output Skew Between Falling Edges, Q4-Q0[2,4]	—	350	ps
t_{PW}	Pulse Width[2]	T_{CY}/2 –0.5	T_{CY}/2 +0.5	ns
t_J	Cycle to Cycle Jitter, F_I > 33MHz[6]	—	250	ps
t_{PD}	SYNC Input Feedback Delay, 10MHz	–100	400	ps
t_{PD}	SYNC Input Feedback Delay, 33MHz, 50Ω to 1.5V[2]	–100	400	ps
t_{LOCK}	SYNC to Phase Lock[2]	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, OE LOW to HIGH[5]	0	7	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OE HIGH to LOW[2,5]	0	6	ns
t_R, t_F	Output Rise and Fall Times, 0.8V to 2.0V[2]	0.4	1.5	ns

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The F_I specification is based on Q output feedback. See FREQUENCY SELECTION TABLE for more detail on allowable SYNC input frequencies for different feedback combinations.
4. Skew specifications apply under identical environments (loading, temperature, V_{CC}, device speed grade).
5. Measured in open loop mode PLL_EN = 0.
6. Jitter is characterized using a digital oscilloscope. Jitter is characterized but not tested. See FREQUENCY SELECTION TABLE for information on proper FREQ_SEL level for specified SYNC input frequencies.