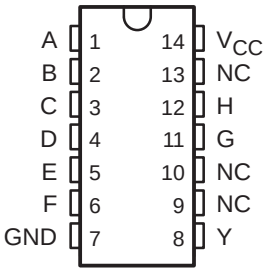
description

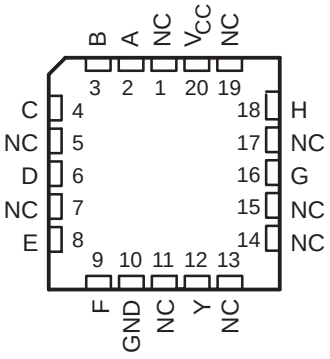
These devices contain an 8-input positive-NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H} \text{ or}$$
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . D OR N PACKAGE
SN74AS30 . . . DB PACKAGE
(TOP VIEW)



SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

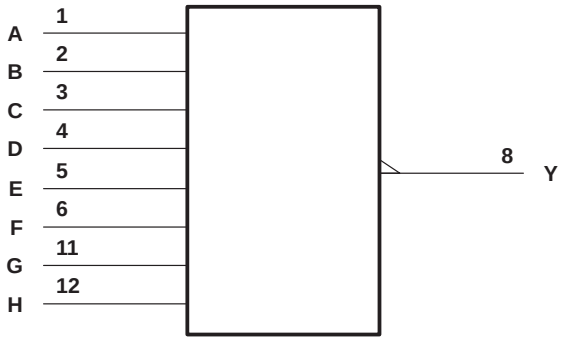
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS30AN	SN74ALS30AN
			SN74AS30N	SN74AS30N
	SOIC – D	Tube	SN74ALS30AD	ALS30A
		Tape and reel	SN74ALS30AD	
		Tube	SN74AS30D	AS30
		Tape and reel	SN74AS30D	
	SSOP – DB	Tape and reel	SN74AS30DBR	AS30
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS30AJ	SNJ54ALS30AJ
			SNJ54AS30J	SNJ54AS30J
	LCCC – FK	Tube	SNJ54ALS30AFK	SNJ54ALS30AFK
			SNJ54AS30FK	SNJ54AS30FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

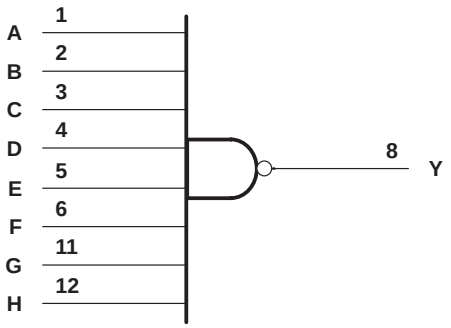
INPUTS A–H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8†	V
					0.7‡	
I_{OH}	High-level output current	’ALS30A			–0.4	mA
		’AS30			–2	
I_{OL}	Low-level output current	SN54ALS30A			4	mA
		SN74ALS30A			8	
		’AS30			20	
T_A	Operating free-air temperature	SN54ALS30A	–55		125	°C
		SN54AS30	–55		125	
		SN74ALS30A	0		70	
		SN74AS30	0		70	

† Applies to the ’AS30 and SN74ALS30A across the full operating temperature range, and SN54ALS30A over the temperature range of –55°C to 70°C.
‡ Applies to the SN54ALS30A over the temperature range of 70°C to 125°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

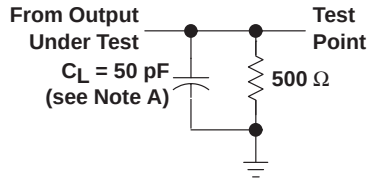
PARAMETER	TEST CONDITIONS			MIN	TYP§	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA	’ALS30A			–1.5	V
			’AS30			–1.2	
V_{OH}	V_{CC} = 4.5 V to 5.5 V	I_{OH} = –0.4 mA	’ALS30A	V_{CC}–2			V
		I_{OH} = –2 mA	’AS30	V_{CC}–2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA	’ALS30A		0.25	0.4	V
		I_{OL} = 8 mA	SN74ALS30A		0.35	0.5	
		I_{OL} = 20 mA	’AS30		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V	’ALS30A			–0.1	mA
			’AS30			–0.5	
I_O¶	V_{CC} = 5.5 V,	V_O = 2.25 V	SN54ALS30A	–20		–112	mA
			SN74ALS30A	–30		–112	
			’AS30	–30		–112	
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0	’ALS30A		0.22	0.36	mA
			’AS30		0.9	1.5	
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V	’ALS30A		0.54	0.9	mA
			’AS30		3	4.9	

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

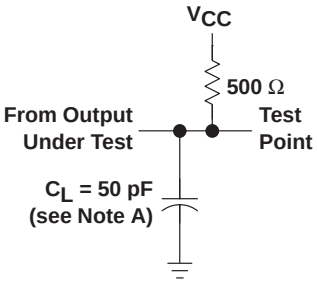
switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
t_{PLH}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	10	
			SN54AS30	1	5.5	
			SN74AS30	1	5	
t_{PHL}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	12	
			SN54AS30	1	5	
			SN74AS30	1	4.5	

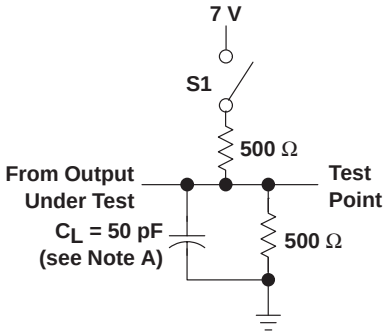
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



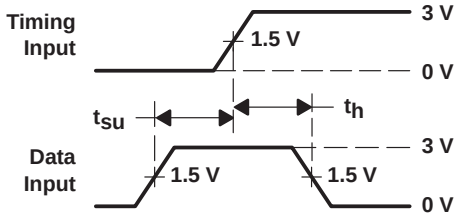
LOAD CIRCUIT FOR
BI-STATE TOTEM-POLE OUTPUTS



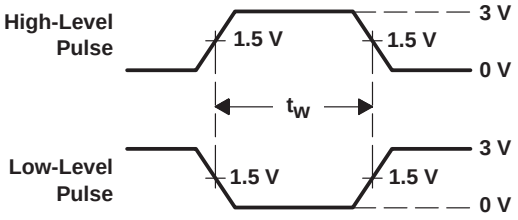
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



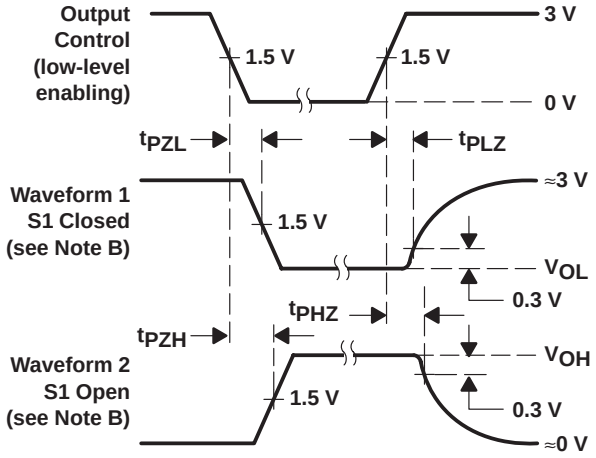
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



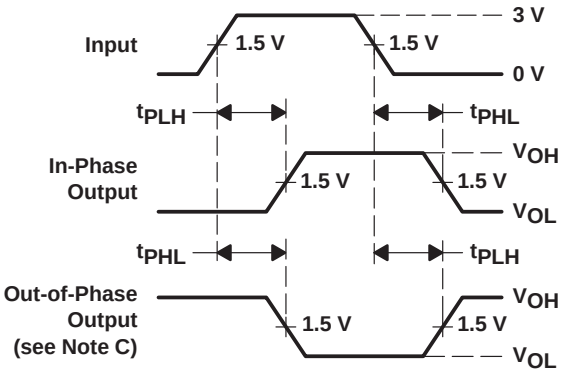
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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