

SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS036D – APRIL 1982 – REVISED AUGUST 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

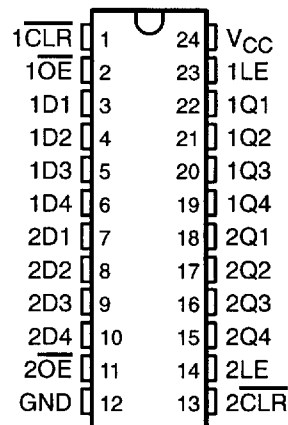
description

These dual 4-bit D-type latches feature 3-state outputs designed specifically for bus driving. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

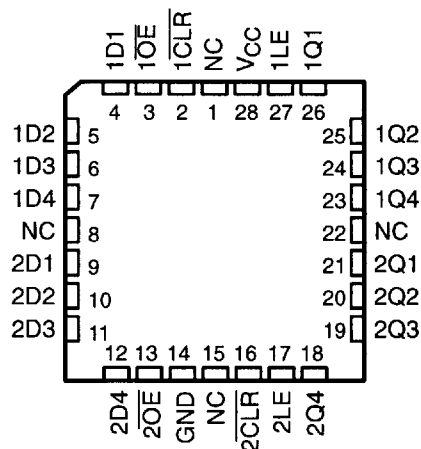
The dual 4-bit latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs in true form, according to the function table. When LE is low, the outputs are latched. When the clear ($\overline{\text{CLR}}$) input goes low, the Q outputs go low independently of LE. The outputs are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is at a high logic level.

The SN54ALS873B and SN54AS873A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS873B and SN74AS873A are characterized for operation from 0°C to 70°C .

SN54ALS873B, SN54AS873A . . . JT PACKAGE
SN74ALS873B, SN74AS873A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS873B, SN54AS873A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each latch)

| INPUTS | | | | OUTPUT Q |
|------------------------|-------------------------|----|---|-------------|
| $\overline{\text{OE}}$ | $\overline{\text{CLR}}$ | LE | D | |
| L | L | X | X | L |
| L | H | H | H | H |
| L | H | H | L | L |
| L | H | L | X | Q_0 |
| H | X | X | X | Z |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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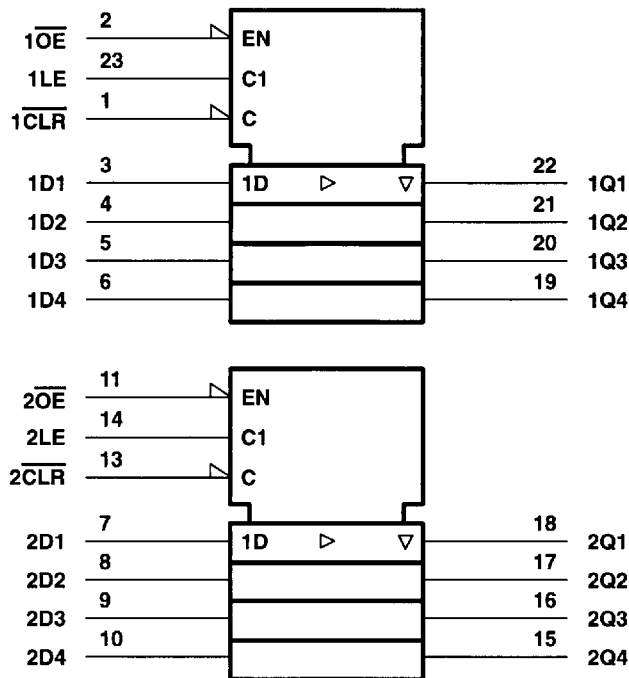
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DUAL 4-BIT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

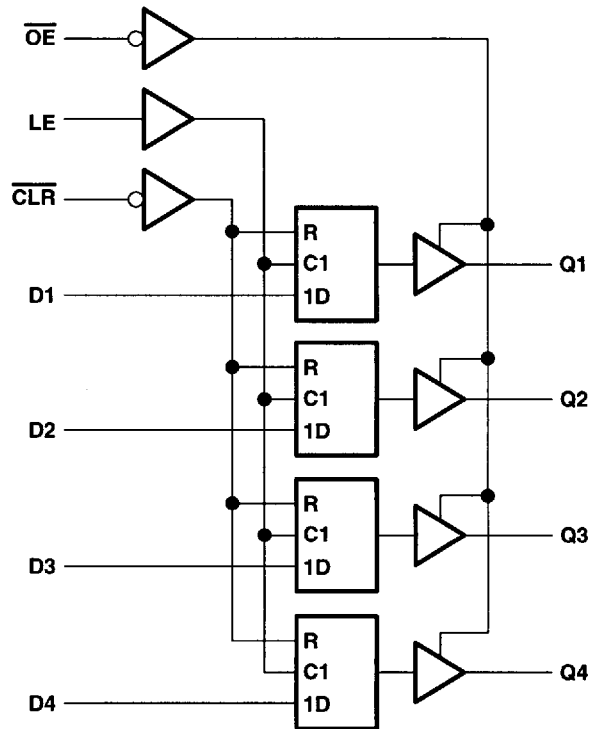
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range, T_A : SN54ALS873B | -55°C to 125°C |
| SN74ALS873B | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | SN54ALS873B | | | SN74ALS873B | | | UNIT |
|--------------------------------------|-------------|-----|-----|-------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} High-level output current | | | -1 | | | -2.6 | mA |
| I_{OL} Low-level output current | | | 12 | | | 24 | mA |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54ALS873B | | SN74ALS873B | | UNIT | | |
|-----------------|--|------------------|------|--------------|------|------|---------------|-----|
| | | MIN | TYP† | MAX | MIN | | TYP† | MAX |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | V | |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | $V_{CC} - 2$ | | V | | |
| | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$ | 2.4 | 3.3 | | | | | |
| | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -2.6\text{ mA}$ | | | 2.4 | 3.2 | | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$ | | 0.25 | 0.4 | 0.25 | 0.4 | V | |
| | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 24\text{ mA}$ | | | | 0.35 | 0.5 | | |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$ | | | 20 | | 20 | μA | |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$ | | | -20 | | -20 | μA | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | | 0.1 | mA | |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 20 | | 20 | μA | |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | -0.2 | | -0.2 | mA | |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | -20 | | -112 | -30 | -112 | mA | |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | | 11 | 21 | 11 | 21 | mA |
| | | Outputs low | | 16 | 29 | 16 | 29 | |
| | | Outputs disabled | | 20 | 31 | 20 | 31 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54ALS873B | | SN74ALS873B | | UNIT |
|----------|-----------------------------|-------------|-----|-------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | CLR low | 15 | | 15 | ns |
| | | LE high | 10 | | 10 | |
| t_{su} | Setup time, data before LE↓ | | 10 | | 10 | ns |
| t_h | Hold time, data after LE↓ | | 7 | | 7 | ns |



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DUAL 4-BIT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|--------------|-------------|--|-----|-------------|-----|------|
| | | | SN54ALS873B | | SN74ALS873B | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | Q | 2 | 23 | 2 | 14 | ns |
| t _{PHL} | | | 2 | 17 | 2 | 14 | |
| t _{PLH} | LE | Q | 8 | 31 | 8 | 22 | ns |
| t _{PHL} | | | 8 | 26 | 8 | 21 | |
| t _{PHL} | CLR | Q | 6 | 27 | 6 | 20 | ns |
| t _{PZH} | OE | Q | 4 | 24 | 4 | 18 | ns |
| t _{PZL} | | | 4 | 23 | 4 | 18 | |
| t _{PHZ} | OE | Q | 2 | 12 | 2 | 10 | ns |
| t _{PLZ} | | | 2 | 30 | 2 | 15 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ‡

| | |
|---|----------------|
| Supply voltage, V _{CC} | 7 V |
| Input voltage, V _I | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range, T _A : SN54AS873A | -55°C to 125°C |
| SN74AS873A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | SN54AS873A | | | SN74AS873A | | | UNIT |
|---|------------|-----|-----|------------|-----|-----|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} High-level output current | | | -12 | | | -15 | mA |
| I _{OL} Low-level output current | | | 32 | | | 48 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS873A | | SN74AS873A | | UNIT | |
|-----------------|--|------------------|------|--------------|------|------|---------------|
| | | MIN | TYP† | MAX | MIN | | TYP† |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | $V_{CC} - 2$ | | V | |
| | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$ | 2.4 | 3.2 | | | | |
| | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$ | | | 2.4 | 3.3 | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$ | | 0.25 | 0.5 | | V | |
| | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$ | | | | 0.35 | | 0.5 |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$ | | | 50 | | 50 | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$ | | | -50 | | -50 | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 20 | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | -0.5 | | -0.5 | mA |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | -30 | | -112 | -30 | -112 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | 68 | 110 | 68 | 110 | mA |
| | | Outputs low | 67 | 109 | 67 | 109 | |
| | | Outputs disabled | 80 | 129 | 80 | 129 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54AS873A | | SN74AS873A | | UNIT |
|------------|-----------------------------|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t_w^* | Pulse duration | CLR low | 5 | | 5 | ns |
| | | LE high | 6 | | 5 | |
| t_{su}^* | Setup time, data before LE↓ | | 2 | | 2 | ns |
| t_h^* | Hold time, data after LE↓ | | 4.5 | | 4.5 | ns |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|-------------------------|----------------|--|------|------------|------|------|
| | | | SN54AS873A | | SN74AS873A | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | Q | 3 | 12.5 | 3 | 9.5 | ns |
| t _{PHL} | | | 3 | 8.5 | 3 | 7.5 | |
| t _{PLH} | LE | Q | 6 | 15.5 | 6 | 13 | ns |
| t _{PHL} | | | 4 | 9 | 4 | 7.5 | |
| t _{PHL} | $\overline{\text{CLR}}$ | Q | 3 | 10.5 | 3 | 9 | ns |
| t _{PZH} | $\overline{\text{OE}}$ | Q | 2 | 8 | 2 | 6.5 | ns |
| t _{PZL} | | | 4 | 11 | 4 | 10.5 | |
| t _{PHZ} | $\overline{\text{OE}}$ | Q | 2 | 8 | 2 | 7.5 | ns |
| t _{PLZ} | | | 2 | 8.5 | 2 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

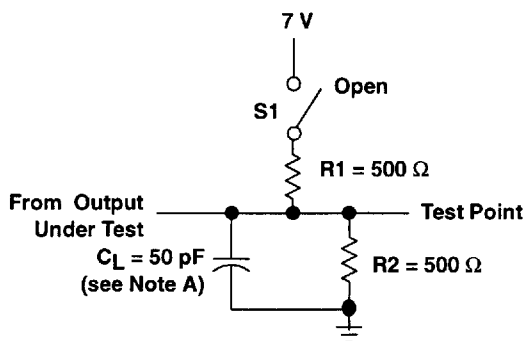


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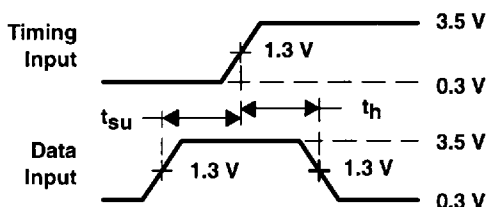
PARAMETER MEASUREMENT INFORMATION



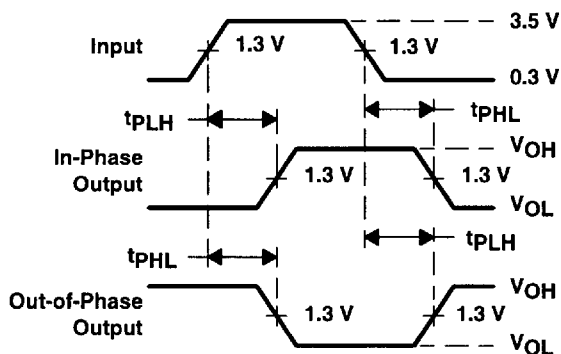
SWITCH POSITION TABLE

| TEST | S1 |
|-----------|--------|
| t_{PLH} | Open |
| t_{PHL} | Open |
| t_{PZH} | Open |
| t_{PZL} | Closed |
| t_{PHZ} | Open |
| t_{PLZ} | Closed |

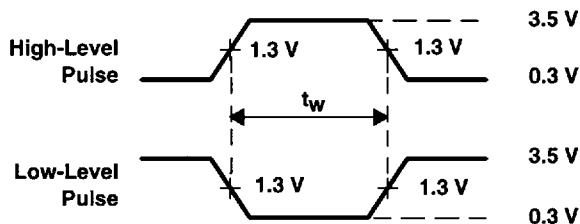
LOAD CIRCUIT FOR 3-STATE OUTPUTS



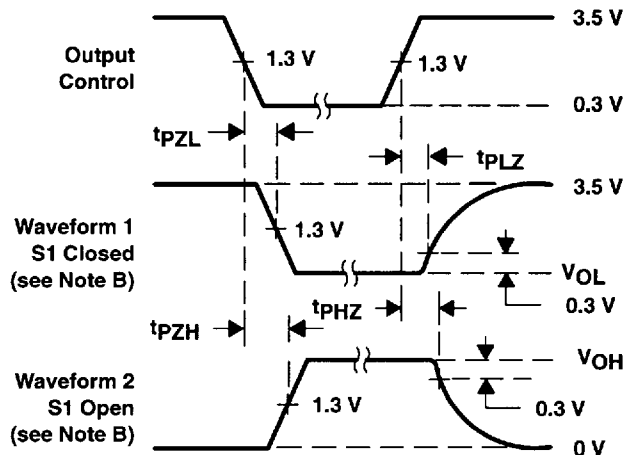
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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