

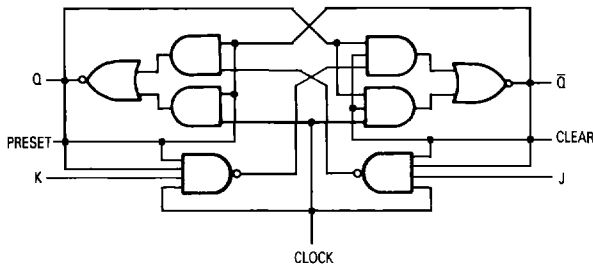


# Dual J-K Flip-Flop With Clear and Preset

ELECTRICALLY TESTED PER:  
MIL-M-38510/30110

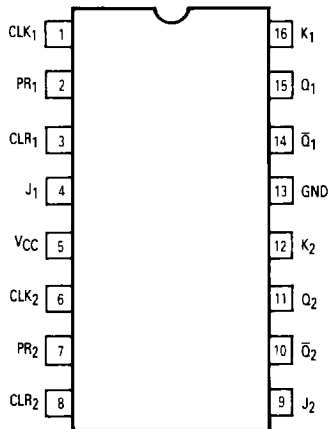
The 54LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH to LOW clock pulse.

LOGIC DIAGRAM  
(one half show)

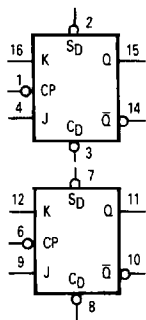


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAM



LOGIC SYMBOL



\*Both outputs will be HIGH while both  $\bar{S}_D$  and  $\bar{C}_D$  are LOW, but the output states are unpredictable if  $\bar{S}_D$  and  $\bar{C}_D$  go HIGH simultaneously.

H, h = HIGH Voltage Level  
L, l = LOW Voltage Level  
X = Don't Care  
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

Military 54LS76A



AVAILABLE AS:

- 1) JAN: JM38510/30110BXA
- 2) SMD: 7601301
- 3) 883C: 54LS76A/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: C

CERFLAT: D

LCC: SEE 54LS112A

\*Call Factory for latest update

## PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION A)
CLK <sub>1</sub>	1	1	VCC
PR <sub>1</sub>	2	2	GND
CLR <sub>1</sub>	3	3	GND
J <sub>1</sub>	4	4	VCC
VCC	5	5	VCC
CLK <sub>2</sub>	6	6	VCC
PR <sub>2</sub>	7	7	GND
CLR <sub>2</sub>	8	8	GND
J <sub>2</sub>	9	9	VCC
$\bar{Q}_2$	10	10	VCC
Q <sub>2</sub>	11	11	VCC
K <sub>2</sub>	12	12	VCC
GND	13	13	GND
$\bar{Q}_1$	14	14	VCC
Q <sub>1</sub>	15	15	VCC
K <sub>1</sub>	16	16	VCC

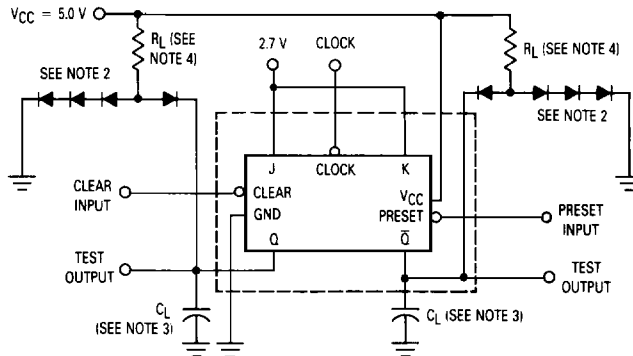
BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

## MODE SELECT — TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\bar{S}_D$	$\bar{C}_D$	J	K	Q	$\bar{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\bar{q}$

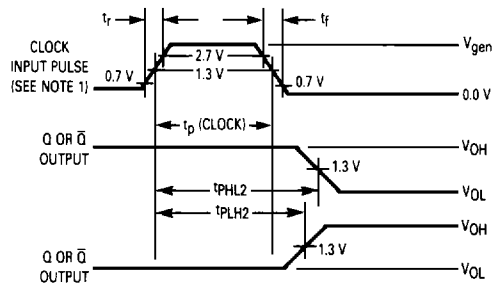
# 54LS76A

## AC TEST CIRCUIT



Synchronous Switching Test Circuit

## WAVEFORMS

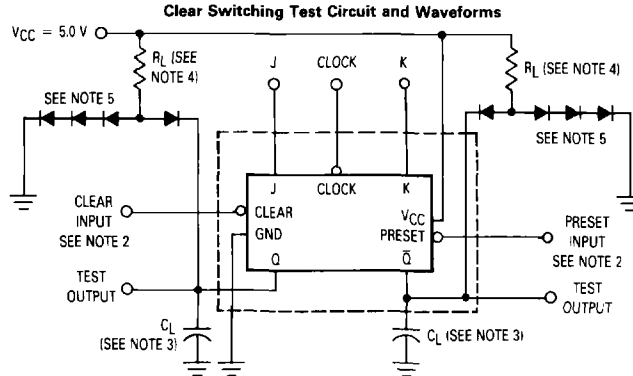


### NOTES:

1. Clock input characteristics for  $t_{PLH}$ ,  $t_{PHL}$  (clock to output):  
 $V_{gen} = 3.0\text{ V}$ ,  $t_r \approx 15\text{ ns}$ ,  $t_f \approx 6.0\text{ ns}$ ,  $t_p(\text{clock}) = 25\text{ ns}$  and  $PRR \approx 1.0\text{ MHz}$ . When testing  $f_{MAX}$  the clock input characteristics are:  $V_{gen} = 3.0\text{ V}$ ,  $t_r = t_f \approx 6.0\text{ ns}$ ,  $t_p(\text{clock}) \approx 20\text{ ns}$  and  $PRR = \text{see table 1}$ .
2. All diodes are 1N3064, or equivalent.
3.  $C_L = 50\text{ pF} \pm 10\%$  (including jig and probe capacitance).
4.  $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .

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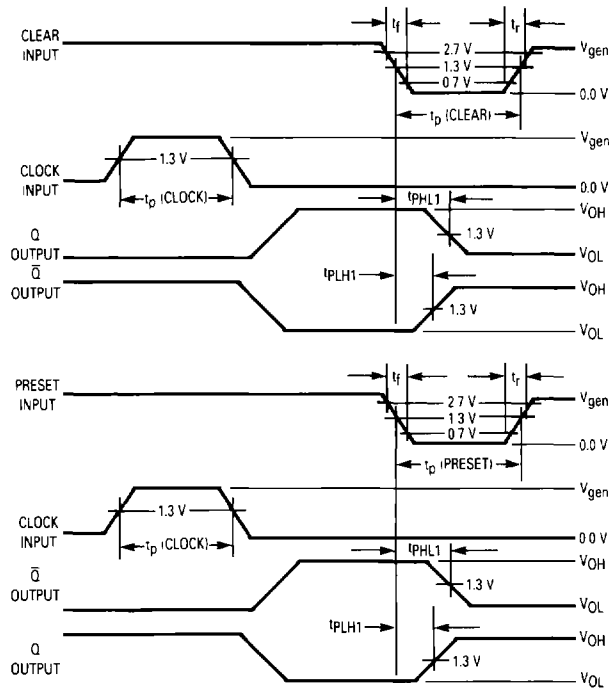
## AC TEST CIRCUIT



### NOTES:

1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics:  
 $V_{gen} = 3.0\text{ V}$ ,  $t_r \leq 15\text{ ns}$ ,  $t_f \leq 6.0\text{ ns}$ ,  $PRR \leq 1.0\text{ MHz}$ ,  
 $t_p(\text{clear}) = t_p(\text{preset}) = 30\text{ ns}$ ,  $Z_{out} \approx 50\ \Omega$ .
3.  $C_L = 50\text{ pF} \pm 10\%$  (including jig and probe capacitance).
4.  $R_L = 2.0\text{ k}\Omega \pm 5.0\%$ .
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table 1).
7. Clock input pulse characteristics:  
 $t_p(\text{clock}) \geq 25\text{ ns}$ ,  $V_{gen} = 3.0\text{ V}$ ,  $PRR \leq 1.0\text{ MHz}$ .



## WAVEFORMS



### 54LS76A

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -0.4 mA, V <sub>IN</sub> = 2.0 V, V <sub>IL</sub> = 0.7 V.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.7 V.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH1</sub>	Logical "1" Input Current (J & K inputs)		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, PR & K = 4.5 V, CLK & CLR = 0 V.
I <sub>IHH1</sub>	Logical "1" Input Current (J & K inputs)		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, CLR & J = 4.5 V, CLK & PR = 0 V.
I <sub>IH2</sub>	Logical "1" Input Current (CLR & PR)		60		60		60	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, K = 4.5 V, CLK & CLR = GND, PR = (See Note 2).
I <sub>IHH2</sub>	Logical "1" Input Current (CLR & PR)		300		300		300	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, J = 4.5 V, CLK & K = GND, CLR = (See Note 2).
I <sub>IH3</sub>	Logical "1" Input Current (CLK inputs)		80		80		80	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs = GND.
I <sub>IHH3</sub>	Logical "1" Input Current (CLK inputs)		400		400		400	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 5.5 V, other inputs = GND.
I <sub>IL1</sub>	Logical "0" Input Current (J & K inputs)	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, CLK - CLR & J = 4.5 V, PR = (See Note 2).
I <sub>IL2</sub>	Logical "0" Input Current (CLK & inputs)	-0.24	-0.72	-0.24	-0.72	-0.24	-0.72	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, PR - J & K = 4.5 V, CLR = (See Note 2).
I <sub>IL3</sub>	Logical "0" Input Current (PR inputs)	-0.12	-0.72	-0.12	-0.72	-0.12	-0.72	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V, other inputs = 4.5 V.
I <sub>OS</sub>	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, other inputs = GND, V <sub>OUT</sub> = 0 V.
I <sub>CC</sub>	Power Supply Current		8.0		8.0		8.0	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V, or V <sub>IN</sub> = 5.5 V, other inputs = GND.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.4 V, and V <sub>INH</sub> = 2.5 V.

**NOTES:**

1.  2.5 V min/5.5 V max
2.  2.5 V min/5.5 V max  
0.0 V

## 54LS76A

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub> t <sub>PHL1</sub>	Propagation Delay /Data-Output CLR <sub>n</sub> or PR <sub>n</sub> to Q <sub>n</sub>	5.0	28 20	5.0	40 35	5.0	40 35	ns ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
t <sub>PLH1</sub> t <sub>PLH1</sub>	Propagation Delay /Data-Output CLR <sub>n</sub> or PR <sub>n</sub> to Q <sub>n</sub>	5.0	21 20	5.0	32 27	5.0	32 27	ns ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
t <sub>PHL2</sub>	Propagation Delay /Data-Output CLK <sub>n</sub> to Q <sub>n</sub>	5.0	30	5.0	42	5.0	42	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
t <sub>PLH2</sub>	Propagation Delay /Data-Output CLK <sub>n</sub> to Q <sub>n</sub>	5.0	22	5.0	32	5.0	32	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	25		25		25		MHz	V <sub>CC</sub> = 5.0 V, V <sub>IN</sub> = 2.7 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	30						MHz	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ ± 5.0%.

**NOTES:**

1. f<sub>MAX</sub> min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C<sub>L</sub> = 15 pF are guaranteed but not tested.