LF157 Monolithic JFET Input Operational Amplifiers

LF157, LF157A, LF357, LF357A

Wide Band Decompensated ($A_{V_{MIN}}$ = 10)

General Description

These are among the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

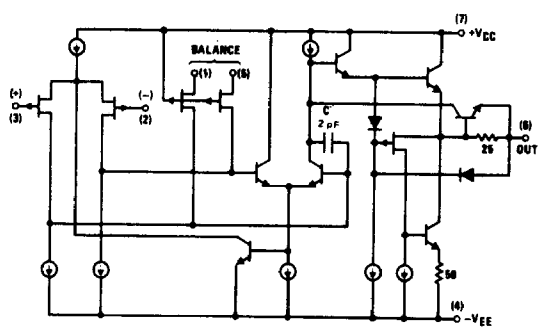
Features

LF157A

Low input bias current	30 pA
Low Input Offset Current	3 pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1 mV
Low input offset voltage temperature drift	3μV/°C
Low input noise current	0.01 pA/√Hz
High common-mode rejection ratio	100 dB
Large dc voltage gain	106 dB

	LF157A (A_V = 10)	UNITS
Extremely fast settling time to 0.01%	1.5	μs
Fast slew rate	50	V/μs
Wide gain bandwidth	20	MHz
Low input noise voltage	18	nV/√Hz

Simplified Schematic



Absolute Maximum Ratings

	LF157A	LF157	LF357A/LF357
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 1)	670 mW	670 mW	500 mW
TO-99)H package)			
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C	0°C to +70°C
$T_{j(MAX)}$	150°C	150°C	100°C
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF157A			LF357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3			3		µV/°C
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{os}	Input Offset Current	$T_j = 25°C$, (Notes 3, 6) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$ Over Temperature	50	200		50 25	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$ $V_S = \pm15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	±12		±11	±12		V V
CMRR	Common-mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF157A/357A			UNITS
			MIN	TYP	MAX	
SR	Slew Rate	LF157A: $A_V = 5$	40	50		V/µs
GBW	Gain-Bandwidth Product		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		32 18		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF157			LF357			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ$ Over Temperature		3	5 7		3	10 13	mV mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5		$\mu V/^\circ C$
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu V/^\circ C$ per mV
I_{os}	Input Offset Current	$T_j = 25^\circ C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25^\circ C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25^\circ C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25^\circ C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 10k$	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	± 11	± 12		± 10	± 12		V V
CMRR	Common-Mode Rejection Ratio		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		80	100		dB

DC Electrical Characteristics $T_A = 25^\circ C$, $V_S = \pm 15V$

PARAMETER	LF157A/LF157		LF357A/LF357		UNITS
	TYP	MAX	TYP	MAX	
Supply Current	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25^\circ C$, $V_S = \pm 15V$

SYMBOL	PARAMETER	CONDITIONS	LF157	LF157/357	UNITS
			MIN	TYP	
SR	Slew Rate	LF157: $A_V = 10$	30	50	$V/\mu s$
GBW	Gain-Bandwidth Product			20	MHz
t_s	Settling Time to 0.01%	(Note 7)		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 32 18	 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz		0.01 0.01	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3	pF

Notes for Electrical Characteristics

Note 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF157A and the LF157. For the LF357/LF357A these specifications apply for $\pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS} I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA} Pd$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time as defined here, is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -10$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

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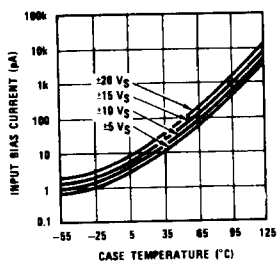
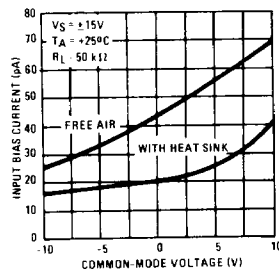
Typical DC Performance Characteristics Curves are for LF157 unless otherwise specified.

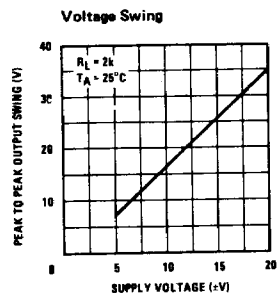
Input Bias Current



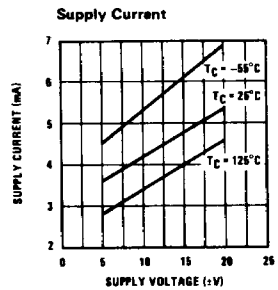
Input Bias Current



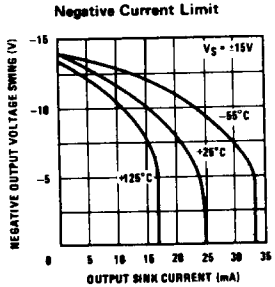
Voltage Swing



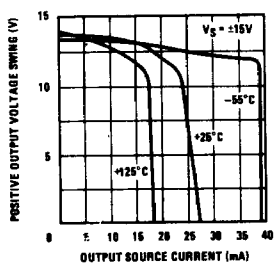
Supply Current



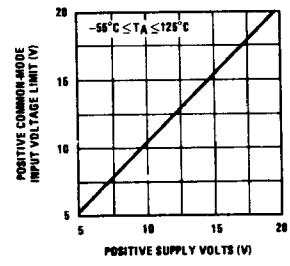
Negative Current Limit



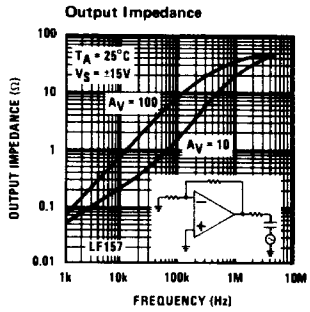
Positive Current Limit



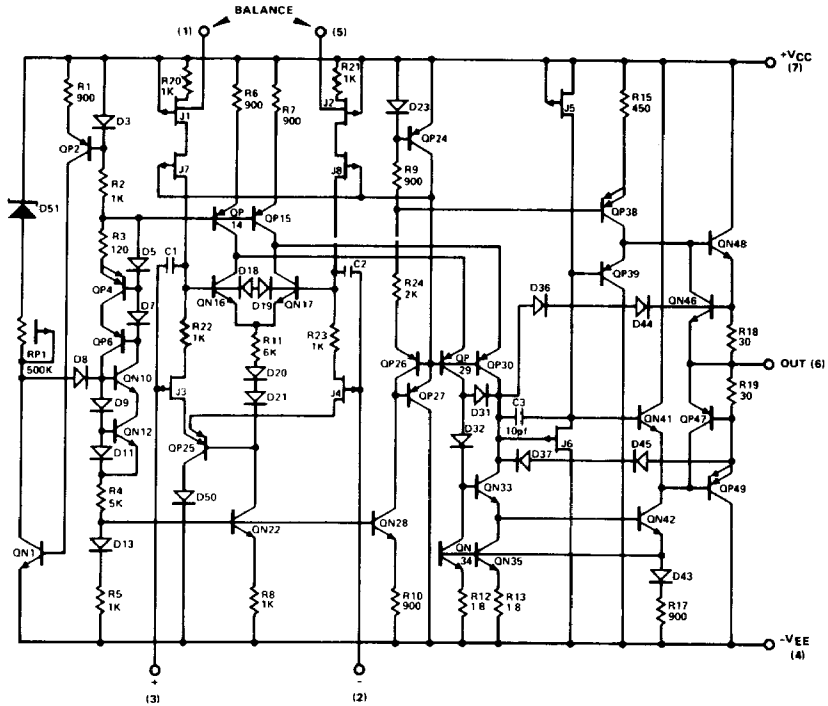
Positive Common-Mode Input Voltage Limit



Typical AC Performance Characteristics (Continued)



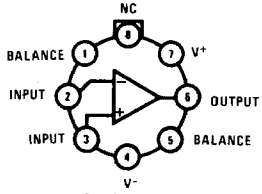
Detailed Schematic



Connection Diagrams

Section 11 for Packaging

Metal Can Package

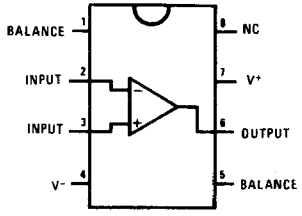


Note 4: Pin 4 connected to case.

TOP VIEW

Order Number
LF157AH
LF157H
LF357AH
LF357H

Dual-In-Line Package



Order Number
LF357J-8, LF357N

TOP VIEW

Application Hints

The LF157 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

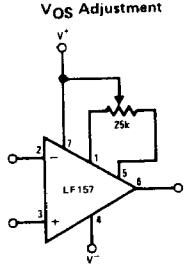
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant

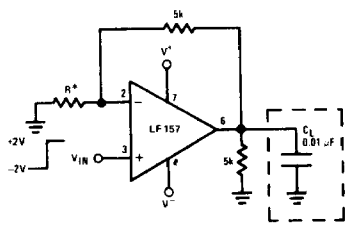
Typical Circuit Connections

V_{OS} Adjustment



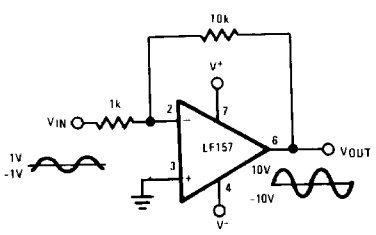
- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ÷(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(MAX)} \cong 0.01\ \mu F$
Overshoot $\leq 20\%$
Settling time (t_s) $\cong 5\ \mu s$

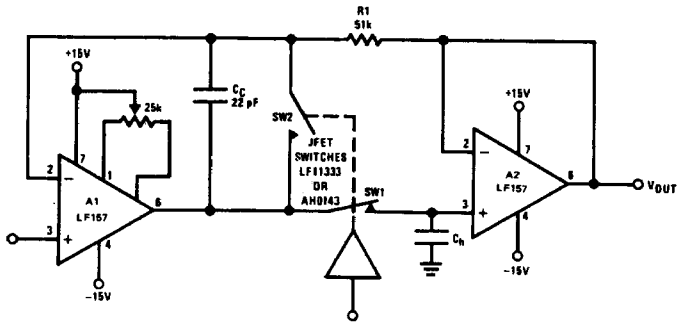
LF157. A Large Power BW Amplifier



For distortion < 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz

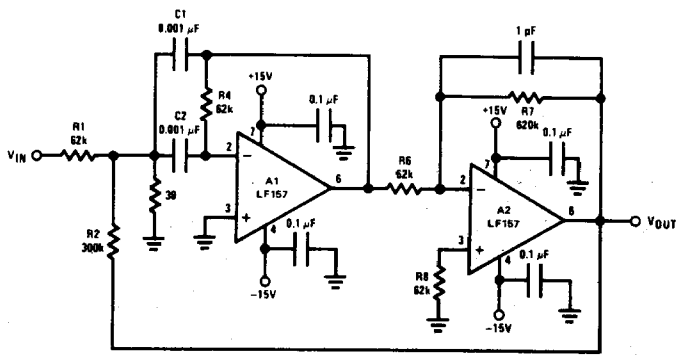
Typical Applications (Continued)

High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation

High Q Band Pass Filter



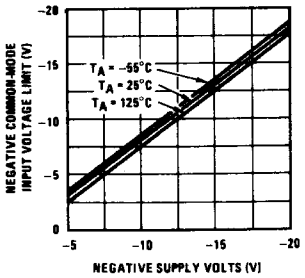
- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

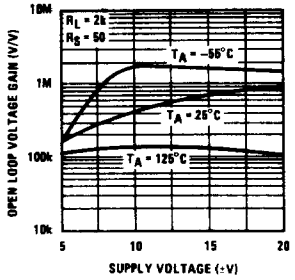
- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 µs

Typical DC Performance Characteristics (Continued)

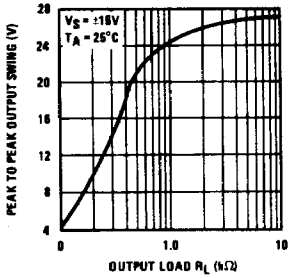
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

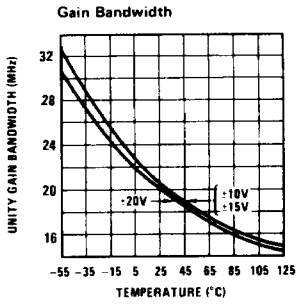


Output Voltage Swing

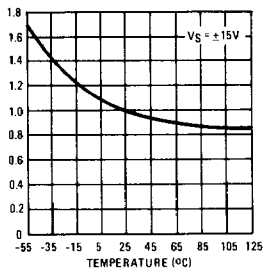


Typical AC Performance Characteristics

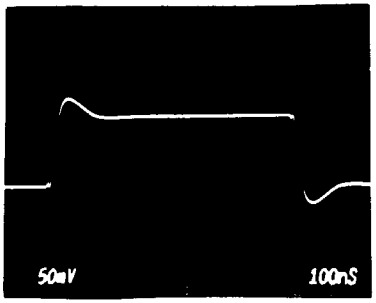
Gain Bandwidth



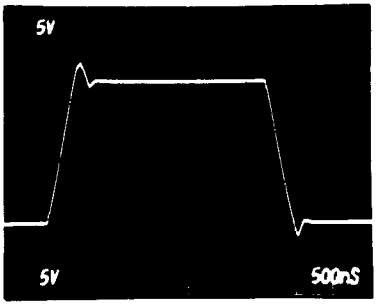
Normalized Slew Rate



LF157 Small Signal Pulse Response, A_V = +10

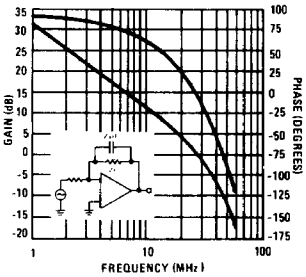


LF157 Large Signal Pulse Response, A_V = +10

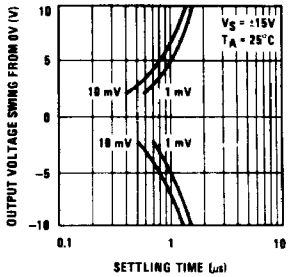


Typical AC Performance Characteristics (Continued)

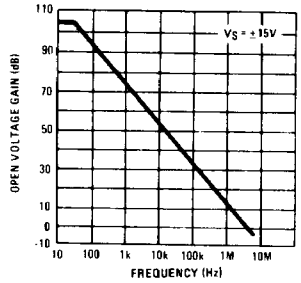
Bode Plot



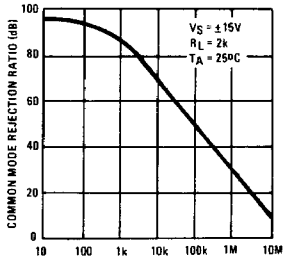
Inverter Settling Time



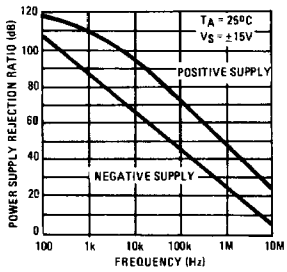
Open Loop Frequency Response



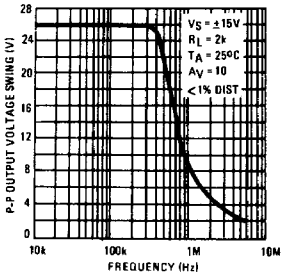
Common-Mode Rejection Ratio



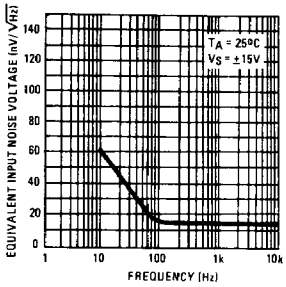
Power Supply Rejection Ratio



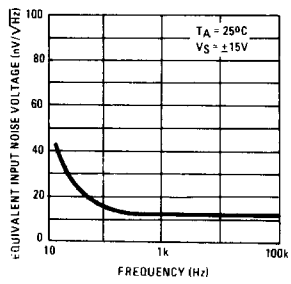
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

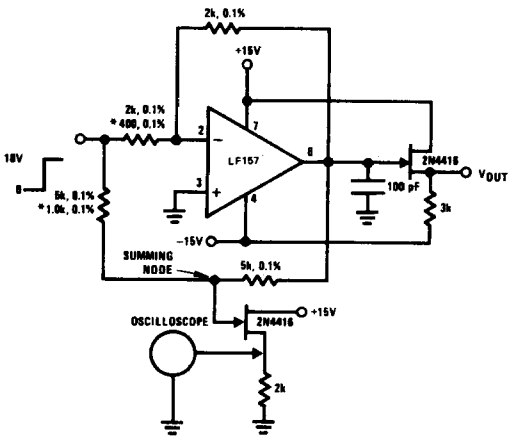


Equivalent Input Noise Voltage (Expanded Scale)



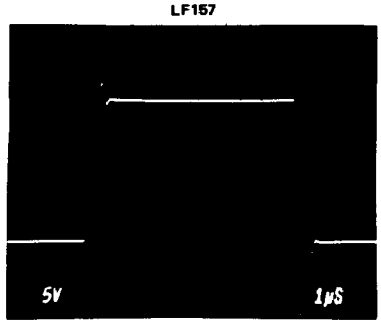
Typical Applications

Settling Time Test Circuit



- Settling time is tested with the LF157 connected for $A_V = -10$
- FET used to isolate the probe capacitance
- Output = 10V step

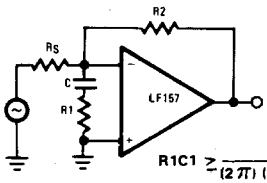
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



1 μs/DIV

Low Drift Adjustable Voltage Reference

Non-Inverting Unity Gain Operation for LF157



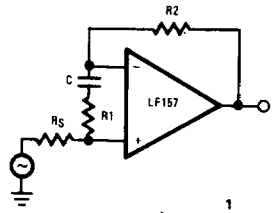
$$R1C1 \geq \frac{1}{(2\pi)(5\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5MHz$

Inverting Unity Gain for LF157



$$R1C1 \geq \frac{1}{(2\pi)(5\ MHz)}$$

$$R1 = \frac{R2}{4}$$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5MHz$