M74HC534-1P/FP

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC534-1 is an integrated circuit chip consisting of eight edge-triggered 3-state output D-type flip-flops with common clock input and output-enable input.

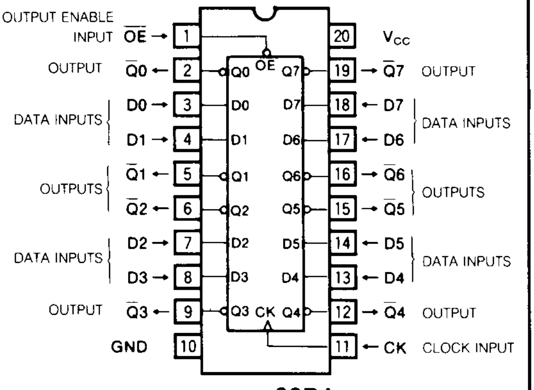
FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : (Clock frequency) 80MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : V_{CC}=2~6V
- Wide operating temperature range : T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 20P2N

FUNCTION

Use of silicon gate technology allows the M74HC534-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS534. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents.

The M74HC534-1 consists of eight edge-triggered D-type flip-flops, sharing common clock input CK and output-enable input $\overline{OE}$.

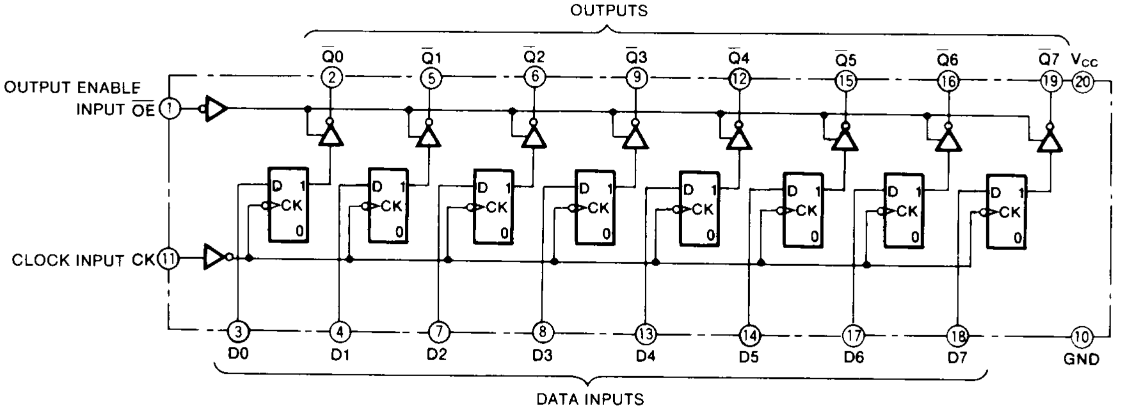
When CK changes from low-level to high-level, the signals just previously data input D is stored in the flip-flop.

When $\overline{OE}$ is low-level, the signal stored in the flip-flop will be output to $\overline{Q}$.

When $\overline{OE}$ is high-level, all outputs $\overline{Q}$ will become high impedance state. The contents stored in the flip-flop will not be affecterd even if $\overline{OE}$ changes.

A version of the M74HC534-1 with the same pin connection and a noninverted output, the M74HC374-1, is also available.

LOGICAL DIAGRAM



OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Inputs			Output
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	$\overline{Q}^0$
L	H	X	$\overline{Q}^0$
L	↓	X	$\overline{Q}^0$
H	X	X	Z

Note 1 : $\overline{Q}^0$: Output state $\overline{Q}$ before $\overline{CK}$ changed.
Z : High impedance
X : Irrelevant
↑ : Chnage from low-to high-level
↓ : Change from high-to low-level

ABSOLUTE MAXIMUM RATINGS (T_a = −40~+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage		−0.5~V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
Pd	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65~+150	℃

Note 2 : M74HC534-1FP : T_a=−40~+75℃ and T_a=75~85℃ are derated at −7mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40~+85℃)

Symbol	Parameter		Limits Min	Typ	Max	Unit
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		−40		+85	℃
t_r, t_f	Input rise time, fall time	V_{CC} = 2.0V	0		500	ns/V
		V_{CC} = 4.5V	0		50	
		V_{CC} = 6.0V	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC} = 0.1V, I_O = 20μA		2.0	1.5			1.5		V
				4.5	3.15			3.15		
				6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V, I_O = 20μA		2.0			0.5		0.5	V
				4.5			1.35		1.35	
				6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IL}, V_{IH}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −24mA	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0			0.1		0.1	V
			I_{OL} = 20μA	4.5			0.1		0.1	
			I_{OL} = 20μA	6.0			0.1		0.1	
			I_{OL} = 24mA	4.5			0.44		0.53	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			5.0		50.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 4)	35			MHz
t_{TLH}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{THL}	Low-to high-level and high-to low-level output transition time	C_L = 50pF (Note 4)			10	ns
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns
t_{PHL}	Low-to high-level and high-to low-level output propagation time (CK − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			18	ns
t_{PHZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 5 pF (Note 4)			18	ns
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns
t_{PZH}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)	C_L = 50pF (Note 4)			20	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	V_{CC}(V)	25℃ Min	25℃ Typ	25℃ Max	−40~+85℃ Min	−40~+85℃ Max	Unit
f_{max}	Maximum repetitive frequency	C_L = 50pF (Note 4)	2.0	6			5		MHz
			4.5	32			26		
			6.0	38			31		
t_{TLH}	Low-to high-level and high-to low-level output transition time		2.0		13	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{THL}			2.0		16	60		75	ns
			4.5		5	12		15	
			6.0		4	10		13	
t_{PLH}	Low-to high-level and high-to low-level output propagation time (CK − $\overline{Q}$)		2.0		35	105		130	ns
			4.5		12	21		26	
			6.0		10	18		22	
t_{PHL}			2.0		34	105		130	ns
			4.5		13	21		26	
			6.0		10	18		22	
t_{PLZ}	Low-level and high-level output disable time ($\overline{OE}$ − $\overline{Q}$)		2.0		16	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
t_{PHZ}			2.0		17	105		130	ns
			4.5		10	21		26	
			6.0		10	18		22	
t_{PZL}	Low-level and high-level output enable time ($\overline{OE}$ − $\overline{Q}$)		2.0		22	105		130	ns
			4.5		8	21		26	
			6.0		7	18		22	
t_{PZH}			2.0		27	105		130	ns
			4.5		11	21		26	
			6.0		9	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				61.6				pF

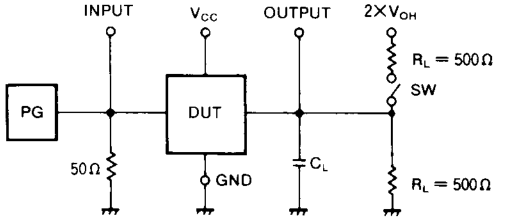
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per flip-flop). The power dissipated during operation under no-load condition is calculated using the following formula :
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOP

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	Clock pulse width		2.0	60	10		75		ns
			4.5	12	3		15		
			6.0	10	2		13		
t_{su}	D setup time with respect to CK		2.0	50	2		65		ns
			4.5	10	1		13		
			6.0	9	0		11		
t_h	D hold time with respect to CK		2.0	25	1		30		ns
			4.5	5	1		6		
			6.0	5	0		6		

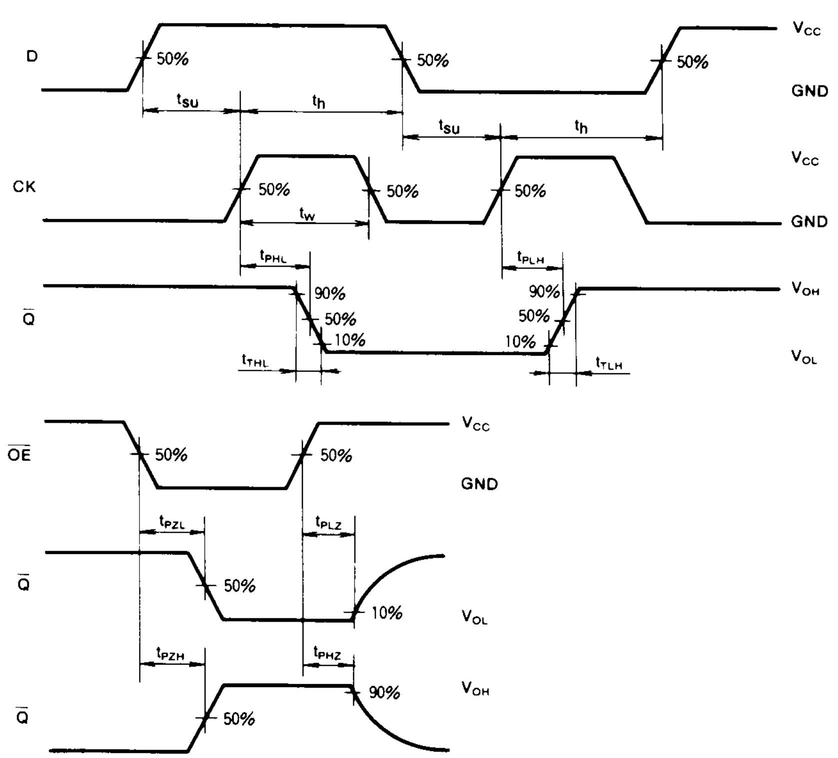
Note 4 : Test Circuit



Parameter	SW
t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

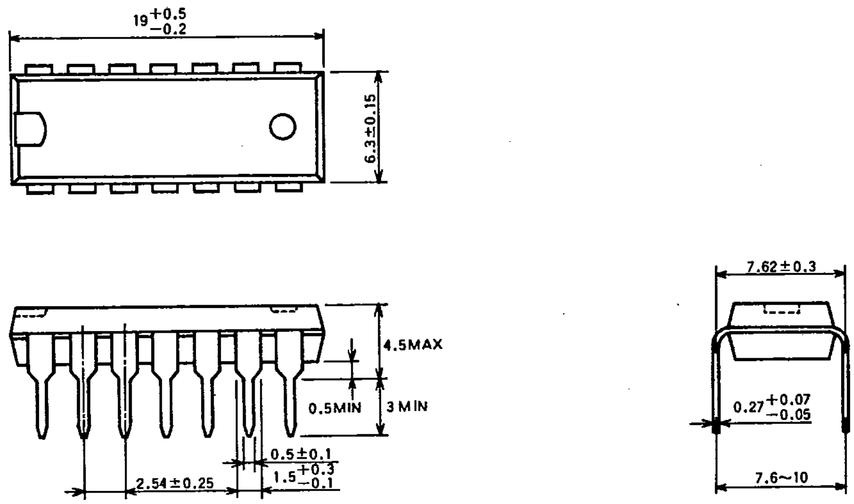


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

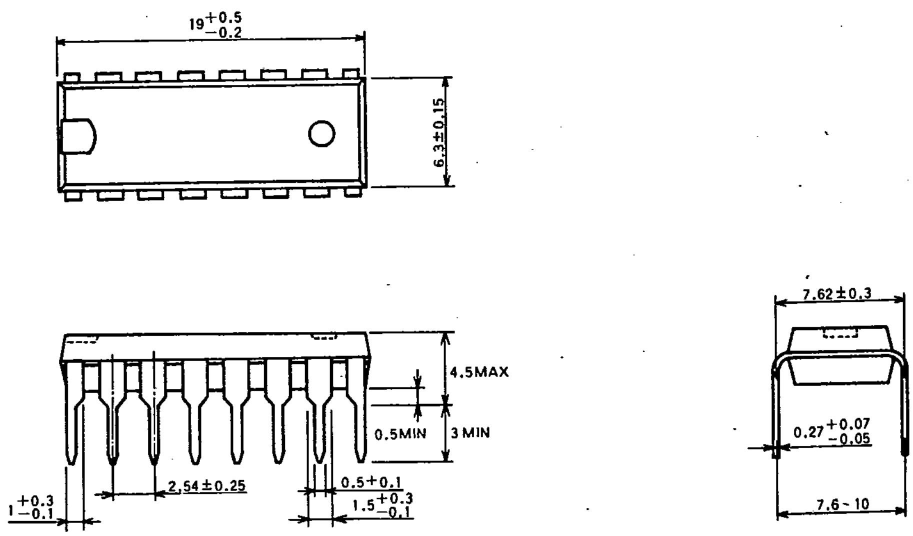
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm

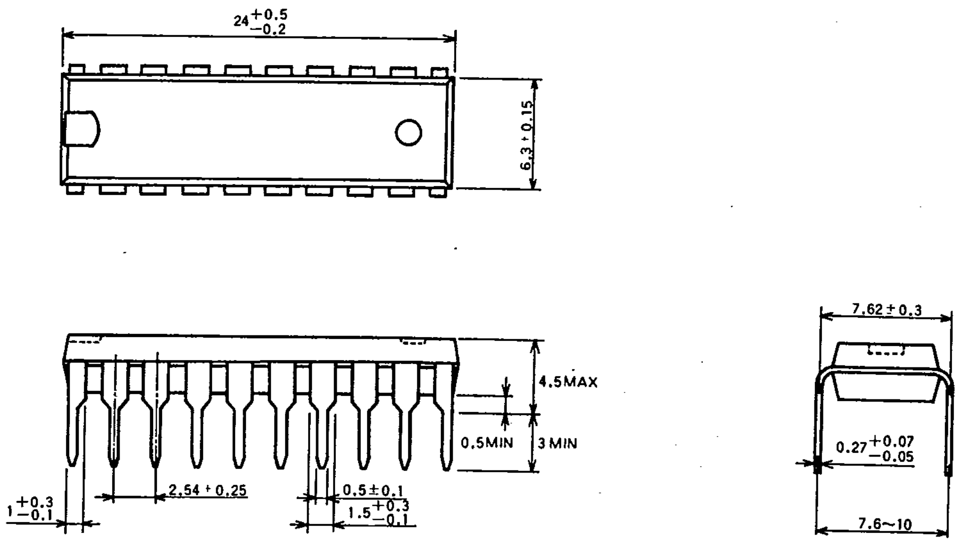


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

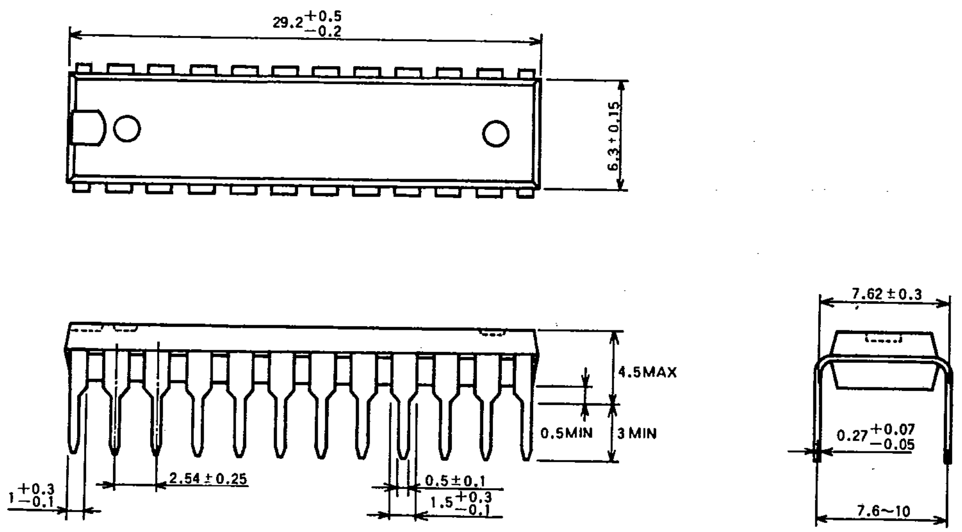
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

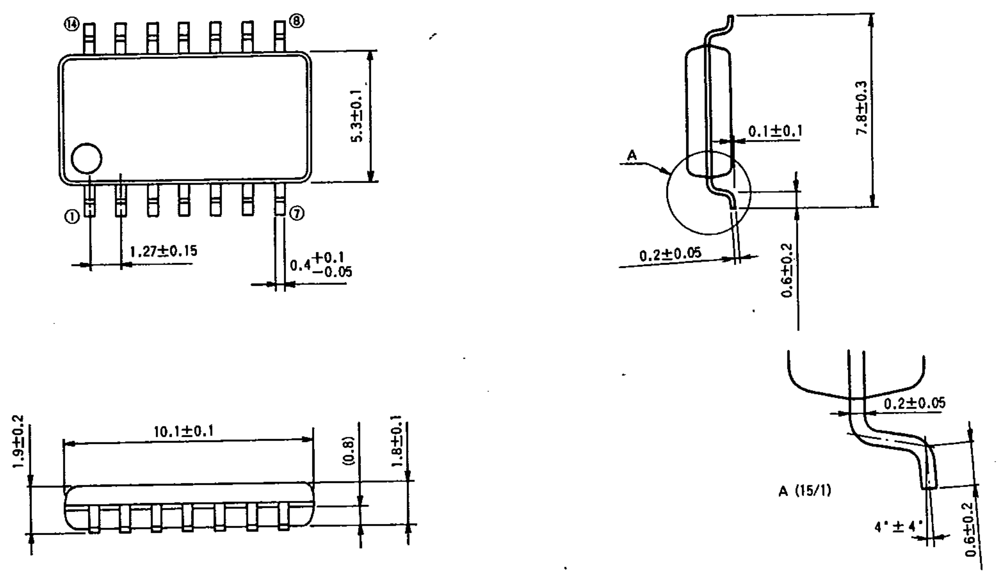
Dimension in mm



MITSUBISHI ELECTRIC

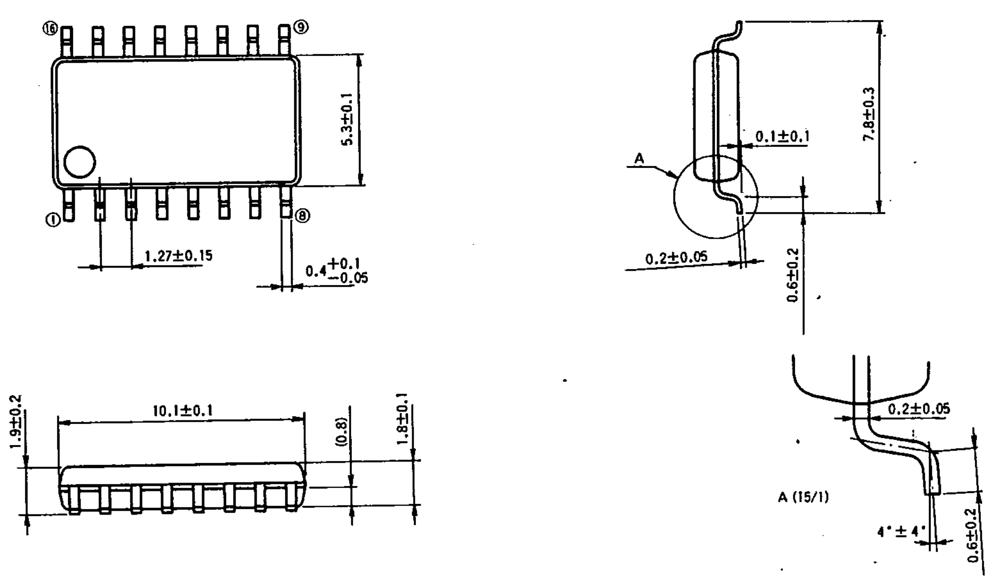
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

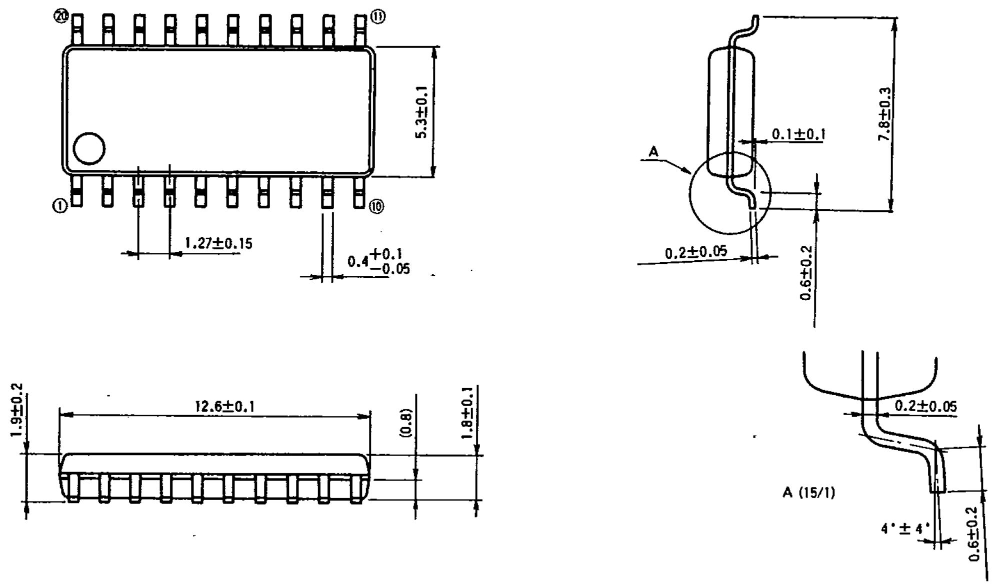
Dimension in mm



PACKAGE OUTLINES

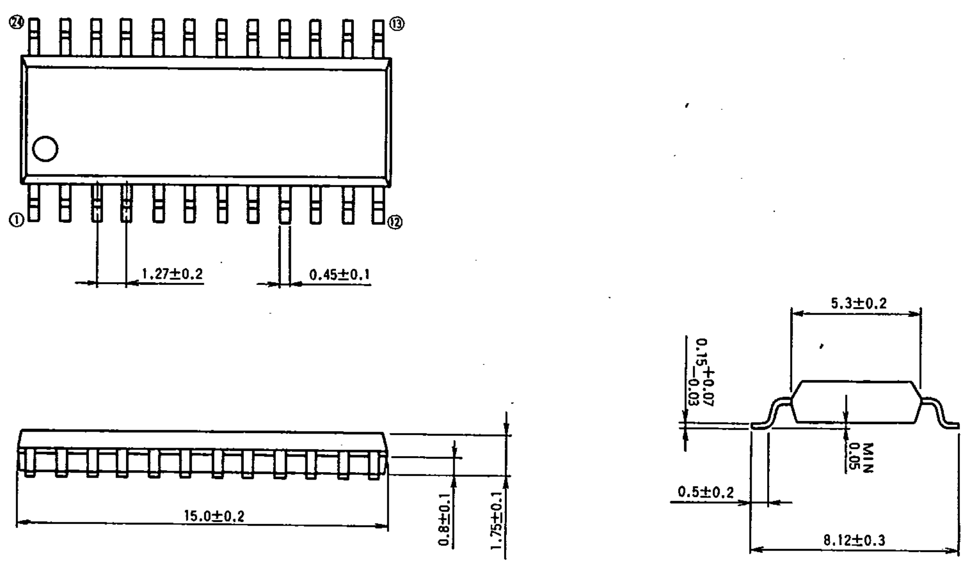
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

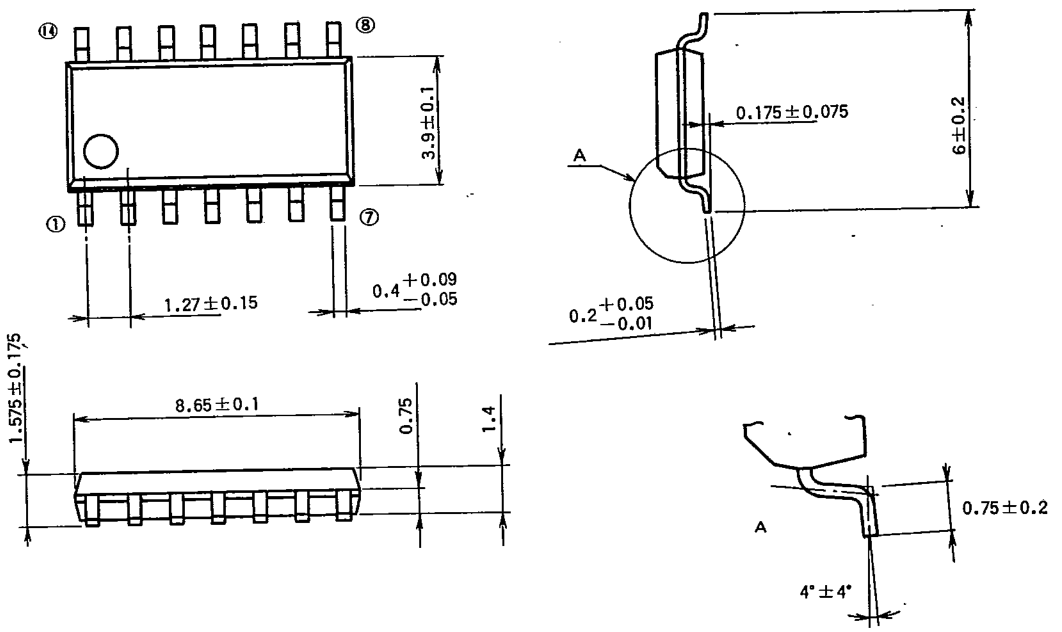
Dimension in mm



PACKAGE OUTLINES

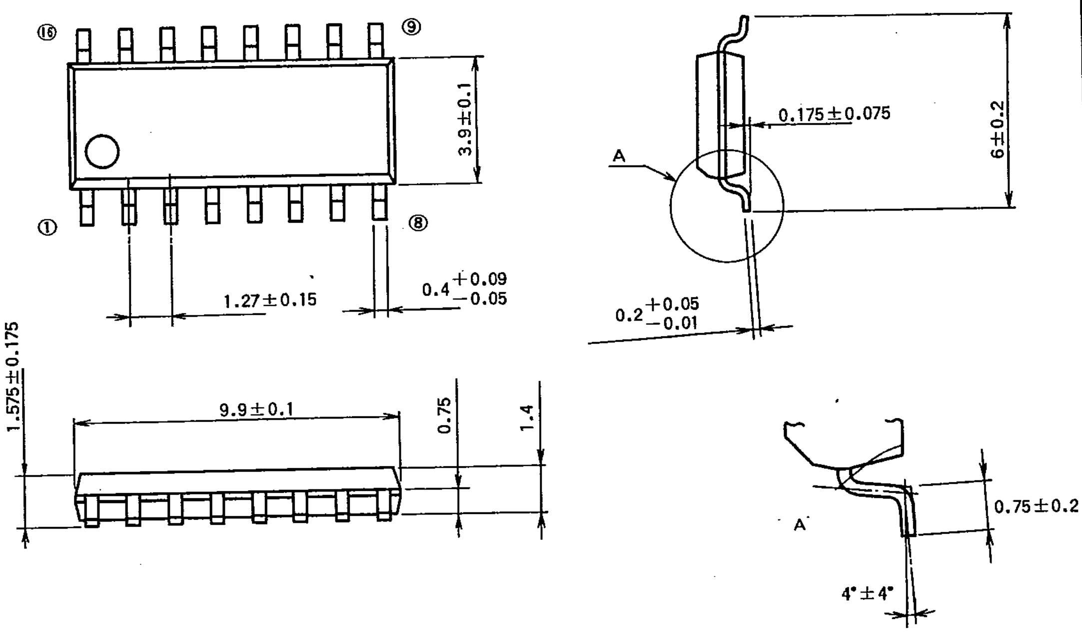
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

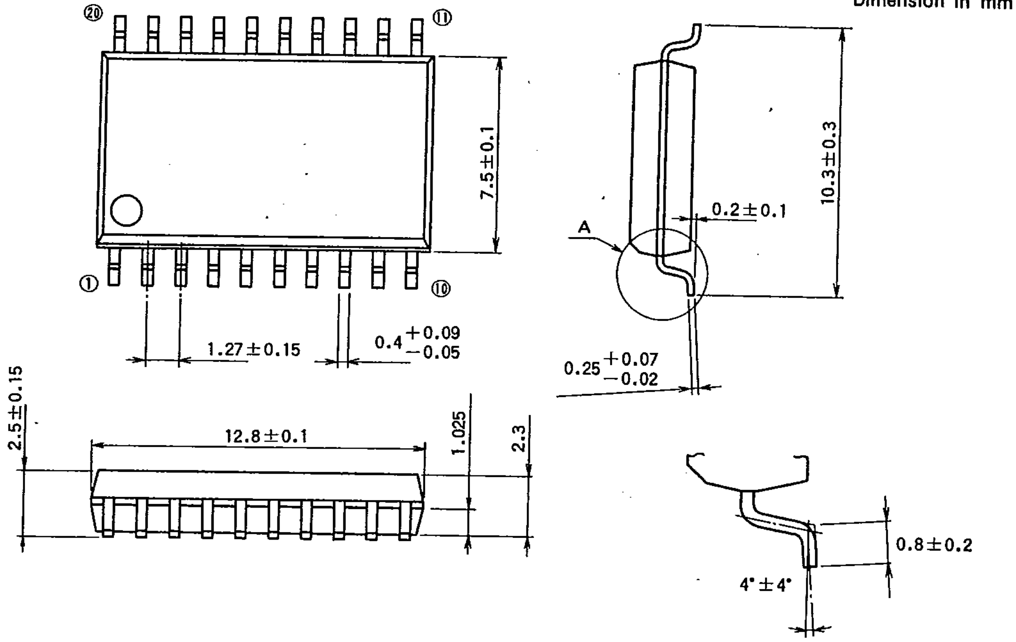
Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm



MITSUBISHI ELECTRIC