



# High Speed CMOS Bus Interface 8-Bit Latches

QS54/74FCT373T  
QS54/74FCT533T\*

QS54/74FCT2373T  
QS54/74FCT2533T\*

## FEATURES/BENEFITS

- Pin and function compatible to the 74F373/533 74FCT373/533 and 74ABT373/533
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 373T, 533T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, C, and D speed grades with 3.7 ns for D
- $I_{OL} = 48$  mA Com., 32 mA Mil.

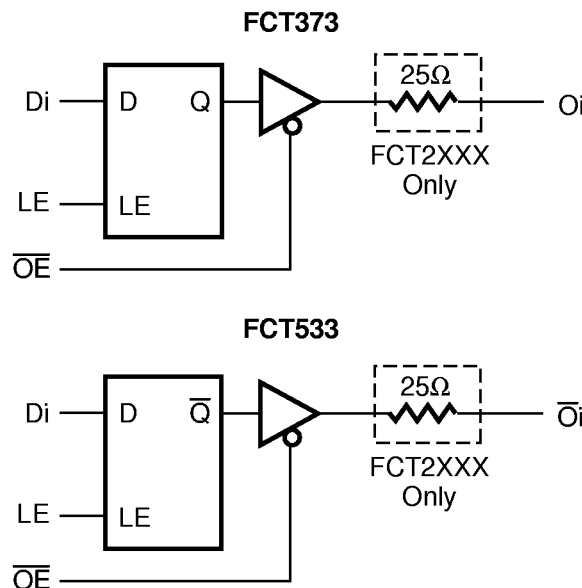
### FCT-T 2373T, 2533T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- Std., A, C, and D speed grades with 3.7 ns for D
- $I_{OL} = 12$  mA Com.

## DESCRIPTION

The QSFCT373T and QSFCT533T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2373 and 2533 devices are  $25\Omega$  resistor output versions useful for driving transmission lines and reducing system noise. The 2373 and 2533 series parts can replace 373 and 533 devices in existing designs to reduce noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

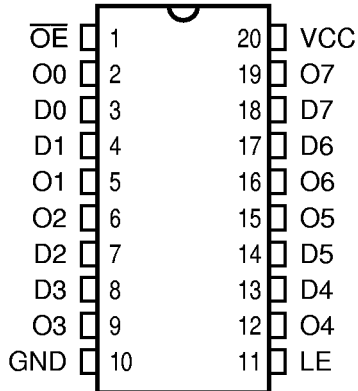
## FUNCTIONAL BLOCK DIAGRAM



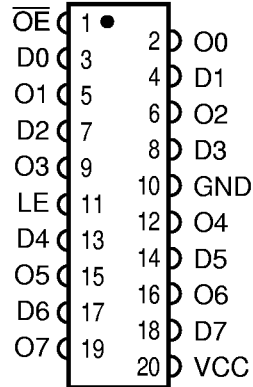
\*Note: QS54/74FCT533T and QS54/74FCT2533T are not recommended for use in new designs

**PIN CONFIGURATIONS (All Pins Top View)**

PDIP, SOIC, QSOP, HQSOP



ZIP



**PIN DESCRIPTION**

Name	I/O	Description
Di	I	Data Inputs
O <sub>i</sub>	O	Data Outputs
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

**FUNCTION TABLE**

$\overline{OE}$	Inputs LE Di		Internal Q Value	Outputs		Function
				373 O <sub>i</sub>	533 $\overline{O_i}$	
H	X	X	X	Hi-Z	Hi-Z	Disable Outputs
L	L	X	H	H	L	Enable Outputs
L	L	X	L	L	H	
L	H	L	L	L	H	Pass Inputs
L	H	H	H	H	L	
L	L	X	Q	Q	$\overline{Q}$	Hold Prior Data

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1, 3, 4, 7, 8, 11, 13, 14, 17, 18	4	4	5	7	pF
2, 5, 6, 9, 12, 15, 16, 19	6	6	7	9	pF
—	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0$ <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/ MHz

### Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
- For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2XXX - 25 $\Omega$ )	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}$ $I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$V_{OL}$	Output LOW Voltage (FCT2XXX - 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2XXX - 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

## QSFCT373T, 533T, 2373T, 2533T

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

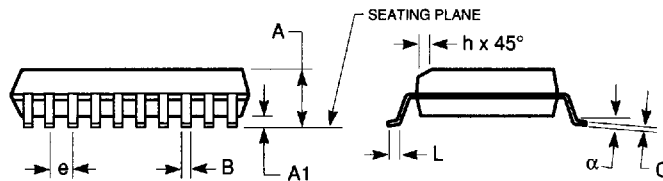
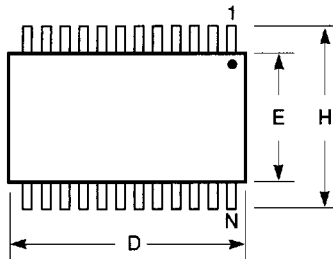
$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		373 533 2373 2533		373A 533A 2373A 2533A		373C 533C 2373C 2533C		373D 533D 2373D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	COM	1.5	8	1.5	5.2	1.5	4.2	1.5	3.7	ns
t <sub>PLH</sub>	Data to O <sub>i</sub> , 373	MIL	2	8.5	1.5	5.6	1.5	5.1	—	—	
t <sub>PHL</sub>	Propagation Delay	COM	1.5	8	1.5	5.2	1.5	4.2	1.5	3.7	ns
t <sub>PLH</sub>	Data to O <sub>i</sub> , 2373	MIL	2	8.5	1.5	5.6	1.5	5.1	—	—	
t <sub>PHL</sub>	Propagation Delay	COM	2	13	2	8.5	2	5.5	2	4.9	ns
t <sub>PLH</sub>	LE to O <sub>i</sub> , 373	MIL	2	14	2	9.8	2	8	—	—	
t <sub>PHL</sub>	Propagation Delay	COM	2	13	2	8.5	2	5.5	2	4.9	ns
t <sub>PLH</sub>	LE to O <sub>i</sub> , 2373	MIL	2	14	2	9.8	2	8	—	—	
t <sub>PZH</sub>	Output Enable Time	COM	1.5	11	1.5	6.5	1.5	5.5	1.5	5.5	ns
t <sub>PZL</sub>	$\overline{\text{OE}}$ to Y <sub>i</sub> , 373	MIL	1.5	12.5	1.5	7.5	1.5	6.3	—	—	
t <sub>PZH</sub>	Output Enable Time	COM	1.5	11	1.5	6.5	1.5	6.2	1.5	6.2	ns
t <sub>PZL</sub>	$\overline{\text{OE}}$ to Y <sub>i</sub> , 2373	MIL	1.5	12.5	1.5	7.5	1.5	7.2	—	—	
t <sub>PHZ</sub>	Output Disable Time	COM <sup>(2)</sup>	1.5	7	1.5	5.5	1.5	5.0	1.5	5.0	ns
t <sub>PLZ</sub>	$\overline{\text{OE}}$ to Y <sub>i</sub>	MIL <sup>(2)</sup>	1.5	8.5	1.5	6.5	1.5	5.9	—	—	
t <sub>s</sub>	Data Setup Time	COM	2	—	2	—	2	—	2	—	ns
		MIL	2	—	2	—	2	—	—	—	
t <sub>H</sub>	Data Hold Time	COM	1.5	—	1.5	—	1.5	—	1.5	—	ns
		MIL	1.5	—	1.5	—	1.5	—	—	—	
t <sub>w</sub>	LE Pulse Width	COM <sup>(2)</sup>	6	—	5	—	4	—	4	—	ns
	HIGH or LOW	MIL <sup>(2)</sup>	6	—	6	—	6	—	—	—	

**Notes:**

1. Minimums guaranteed but not tested for all parameters except  $t_s$  and  $t_H$ .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

**300-MIL SOIC - Package Code SO**  
Plastic Small Outline Gull-Wing



**Notes:**

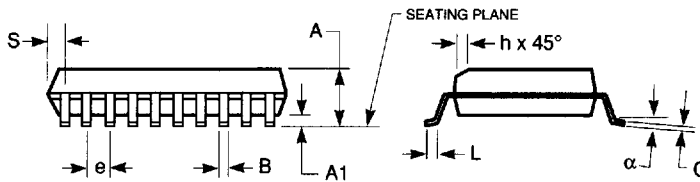
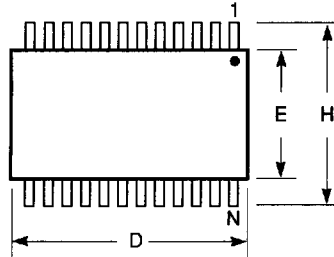
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.

JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
$\alpha$	0°	8°	0°	8°	0°	8°	0°	8°

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**150-MIL QSOP - Package Code Q**

**Quarter-Size Outline Package  
Plastic Small Outline Gull-Wing**



**Notes:**

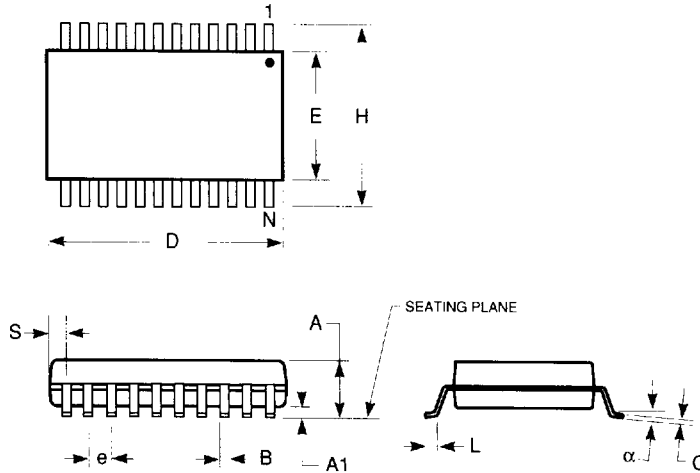
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.

JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

7466803 0003751 569  
QUALITY SEMICONDUCTOR, INC.

**150-MIL HQSOP - Package Code H**

Hermetic Quarter-Size Outline Package  
Ceramic Small Outline Gull-Wing



JEDEC#	TBD			TBD		
DWG#	HSS-20A			HSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.070	0.074	0.078	0.070	0.074	0.078
A1	0.008	0.012	0.016	0.008	0.012	0.016
B	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010
D	0.337	0.342	0.350	0.337	0.342	0.350
E	0.150	0.155	0.158	0.150	0.155	0.158
e	0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
L	0.016	0.025	0.035	0.016	0.025	0.035
N	20			24		
$\alpha$	0°	5°	8°	0°	5°	8°
S	0.056	0.058	0.062	0.031	0.033	0.037

**Notes:**

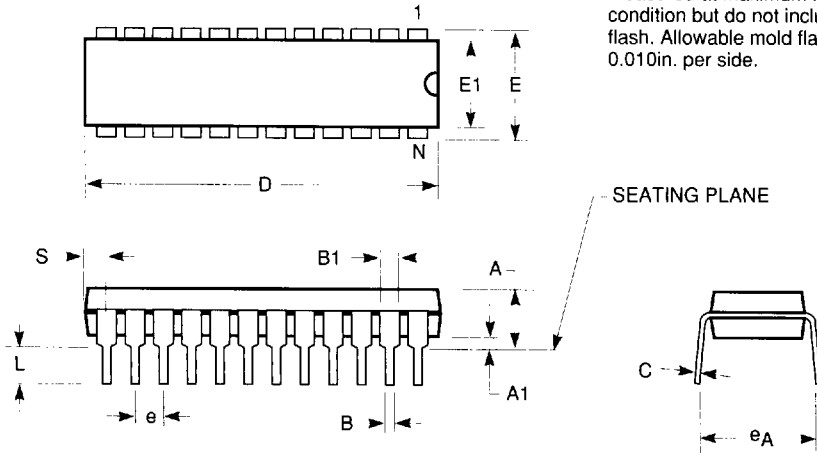
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition.
5. Lead coplanarity is 0.004in. maximum.



**300-MIL PDIP - Package Code P**  
**Plastic Dual In-line Package**

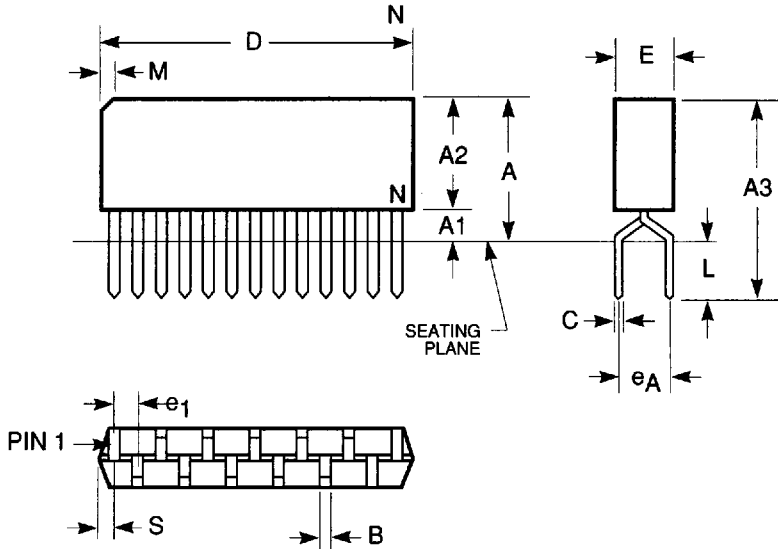
**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010in. per side.



JEDEC#	MS-001AC		MS001AA		MS-001AE		N/A		MS-001AF		MO-095AH	
DWG#	PD14A		PD16A		PD20A		PT22B		PT24A		PT28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.180
A1	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
B1	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.060
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.745	0.765	0.745	0.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
E1	0.240	0.270	0.240	0.270	0.240	0.270	0.240	0.270	0.250	0.280	0.275	0.295
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e <sub>A</sub>	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380
L	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
S	0.070	0.080	0.020	0.035	0.060	0.070	0.010	0.020	0.025	0.080	0.020	0.040
N	14		16		20		22		24		28	

**300-MIL ZIP - Package Code Z**  
Zig-zag In-line Packages



JEDEC#	MO-072AB		MO-072AC		MO-072AD	
DWG#	PZ20A		PZ24A		PZ28A	
Symbol	Min	Max	Min	Max	Min	Max
A	0.350	0.400	0.350	0.400	0.350	0.400
A1	0.030	0.070	0.030	0.070	0.032	0.055
A2	0.280	0.340	0.320	0.350	0.335	0.345
A3	0.450	0.550	0.450	0.550	0.460	0.550
B	0.015	0.024	0.015	0.024	0.015	0.024
C	0.008	0.012	0.008	0.012	0.008	0.012
D	1.008	1.030	1.200	1.250	1.409	1.424
E	0.100	0.120	0.100	0.120	0.110	0.120
e1	0.050 BSC		0.050 BSC		0.050 BSC	
eA	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.100	0.150	0.100	0.150	0.110	0.150
M	0.035	0.085	0.035	0.085	0.035	0.085
N	20		24		28	
S	0.018	0.032	0.018	0.032	0.025	0.038

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010in. per side.