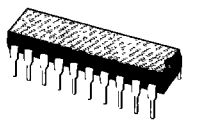
SGS-THOMSON MICROELECTRONICS

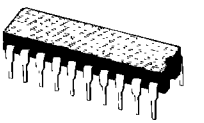
T74LS540
T74LS541

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS

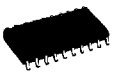
- PNP INPUTS REDUCE LOADING
- 3-STATE OUTPUTS DRIVE BUS LINES
- INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIERS INTERFACE TO MICROPROCESSOR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



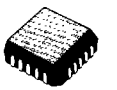
B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)



C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

DESCRIPTION

The T74LS540/541 are Octal Buffers and Line Drivers. Although they have the same functions as LS240 and LS241, they offer a pinout with inputs and outputs on apposite sides of the package. These device are disigned to be used with 3-state memory address drivers, etc.

TRUTH TABLE

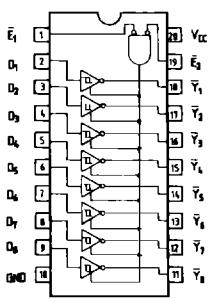
Inputs			Outputs	
$\bar{E}_1$	$\bar{E}_2$	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
Z = HIGH Impedance

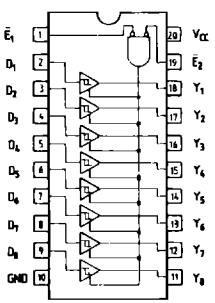
PIN CONNECTION (top view)

DUAL IN LINE

LS540

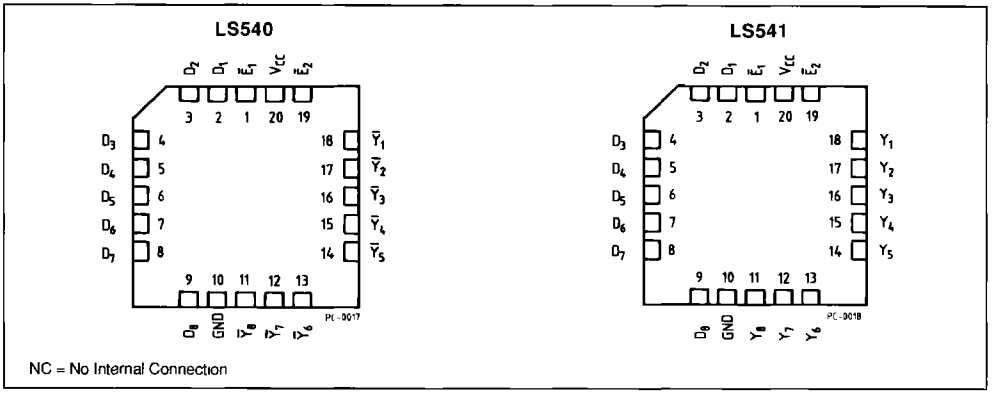


LS541

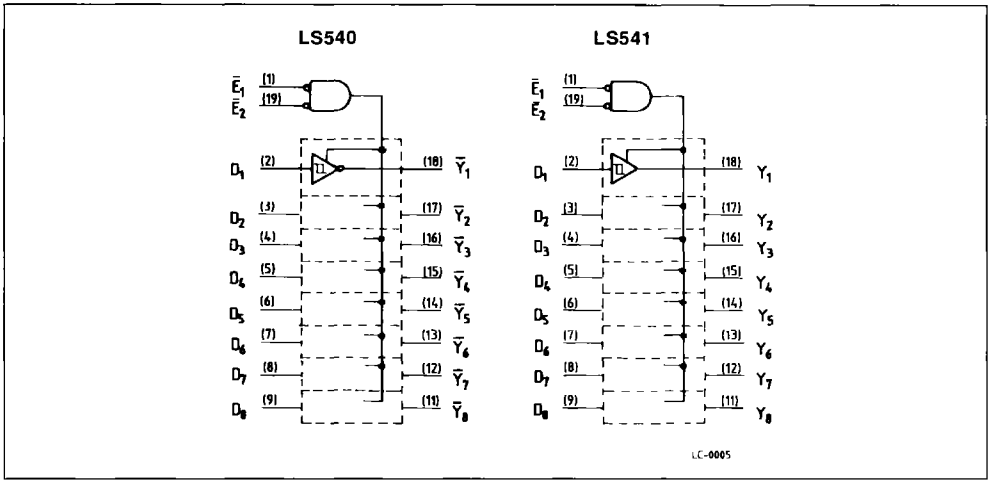


NC = No Internal Connection

CHIP CARRIER



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage. Applied to Output	0 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS540/541XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN. I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.4		V_{CC} = MIN. I_{OH} = - 3.0 mA		V
		2.0			V_{CC} = MIN. I_{OH} = - 15 mA V_{IL} = 0.5 V		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
V_{T+}-V_{T-}	Hysteresis	0.2	0.4		V_{CC} = MIN		
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V		µA
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
				0.1	VCC = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current			- 0.2	VCC = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 40		- 225	V_{CC} = MAX. V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Total, Output HIGH LS540			25	V_{CC} = MAX		mA
	Total, Output HIGH LS541			32			
	Total, Output LOW LS540			45			
	Total, Output LOW LS541			52			
	Total, Output 3-State LS540			52			
	Total, Output 3-State LS541			55			

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS (T_A = 25 °C)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (note 1)	Unit
t_{PLH}	Propagation Delay, Data to Output	LS540		9.0	15	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω	ns
		LS541		12	15		
t_{PHL}		LS540		12	15		ns
		LS541		12	18		
t_{PZH}	Output Enable Time to HIGH Level	LS540		15	25		ns
		LS541		15	32		
t_{PZL}	Output Enable Time to LOW LEvel	LS540		20	38		ns
		LS541		20	38		
t_{PHZ}	Output Disable Time from HIGH Level	LS540		10	18	C_L = 5.0 pF	ns
		LS541		10	18		
t_{PLZ}	Output Diable Time to LOW Level	LS540		15	25		ns
		LS541		15	29		

AC WAVEFORMS

Figure 1.

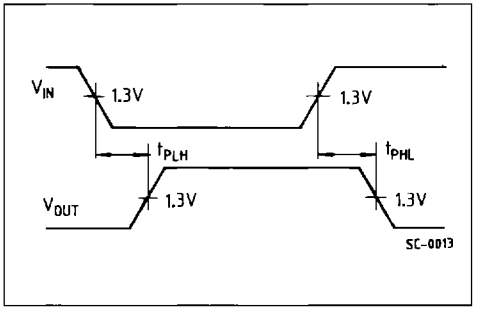


Figure 2.

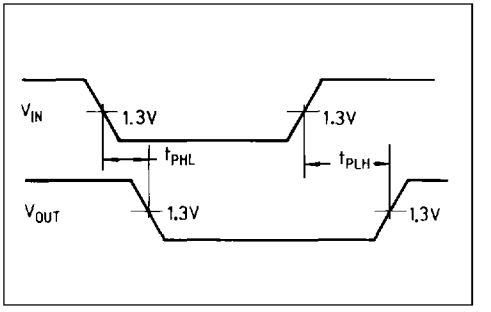


Figure 3.

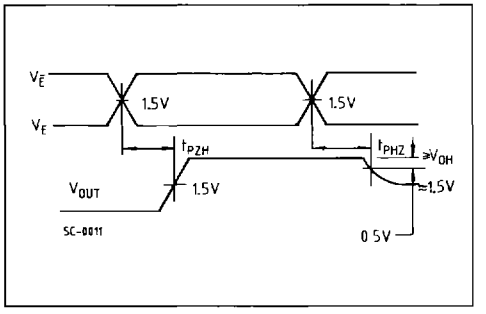
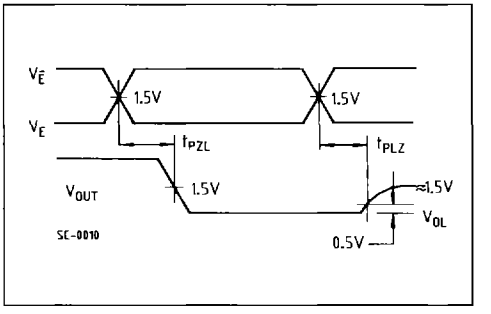
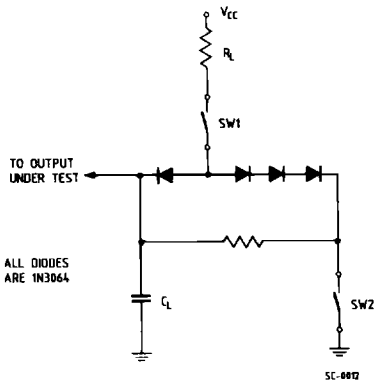


Figure 4.



AC LOAD CIRCUIT

Figure 5.



SWITCH POSITION

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed