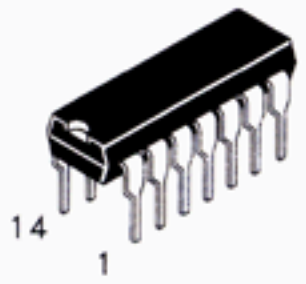
DV4069UB Available Q2, 1995

Quad 2-Input NOR (NAND) Gate
Dual 4-Input NOR (NAND) Gate
Triple 3-Input NOR (NAND) Gate
Quad 2-Input OR (AND) Gate
Hex Inverter Gate (unbuffered)

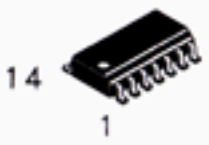
DV4001B (DV4011B)
DV4002B (DV4012B)
DV4025B (DV4023B)
DV4071B (DV4081B)
DV4069UB

These logic gates are constructed with P and N Channel devices in a single monolithic structure (Complementary MOS). They are used for low power dissipation and/or high noise immunity. The DV4069UB is an unbuffered device having slightly less gain but useful for certain applications such as oscillators.

- **Supply voltage range = 3.0 Vdc to 18 Vdc**
- **All outputs buffered**
- **Capable of driving 4 Low Power TTL loads or one LS TTL load over the rated temperature range**
- **Diode protection on all inputs**
- **Highest noise immunity at 12V supply**

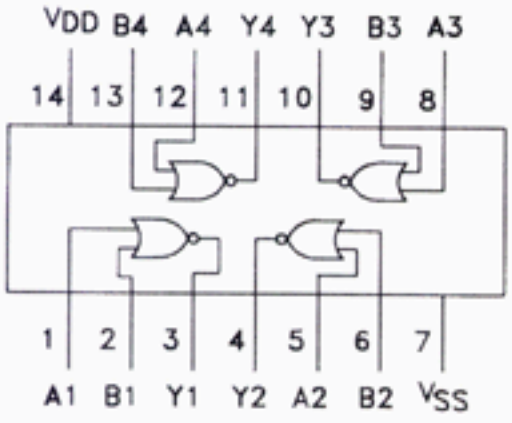


N Suffix
Plastic DIP
AVG-001 Case

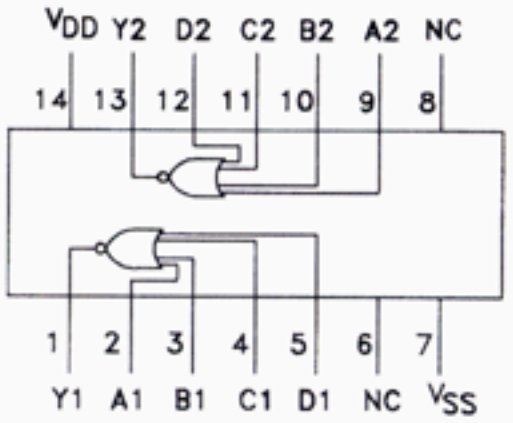


D Suffix
Plastic SOP
AVG-002 Case

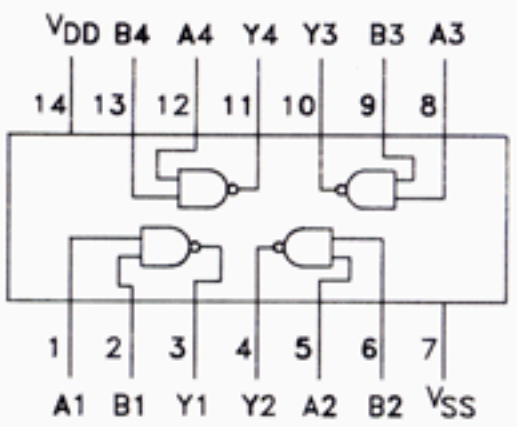
4001B



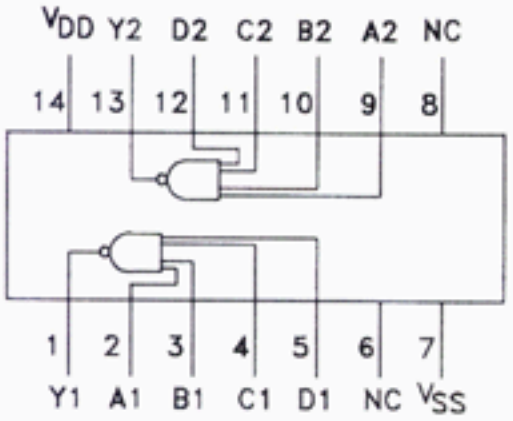
4002B



4011B

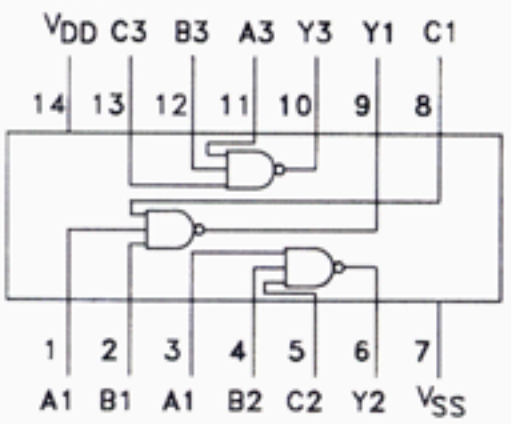


4012B

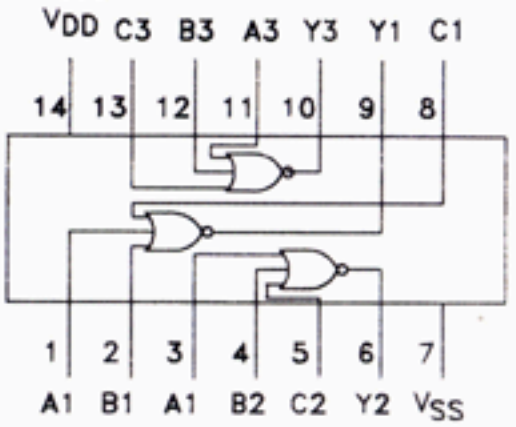


NC=No Connection

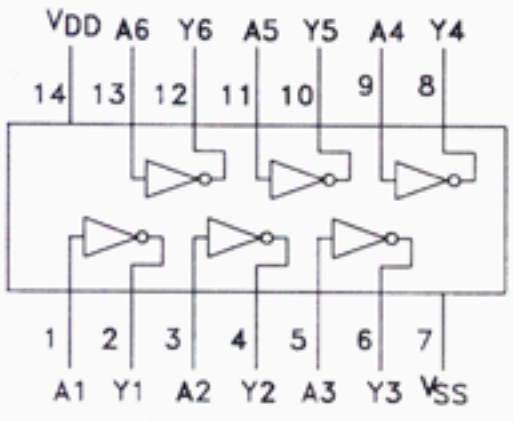
4023B



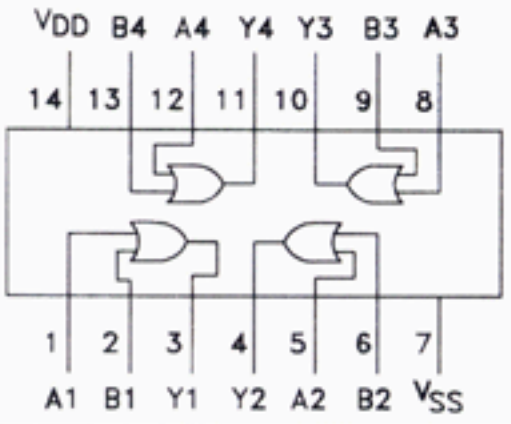
4025B



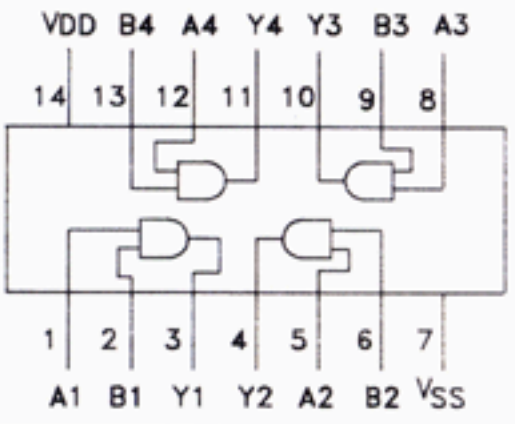
4069UB



4071B



4081B



4001, 02, 11, 12, 23, 25, 69U, 71, 81

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage (Referenced to V_{SS})	−0.5 to +18.0	V
V_{IN}, V_{OUT}	Input or Output Voltage	−0.5 to V_{DD}+0.5	V
I_{IN}, I_{OUT}	DC Current Into or Out of Any Pin	± 10	mA
P_D	Power Dissipation in Still Air, Derating: 12 mW/°C from 65° to 85°C	500	mW
T_{STG}	Storage Temperature Range	−65 to +150	°C
TL	Lead Temperature, (8 Second Soldering)	260	°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter		V_{DD}	Guaranteed Limits							Unit
				−40°C		25°C			85°C		
				Min	Max	Min	Typ	Max	Min	Max	
V_{OL}	Output Voltage V_{IN}=V_{DD} or 0	"0" Level	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V_{OH}	V_{IN}= 0 or V_{DD}	"1" Level	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
V_{IL} Buffered Devices	Input Voltage (V_O=4.5 or 0.5 Vdc) (V_O=9.0 or 1.0 Vdc) (V_O=13.5 or 1.5 Vdc)	"0" Level	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
V_{IL} Un-buffered Devices	DV4069UB only		5.0 10 15		1.0 2.0 2.5			1.0 2.0 2.5		1.0 2.0 2.5	Vdc
V_{IH} Buffered Devices	(V_O=0.5 or 4.5 Vdc) (V_O=1.0 or 9.0 Vdc) (V_O=1.5 or 13.5 Vdc)	"1" Level	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
V_{IH} Un-buffered Devices	DV4069UB only		5.0 10 15	4.0 8.0 12.5		.0 8.0 12.5			.0 8.0 12.5		
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	5.0 5.0 10 15	−2.5 −0.52 −1.3 −3.6	- - - -	−2.1 −0.44 −1.1 −3.0	−4.2 −0.88 −2.25 −8.8	- - - -	−1.7 −0.36 −0.9 −2.4	- - - -	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	5.0 10 15	0.52 1.3 3.6	- - -	0.44 1.1 3.0	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
I_{IN}	Input Current		15	-	±0.3	-	±0.00001	±0.3	-	±1.0	µAdc
C_{IN}	Input Capacitance	V_{IN}=0	-	-	-	-	5.0	7.5	-	-	pF
I_{DD}	Quiescent Current (Per Package)		5.0 10 15	- - -	1.0 2.0 4.0	- - -	0.0005 0.0010 0.0015	1.0 2.0 4.0	- - -	7.5 15 30	µAdc

SWITCHING CHARACTERISTICS (C_L=50 pF, T_A=25°C)

Symbol	Characteristics	V_{DD}	Min	Typ	Max	Unit
t_{TLH}	Output Rise Time	5.0 10 15	- - -	100 50 40	200 100 80	ns
t_{THL}	Output Fall Time	5.0 10 15	- - -	100 50 40	200 100 80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time 4001B, 4011B Only	5.0 10 15	- - -	125 50 40	250 100 80	ns
	All Other 2, 3, and 4 Input Gates	5.0 10 15	- - -	160 65 50	300 130 100	
	DV4069UB only	5.0 10 15		65 40 30	125 75 55	ns

SWITCHING WAVEFORMS