

54F/74F674

16-Bit Serial/Parallel-In, Serial-Out Shift Register

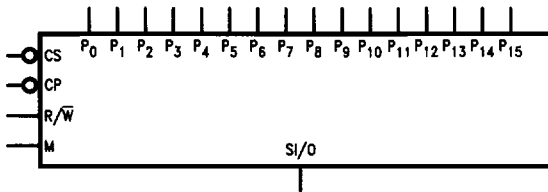
General Description

The '674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a TRI-STATE® serial output. In the serial-out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility.

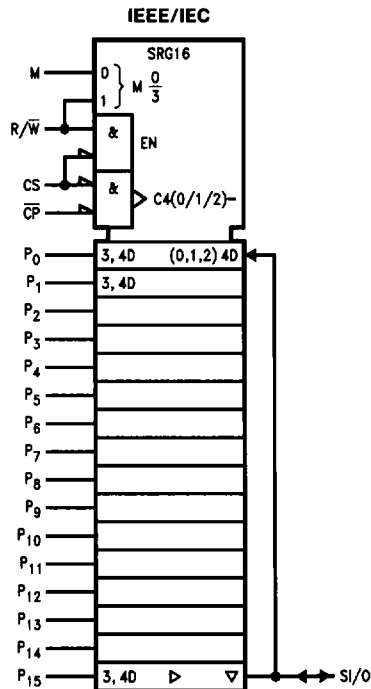
Features

- 16-Bit serial I/O shift register
- 16-Bit parallel-in, serial-out converter
- Recirculating serial shifting
- Common serial data I/O pin
- Slim 24 lead DIP

Logic Symbols



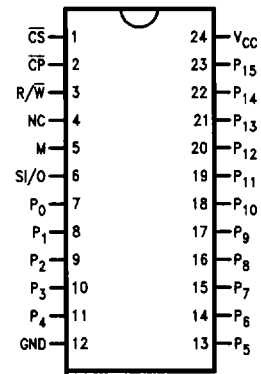
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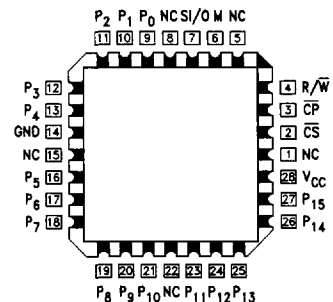
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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Pin Assignment for LCC and PCC



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Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table.

Hold—a HIGH signal on the Chip Select (\overline{CS}) input prevents clocking and forces the Serial Input/Output (SI/O) TRI-STATE buffer into high impedance state.

Serial Load—data present on the SI/O pin shifts into the register on the falling edge of \overline{CP} . Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial Output—the SI/O TRI-STATE buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0 .

Parallel Load—data present on P_0 – P_{15} are entered into the register on the falling edge of \overline{CP} . The SI/O TRI-STATE buffer is active and represents the Q_{15} output.

To prevent false clocking, \overline{CP} must be LOW during a LOW-to-HIGH transition of \overline{CS} .

Shift Register Operations Table

| Control Inputs | | | | SI/O Status | Operating Mode |
|-----------------|-----|----------------|-----------------|-------------|----------------------------------|
| \overline{CS} | R/W | \overline{M} | \overline{CP} | | |
| H | X | X | X | High Z | Hold |
| L | L | X | \sim | Data In | Serial Load |
| L | H | L | \sim | Data Out | Serial Output with Recirculation |
| L | H | H | \sim | Active | Parallel Load; No Shifting |

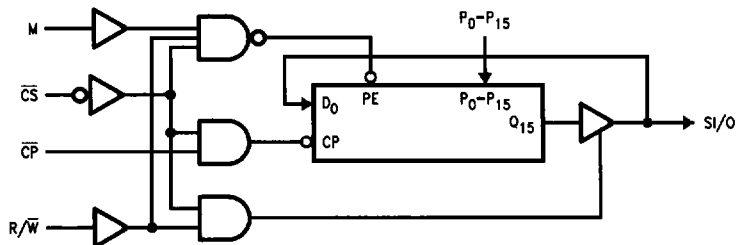
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

\sim = HIGH-to-LOW Transition

Block Diagram



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