

# Octal D-type transparent latch with 5-volt tolerant inputs/outputs; 3-state

## 74LVC373A 74LVCH373A

### FEATURES

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 2.7 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0$  V
- Bushold on all data inputs (LVCH373A only).

### DESCRIPTION

The 74LVC(H)373A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC(H)373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches. The '373' is functionally identical to the '573', but the '573' has different pin arrangement.

### QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$ ; LE to $Q_n$	$C_L = 50$ pF $V_{CC} = 3.3$ V	4.3 4.6	ns
$C_i$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per latch	notes 1 and 2	20	pF

### Notes to the quick reference data

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
2. The condition is  $V_i = GND$  to  $V_{CC}$ .

### ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)373AD	20	SO	plastic	SOT163-1
74LVC(H)373ADB	20	SSOP	plastic	SOT339-1
74LVC(H)373APW	20	TSSOP	plastic	SOT360-1

### PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$Q_0$ to $Q_7$	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	$D_0$ to $D_7$	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	$V_{CC}$	positive supply voltage

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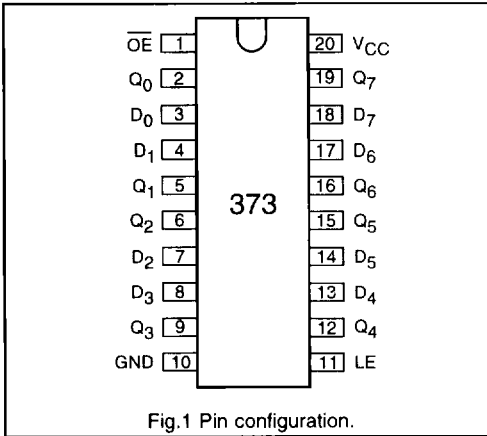


Fig.1 Pin configuration.

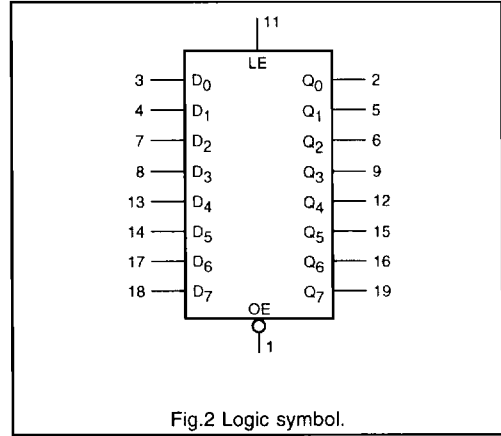


Fig.2 Logic symbol.

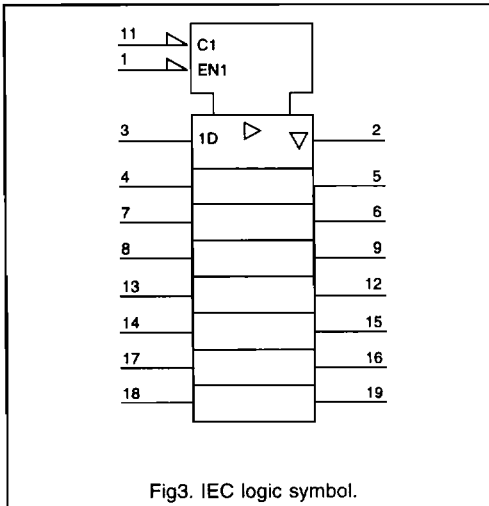


Fig.3. IEC logic symbol.

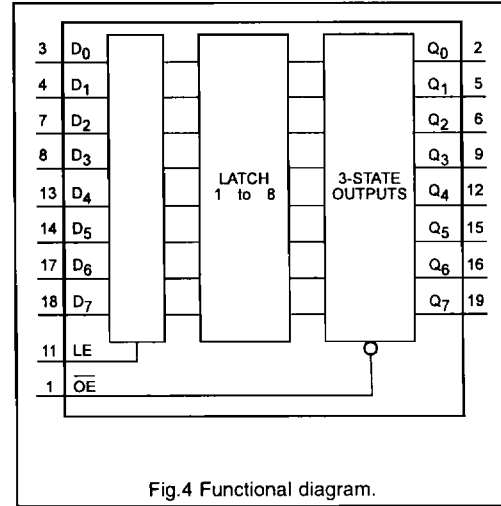


Fig.4 Functional diagram.

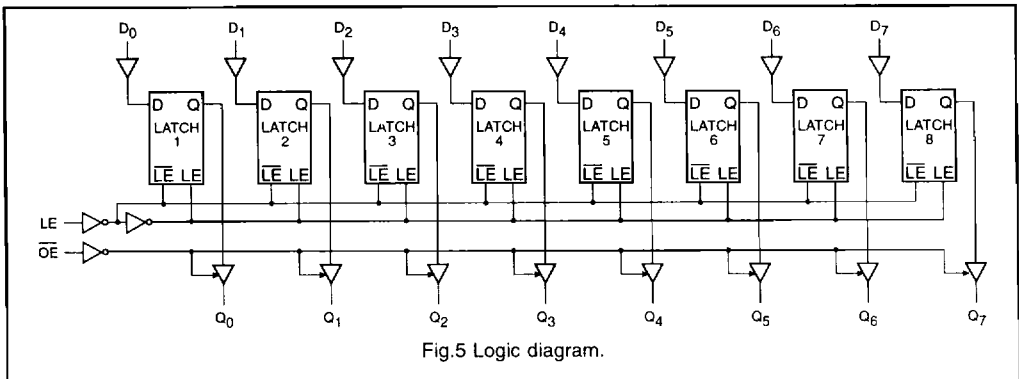


Fig.5 Logic diagram.

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## FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS Q <sub>0</sub> to Q <sub>7</sub>
	$\overline{OE}$	LE	D <sub>n</sub>		
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

X = don't care

Z = high impedance OFF-state

## DC CHARACTERISTICS FOR 74LVC(H)373A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

## AC CHARACTERISTICS FOR 74LVC(H)373A

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V <sub>CC</sub> (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>	- 1.5 1.5	- - -	- 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 10
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>	- 1.5 1.5	- - -	- 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 10
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Q <sub>n</sub>	- 1.5 1.5	- - -	- 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 8, 10
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Q <sub>n</sub>	- 1.5 1.5	- - -	- 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Figs 8, 10
t <sub>w</sub>	LE pulse width HIGH	4.0 4.0	- -	- -	ns	2.7 3.0 to 3.6	Fig.7
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	3.0 2.0	- -	- -	ns	2.7 3.0 to 3.6	Fig.9
t <sub>h</sub>	hold time D <sub>n</sub> to LE	3.0 2.0	- -	- -	ns	2.7 3.0 to 3.6	Fig.9

**Notes:** All typical values are measured at T<sub>amb</sub> = 25 °C.\* Typical values are measured at V<sub>CC</sub> = 3.3 V.

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AC WAVEFORMS

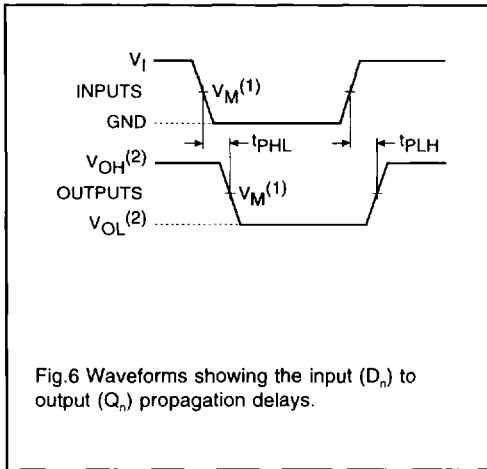


Fig.6 Waveforms showing the input ( $D_n$ ) to output ( $Q_n$ ) propagation delays.

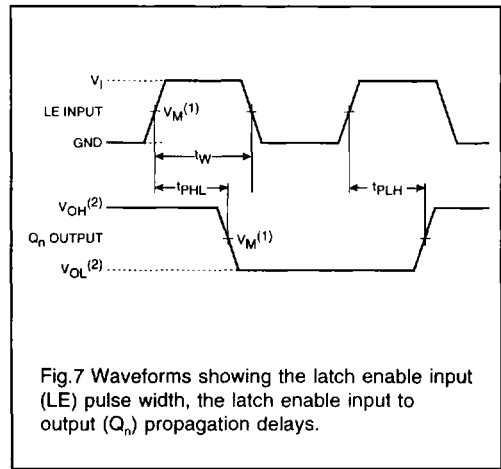


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ( $Q_n$ ) propagation delays.

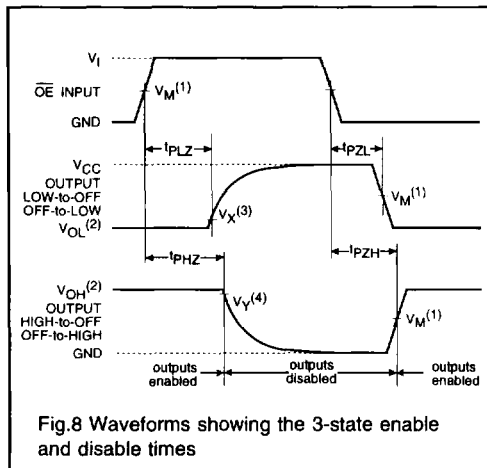


Fig.8 Waveforms showing the 3-state enable and disable times

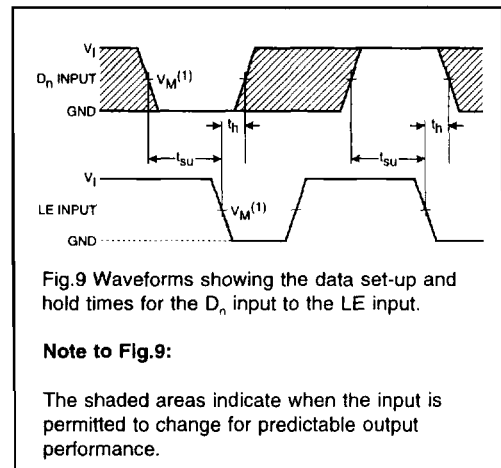


Fig.9 Waveforms showing the data set-up and hold times for the  $D_n$  input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

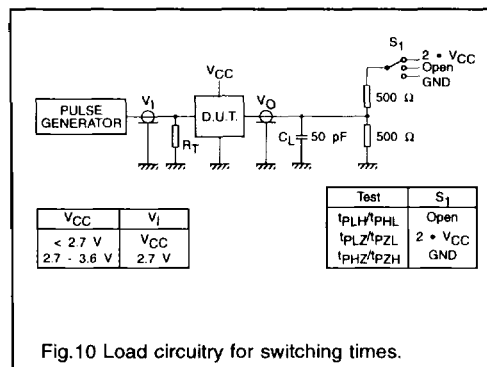


Fig.10 Load circuitry for switching times.

- Notes:
- (1)  $V_M = 1.5$  V at  $V_{CC} \geq 2.7$  V  
 $V_M = 0.5 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V
  - (2)  $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load
  - (3)  $V_X = V_{OL} + 0.3$  V at  $V_{CC} \geq 2.7$  V  
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V
  - (4)  $V_Y = V_{OH} - 0.3$  V at  $V_{CC} \geq 2.7$  V  
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V