DATA SHEET

74LV175

Quad D-type flip-flop with reset; positive-edge trigger

Philips
Semiconductors

PHILIPS

Quad D-type flip-flop with reset; positive-edge trigger

74LV175

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25°C$
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25°C$
- Four edge-triggered D flip-flops
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV175 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT175.

The 74LV175 has four edge-triggered, D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25°C$; $t_r = t_f \le 2.5$ ns

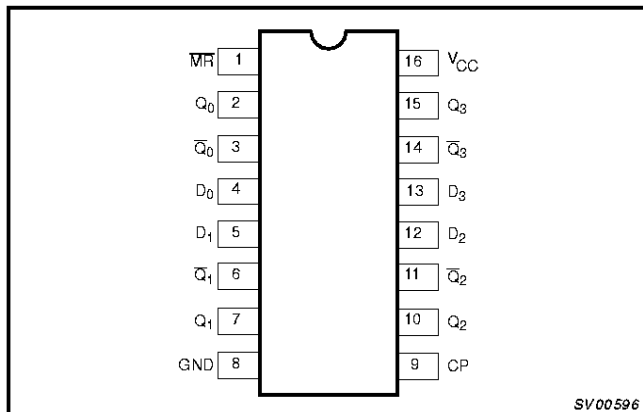| SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n, $\overline{Q}_n$ $\overline{MR}$ to Q_n, $\overline{Q}_n$	$C_L = 15$ pF; $V_{CC} = 3.3$ V	16 14	ns ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	$V_{CC} = 3.3$ V $V_I = $ GND to V_{CC}[1]	32	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; C_L = output load capacity in pF;

f_o = output frequency in MHz; V_{CC} = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

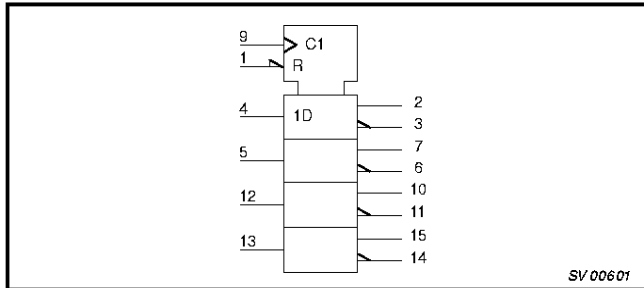| PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV175 N	74LV175 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV175 D	74LV175 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV175 DB	74LV175 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV175 PW	74LV175PW DH	SOT403-1

PIN CONFIGURATION

```
        ___
 MR  1 |   | 16  V_CC
 Q0  2 |   | 15  Q3
~Q0  3 |   | 14  ~Q3
 D0  4 |   | 13  D3
 D1  5 |   | 12  D2
~Q1  6 |   | 11  ~Q2
 Q1  7 |   | 10  Q2
GND  8 |___|  9  CP

SV00596
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PIN DESCRIPTION

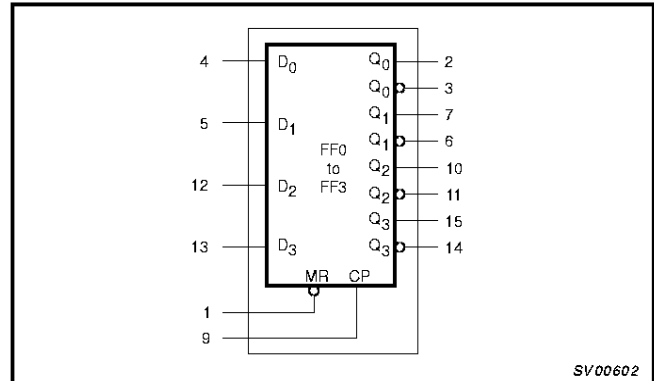| PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Master reset input (active LOW)
2, 7, 10, 15	Q_0 to Q_3	Flip-flop outputs
3, 6, 11, 14	$\overline{Q}_0$ to $\overline{Q}_3$	Complementary flip-flop outputs
4, 5, 12, 13	D_0 to D_3	Data inputs
8	GND	Ground (0 V)
9	CP	Clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	Positive supply voltage

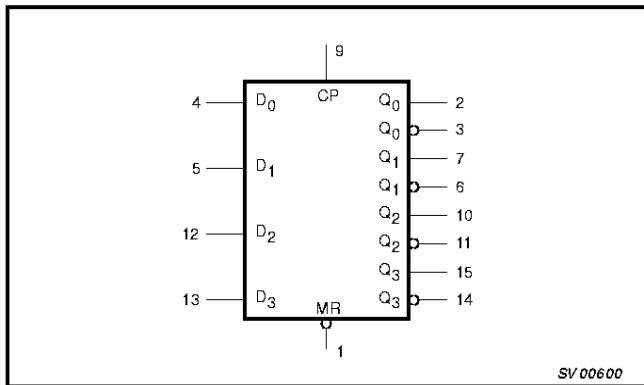# Quad D-type flip-flop with reset; positive-edge trigger

74LV175

LOGIC SYMBOL (IEEE/IEC)

LOGIC SYMBOL
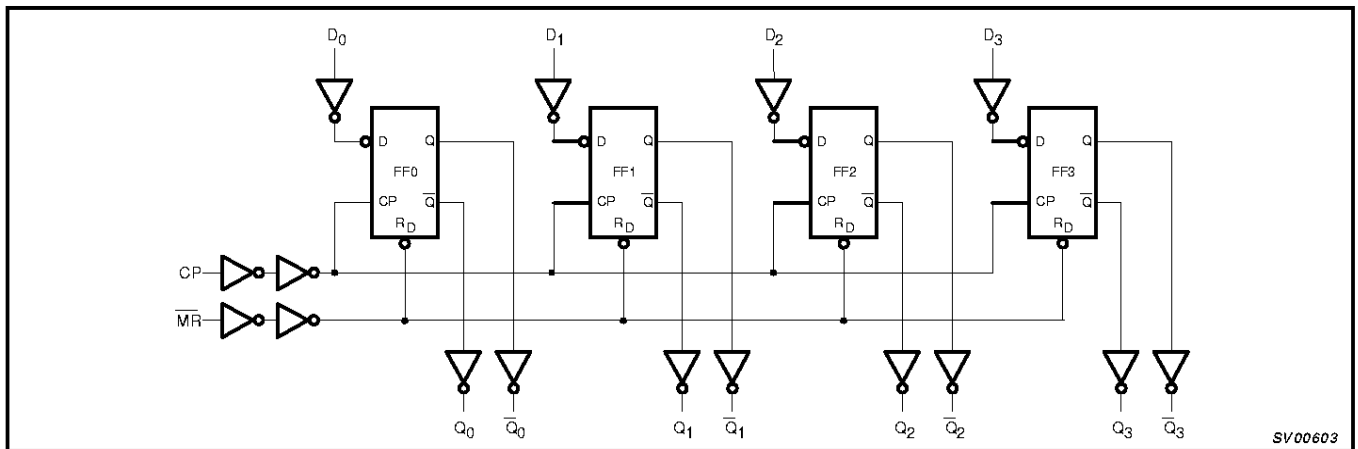
FUNCTIONAL DIAGRAM

LOGIC DIAGRAM

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load '1'	H	↑	h	H	L
Load '0'	H	↑	l	L	H

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition
X = don't care

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
± I_{IK}	DC input diode current	V_I < −0.5 or V_I > V_{CC} + 0.5V	20	mA
± I_{OK}	DC output diode current	V_O < −0.5 or V_O > V_{CC} + 0.5V	50	mA
± I_O	DC output source or sink current – standard outputs – bus driver outputs	−0.5V < V_O < V_{CC} + 0.5V	25 35	mA
± I_{GND}, ± I_{CC}	DC V_{CC} or GND current for types with – standard outputs – bus driver outputs		50 70	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2V$	V_{CC}	0.6		V_{CC}		V
		$V_{CC} = 2.0V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6V$	2.0			2.0		
		$V_{CC} = 4.5$ to $5.5V$	$0.7 * V_{CC}$			$0.7 * V_{CC}$		
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2V$		0.4	GND		GND	V
		$V_{CC} = 2.0V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6V$			0.8		0.8	
		$V_{CC} = 4.5$ to 5.5			$0.3 * V_{CC}$		$0.3 * V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.8	3.0		2.8		
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 6mA$	2.40	2.82		2.20		V
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 12mA$	3.60	4.20		3.50		
V_{OH}	HIGH level output voltage; BUS driver outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 8mA$	2.40	2.82		2.20		V
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 16mA$	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 6mA$		0.25	0.40		0.50	V
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 12mA$		0.35	0.55		0.65	
V_{OL}	LOW level output voltage; BUS driver outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 8mA$		0.20	0.40		0.50	V
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 16mA$		0.35	0.55		0.65	
I_I	Input leakage current	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{OZ}	3-State output OFF-state current	$V_{CC} = 5.5V; V_I = V_{IH}$ or $V_{IL}; V_O = V_{CC}$ or GND			5		10	μA
I_{CC}	Quiescent supply current; SSI	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		40	μA
	Quiescent supply current; flip-flops	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		80	
	Quiescent supply current; MSI	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		160	μA
	Quiescent supply current; LSI	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND; $I_O = 0$			500		1000	
ΔI_{CC}	Additional quiescent supply current per input	$V_{CC} = 2.7V$ to $3.6V; V_I = V_{CC} - 0.6V$			500		850	μA

NOTE:
1. All typical values are measured at $T_{amb} = 25°C$.

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AC CHARACTERISTICS

$GND = 0V$; $t_r = t_f = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION $V_{CC}(V)$	LIMITS −40 to +85 °C MIN	TYP[1]	MAX	−40 to +125 °C MIN	MAX	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n, $\overline{Q}_n$	Figures 1, 4	1.2		100				ns
			2.0		34	65		77	
			2.7		25	48		56	
			3.0 to 3.6		19²	38		45	
t_{PHL}/t_{PLH}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	Figures 2, 4	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17²	34		41	
t_w	Clock pulse width HIGH or LOW	Figures 1	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8²		24		
t_w	Master reset pulse width LOW	Figures 2	2.0	34	14		41		ns
			2.7	25	9		30		
			3.0 to 3.6	20	7²		24		
t_{rem}	Removal time $\overline{MR}$ to CP	Figures 2	1.2		−60				ns
			2.0	5	−20		5		
			2.7	5	−15		5		
			3.0 to 3.6	5	−12²		5		
t_{su}	Set-up time D_n to CP	Figures 3	1.2		5				ns
			2.0	22	2		26		
			2.7	16	2		19		
			3.0 to 3.6	13	1²		15		
t_h	Hold time D_n to CP	Figures 3	1.2		−5				ns
			2.0	5	−1		5		
			2.7	5	0		5		
			3.0 to 3.6	5	0²		5		
f_{max}	Maximum clock pulse frequency	Figures 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70²		20		

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$.
2. Typical values are measured at $V_{CC} = 3.3$ V.

Quad D-type flip-flop with reset; positive-edge trigger

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V;
$V_M = 0.5$ V × V_{CC} at $V_{CC} < 2.7$ V.
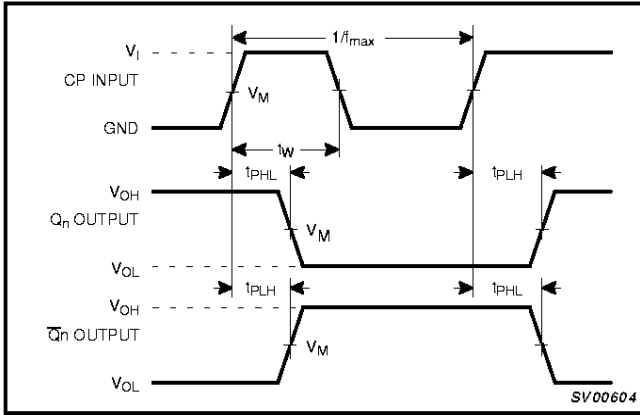V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Figure 1. Clock (CP) to outputs (Q_n, $\overline{Q}_n$) propagation delays, the clock pulse width and the maximum clock pulse frequency.
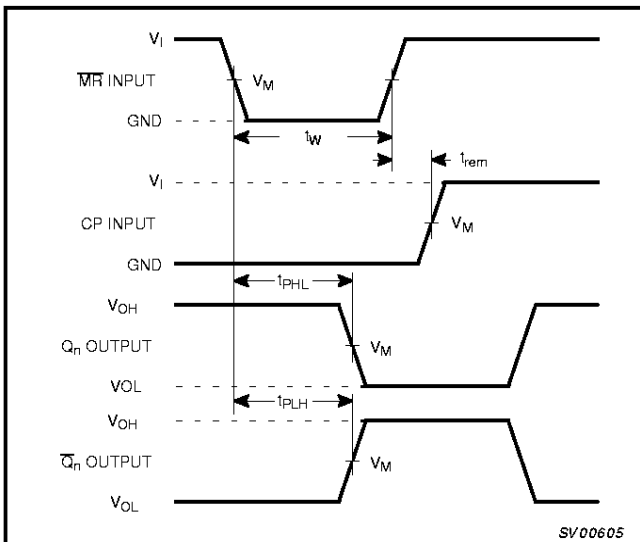

Figure 2. Master reset ($\overline{MR}$) pulse width, the master reset to outputs (Q_n, $\overline{Q}_n$) propagation delay and master reset to clock (CP) removal time.
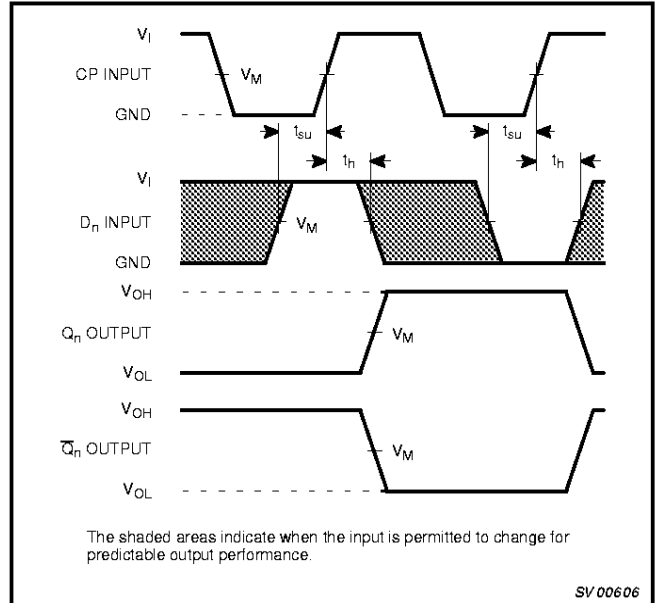

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. Data set-up and hold times for data input (D_n).

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TEST CIRCUIT

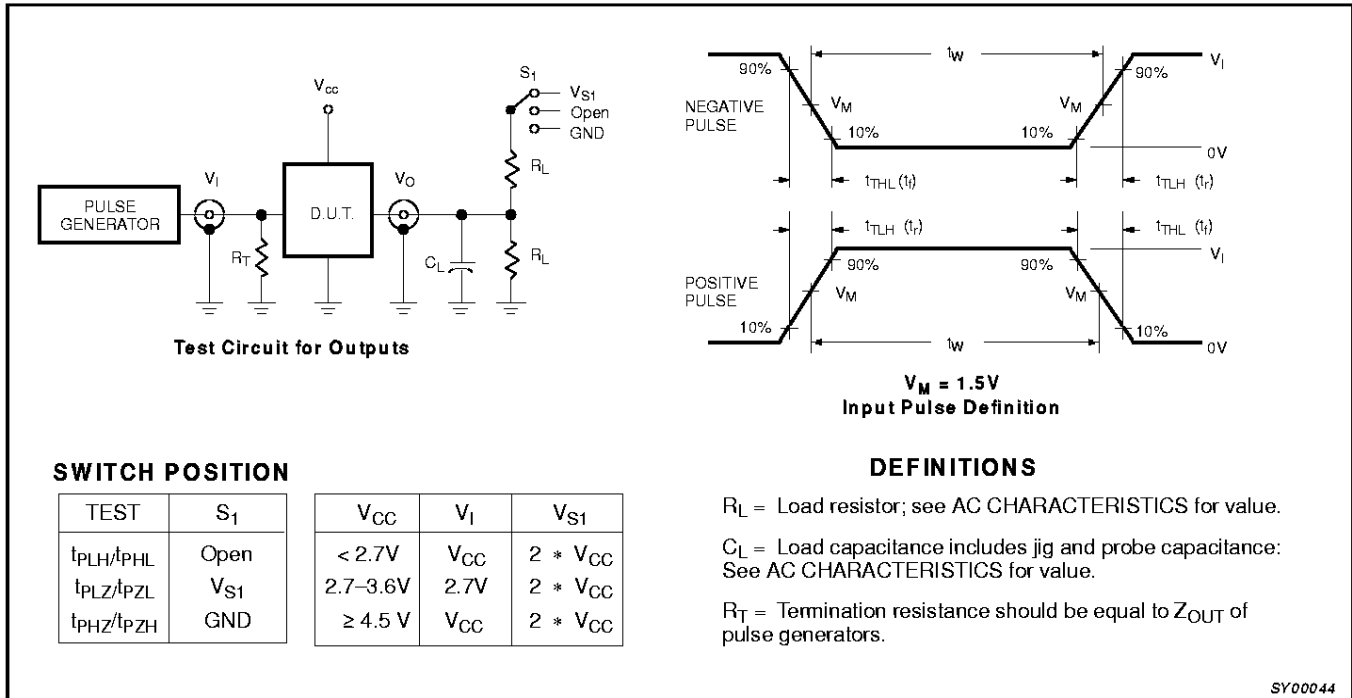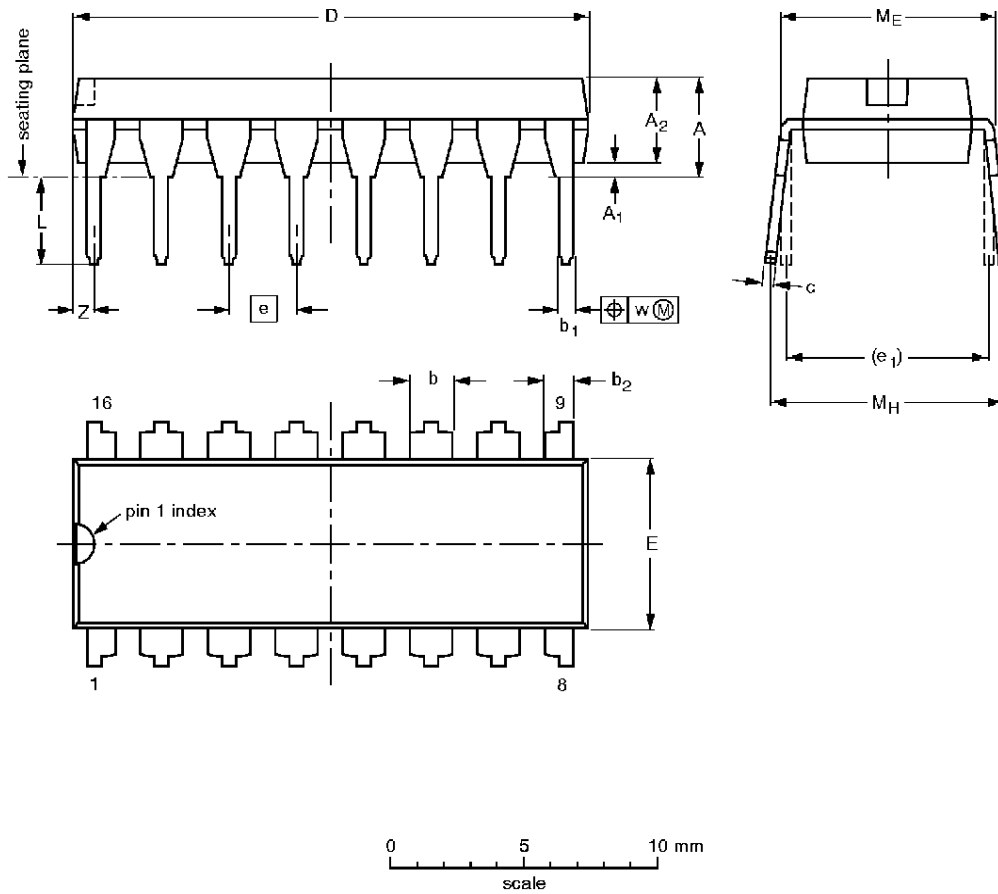

Test Circuit for Outputs

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	$2 * V_{CC}$
2.7–3.6V	2.7V	$2 * V_{CC}$
≥ 4.5 V	V_{CC}	$2 * V_{CC}$

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Figure 4. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil)   **SOT38-4**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$ min.	A$_2$ max.	b	b$_1$	b$_2$	c	D [1]	E [1]	e	e$_1$	L	M$_E$	M$_H$	w	z [1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

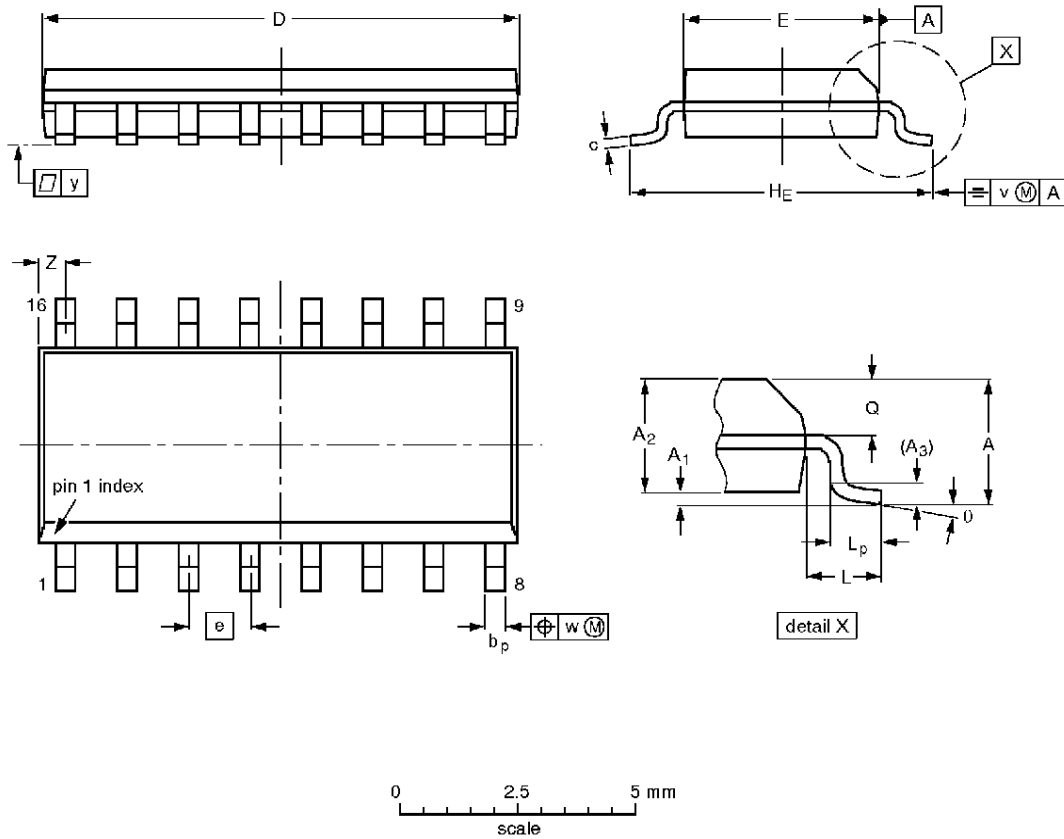1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16:   plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

pin 1 index

detail X

```
0        2.5        5 mm
└─┴─┴─┴─┴─┴─┴─┴─┴─┴─┘
        scale
```

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D⁽¹⁾	E⁽¹⁾	e	Hₑ	L	Lₚ	Q	v	w	y	Z⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

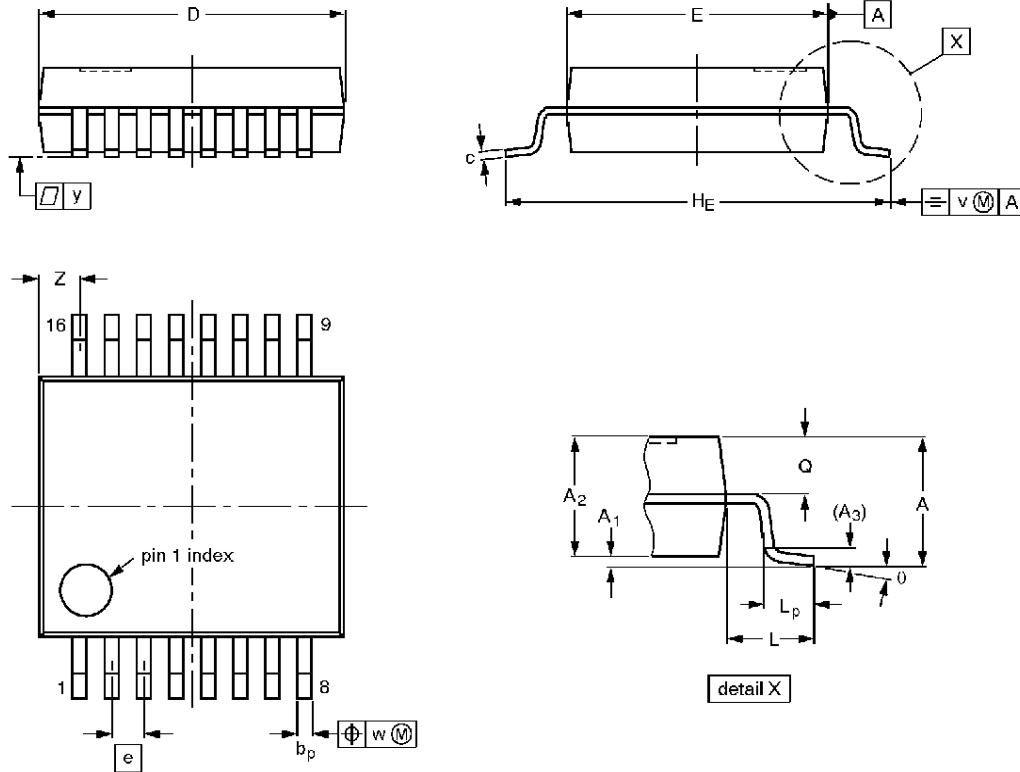1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

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SSOP16:   plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

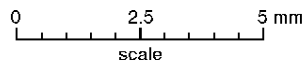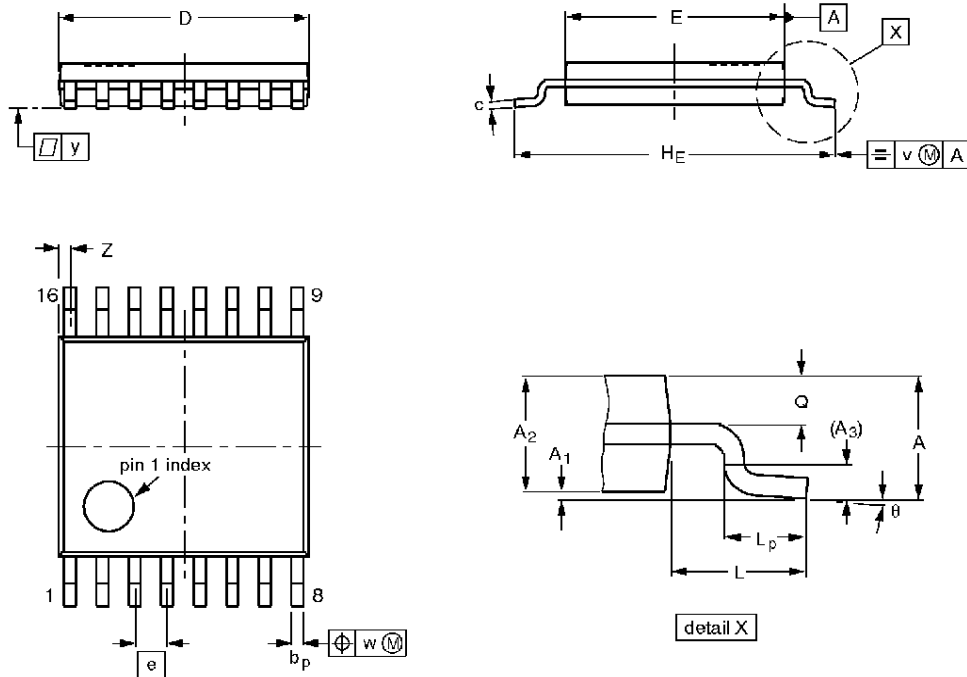1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**

detail X

```
0        2.5        5 mm
|--|--|--|--|--|
      scale
```

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
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