

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

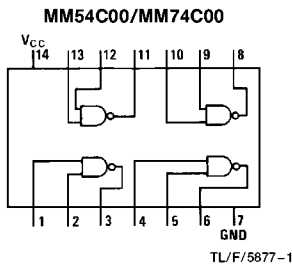
General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

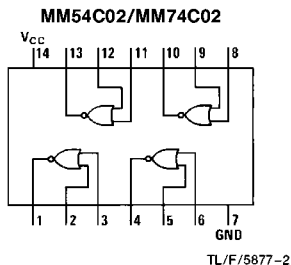
Features

- Wide supply voltage range 3V to 15V
- Guaranteed noise margin 1V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power consumption 10 nW/package (typ.)
- Low power Fan out of 2
- TTL compatibility driving 74L

Connection Diagrams
Dual-In-Line Packages


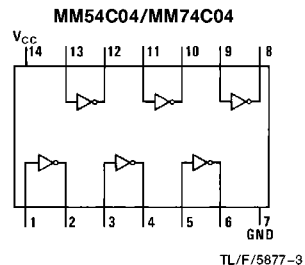
Top View

Order Number MM54C00 or
MM74C00



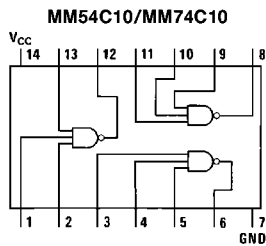
Top View

Order Number MM54C02 or
MM74C02



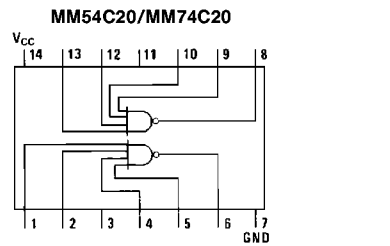
Top View

Order Number MM54C04
or MM74C04



Top View

Order Number MM54C10 or
MM74C10



Top View

Order Number MM54C20 or
MM74C20

MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04, MM54C10/MM74C10, MM54C20/MM74C20

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------|--------------------------|
| Voltage at Any Pin | -0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range | |
| 54C | -55°C to +125°C |
| 74C | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |

| | |
|---|-------------|
| Operating V_{CC} Range | 3.0V to 15V |
| Maximum V_{CC} Voltage | 18V |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|----------------------------|---|----------------|--------|-----|---------|
| CMOS TO CMOS | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5.0V$ | 3.5 | | | V |
| | | $V_{CC} = 10V$ | 8.0 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5.0V$ | | | 1.5 | V |
| | | $V_{CC} = 10V$ | | | 2.0 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5.0V, I_O = -10 \mu A$ | 4.5 | | | V |
| | | $V_{CC} = 10V, I_O = -10 \mu A$ | 9.0 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5.0V, I_O = 10 \mu A$ | | | 0.5 | V |
| | | $V_{CC} = 10V, I_O = 10 \mu A$ | | | 1.0 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V, V_{IN} = 15V$ | | 0.005 | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V, V_{IN} = 0V$ | -1.0 | -0.005 | | μA |
| I_{CC} | Supply Current | $V_{CC} = 15V$ | | 0.01 | 15 | μA |
| LOW POWER TO CMOS | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C, $V_{CC} = 4.5V$ | $V_{CC} - 1.5$ | | | V |
| | | 74C, $V_{CC} = 4.75V$ | $V_{CC} - 1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C, $V_{CC} = 4.5V$ | | | 0.8 | V |
| | | 74C, $V_{CC} = 4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C, $V_{CC} = 4.5V, I_O = -10 \mu A$ | 4.4 | | | V |
| | | 74C, $V_{CC} = 4.75V, I_O = -10 \mu A$ | 4.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C, $V_{CC} = 4.5V, I_O = 10 \mu A$ | | | 0.4 | V |
| | | 74C, $V_{CC} = 4.75V, I_O = 10 \mu A$ | | | 0.4 | V |
| CMOS TO LOW POWER | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C, $V_{CC} = 4.5V$ | 4.0 | | | V |
| | | 74C, $V_{CC} = 4.75V$ | 4.0 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C, $V_{CC} = 4.5V$ | | | 1.0 | V |
| | | 74C, $V_{CC} = 4.75V$ | | | 1.0 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C, $V_{CC} = 4.5V, I_O = -360 \mu A$ | 2.4 | | | V |
| | | 74C, $V_{CC} = 4.75V, I_O = -360 \mu A$ | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C, $V_{CC} = 4.5V, I_O = 360 \mu A$ | | | 0.4 | V |
| | | 74C, $V_{CC} = 4.75V, I_O = 360 \mu A$ | | | 0.4 | V |
| OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25^\circ C$ (short circuit current) | | | | | | |
| I_{SOURCE} | Output Source Current | $V_{CC} = 5.0V, V_{IN(0)} = 0V, V_{OUT} = 0V$ | -1.75 | | | mA |
| I_{SOURCE} | Output Source Current | $V_{CC} = 10V, V_{IN(0)} = 0V, V_{OUT} = 0V$ | -8.0 | | | mA |
| I_{SINK} | Output Sink Current | $V_{CC} = 5.0V, V_{IN(1)} = 5.0V, V_{OUT} = V_{CC}$ | 1.75 | | | mA |
| I_{SINK} | Output Sink Current | $V_{CC} = 10V, V_{IN(1)} = 10V, V_{OUT} = V_{CC}$ | 8.0 | | | mA |

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|--|-------------------------------|-----|-----|-----|-------|
| MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04 | | | | | | |
| t_{pd0} , t_{pd1} | Propagation Delay Time to Logical "1" or "0" | $V_{CC} = 5.0\text{V}$ | | 50 | 90 | ns |
| | | $V_{CC} = 10\text{V}$ | | 30 | 60 | ns |
| C_{IN} | Input Capacitance | (Note 2) | | 6.0 | | pF |
| C_{PD} | Power Dissipation Capacitance | (Note 3) Per Gate or Inverter | | 12 | | pF |
| MM54C10/MM74C10 | | | | | | |
| t_{pd0} , t_{pd1} | Propagation Delay Time to Logical "1" or "0" | $V_{CC} = 5.0\text{V}$ | | 60 | 100 | ns |
| | | $V_{CC} = 10\text{V}$ | | 35 | 70 | ns |
| C_{IN} | Input Capacitance | (Note 2) | | 7.0 | | pF |
| C_{PD} | Power Dissipation Capacitance | (Note 3) Per Gate | | 18 | | pF |
| MM54C20/MM74C20 | | | | | | |
| t_{pd0} , t_{pd1} | Propagation Delay Time to Logical "1" or "0" | $V_{CC} = 5.0\text{V}$ | | 70 | 115 | ns |
| | | $V_{CC} = 10\text{V}$ | | 40 | 80 | ns |
| C_{IN} | Input Capacitance | (Note 2) | | 9 | | pF |
| C_{PD} | Power Dissipation Capacitance | (Note 3) Per Gate | | 30 | | pF |

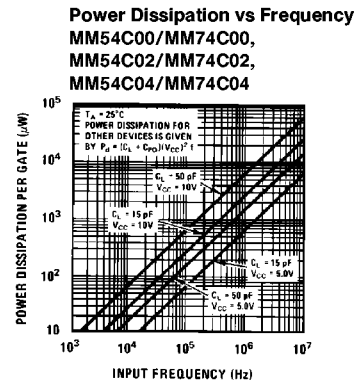
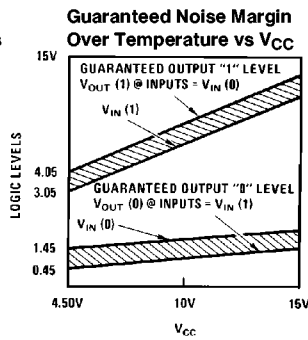
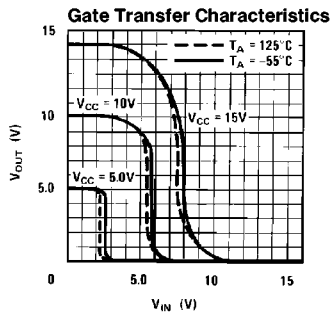
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

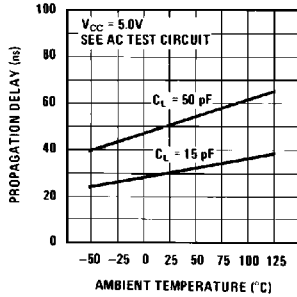
Typical Performance Characteristics



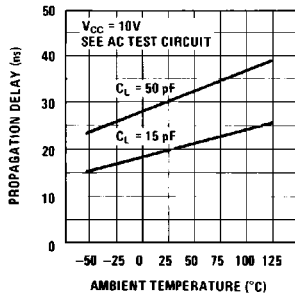
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Typical Performance Characteristics (Continued)

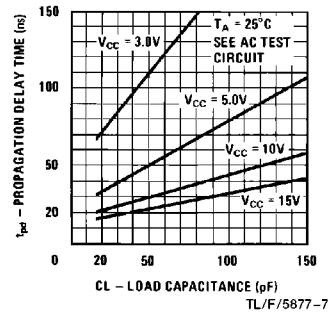
Propagation Delay vs Ambient Temperature
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04



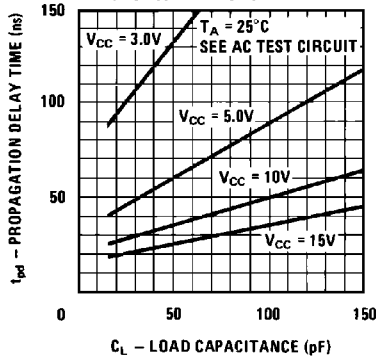
Propagation Delay vs Ambient Temperature
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04



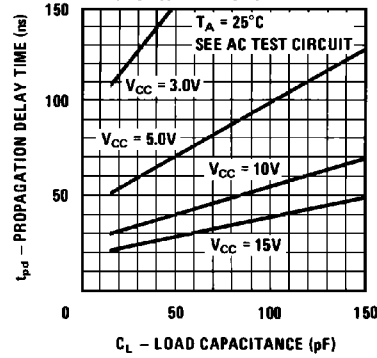
Propagation Delay Time vs Load Capacitance
MM54C00/MM74C00,
MM54C02/MM74C02,
MM54C04/MM74C04



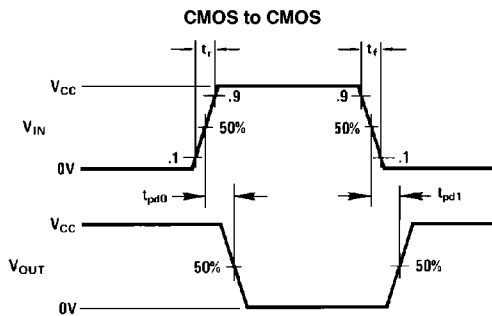
Propagation Delay Time vs Load Capacitance
MM54C10/MM74C10



Propagation Delay Time vs Load Capacitance
MM54C20/MM74C20

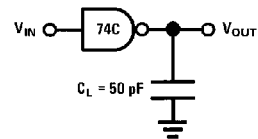


Switching Time Waveforms and AC Test Circuit



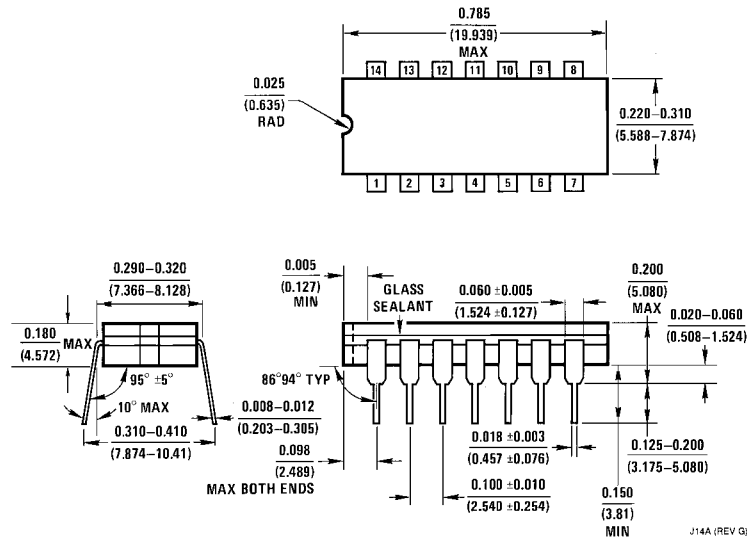
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Note: Delays measured with input $t_r, t_f \leq 20\text{ ns}$.



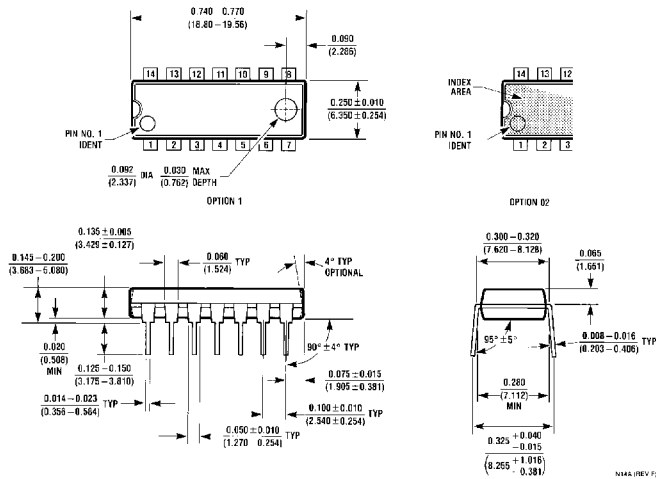
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Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C00J, MM54C02J, MM54C04J, MM54C10J, MM54C20J,
MM74C00J, MM74C02J, MM74C04J, MM74C10J or MM74C20J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM54C00N, MM54C02N, MM54C04N, MM54C10N, MM54C20N,
MM74C00N, MM74C02N, MM74C04N, MM74C10N or MM74C20N
NS Package Number N14A

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