

SN54ACT08, SN74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCAS535A – SEPTEMBER 1995 – REVISED APRIL 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPS

description

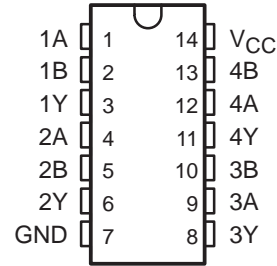
The 'ACT08 are quadruple 2-input positive-AND gates. These devices perform the Boolean functions $Y = A \bullet B$ or $Y = \bar{A} + \bar{B}$ in positive logic.

The SN54ACT08 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ACT08 is characterized for operation from -40°C to 85°C .

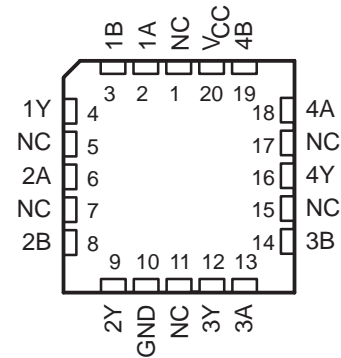
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SN54ACT08 . . . J OR W PACKAGE
SN74ACT08 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)

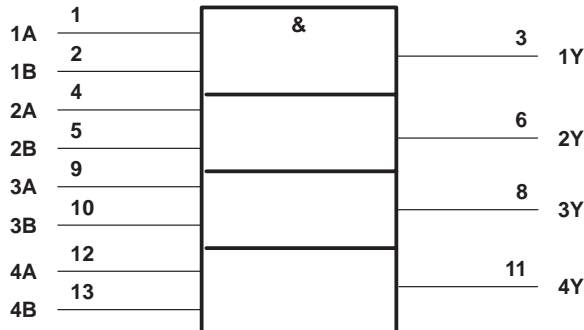


SN54ACT08 . . . FK PACKAGE
(TOP VIEW)

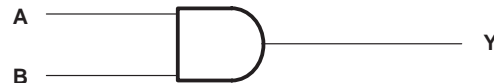


NC – No internal connection

logic symbol†



logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.



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**TEXAS
INSTRUMENTS**

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SN54ACT08, SN74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB package	0.5 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

	SN54ACT08		SN74ACT08		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		-24		-24	mA
I_{OL} Low-level output current		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	8	0	8	ns/V
T_A Operating free-air temperature	-55	125	-40	85	$^\circ\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SN54ACT08, SN74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT08		SN74ACT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = - 50 μA	4.5 V	4.4	4.49		4.4		4.4	V	
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OH} = - 24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
I _{OH} = - 75 mA [†]	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	4.5 V		0.001	0.1		0.1	0.1	V	
		5.5 V		0.001	0.1		0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I _{OL} = 50 mA [†]	5.5 V					1.65			
I _{OL} = 75 mA [†]	5.5 V						1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		80	20	μA	
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.6		1.6	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V			4.5				pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54ACT08		SN74ACT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	1	6.5	9	1	10	1	10	ns
t _{PHL}			1	6.5	9	1	10	1	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

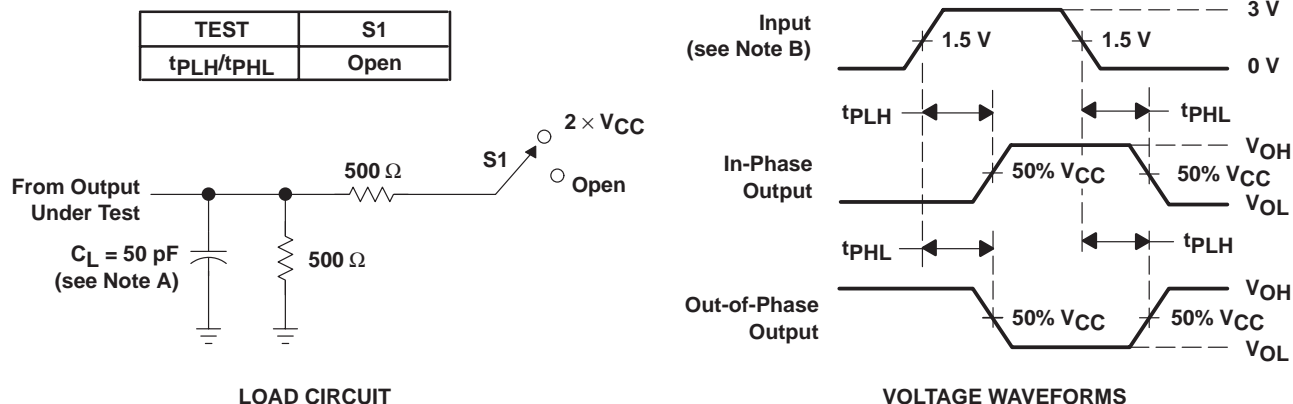
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	20	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN54ACT08, Quadruple 2-Input Positive-AND Gates

Device Status: Active

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- > [Features](#)
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- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
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Parameter Name	SN54ACT08
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	CMOS
No. of Gates	4

Description

The 'ACT08 are quadruple 2-input positive-AND gates. These devices perform the Boolean functions $Y = A \oplus B$ or $Y = A \downarrow B$ in positive logic.

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Features

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Datasheets

Full datasheet in Acrobat PDF: [scas535a.pdf](#) (79 KB)

Full datasheet in Zipped PostScript: [scas535a.psz](#) (75 KB)

Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
SNJ54ACT08FK	<u>FK</u>	20	-55 TO 125	ACTIVE	10.27	1	5962-89547022A	Check stock or order
SNJ54ACT08J	<u>J</u>	14	-55 TO 125	ACTIVE	2.84	1	5962-8954702CA	Check stock or order
SNJ54ACT08W	<u>W</u>	14	-55 TO 125	ACTIVE	10.27	1	5962-8954702DA	Check stock or order

Application Reports

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- [CMOS Power Consumption And CPD Calculation \(SCAA035B - Updated: 06/01/1997\)](#)
- [Designing With Logic \(SDYA009C - Updated: 06/01/1997\)](#)
- [Implications Of Slow Or Floating CMOS Inputs \(SCBA004C - Updated: 02/01/1998\)](#)
- [Using High Speed CMOS And Advanced CMOS In Systems With Multiple Vcc \(SCLA008 - Updated: 04/01/1996\)](#)

Related Documents

- [Documentation Rules \(SAP\) And Ordering Information \(SZZU001B, 4 KB - Updated: 05/06/1999\)](#)
- [Logic Selection Guide Second Half 2000 \(SDYU001N, 5035 KB - Updated: 04/17/2000\)](#)
- [MicroStar Junior BGA Design Summary \(SCET004, 284 KB - Updated: 07/28/2000\)](#)
- [More Power In Less Space - Technical Article \(SCAU001A, 850 KB - Updated: 03/01/1996\)](#)

Table Data Updated on: 9/1/2000