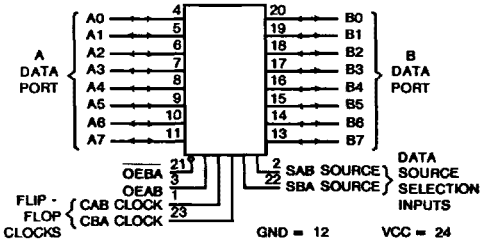
CD54/74FCT651, CD54/74FCT651AT
CD54/74FCT652, CD54/74FCT652AT

July 1990



CD54/74FCT652, 652AT FUNCTIONAL DIAGRAM

Octal Bus Transceivers/ Registers, 3-State

CD54/74FCT651, CD54/74FCT651AT - Inverting
CD54/74FCT652, CD54/74FCT652AT - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6.8ns @ VCC = 5V, TA = 25°C, CL = 50pF (FCT651, FCT652)*

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXX - Speed of bipolar FAST*/AS/S; FCTXXXAT - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *64/48-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

The CD54/74FCT651, 651AT, 652 and 652AT 3-state, octal bus transceivers/registers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enchances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and $\overline{OEBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54/74FCT651, 651AT, 652 and 652AT are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT651 and 652 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

* FAST is a registered trademark of Fairchild Semiconductor Corp.

4 TECHNICAL DATA

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD54/74FCT651, 651AT	CD54/74FCT652, 652AT
L L	H H	H or L ↓	H or L ↓	X X	X X	Input Input	Input Input	Isolation * Store A and B Data	Isolation * Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X‡	X X	Input Input	Unspecified † Output	Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers
L L	X L	H or L ↓	↓ ↓	X X	X X‡	Unspecified † Output	Input Input	Hold A, Store B Stored B in both registers	Hold, A Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output Output	Input Input	Real-Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input Input	Output Output	Real-Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus Stored B Data to A Bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 528mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

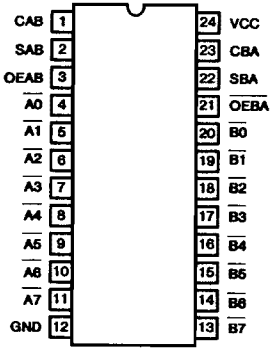
FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, −55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	−55°C to +125°C MIN	−55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	−15	MIN	2.4	-	2.4	-	-	-	V
		VIL	−12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	64	MIN	-	0.55	-	0.55	-	-	V
		VIL	48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	−18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

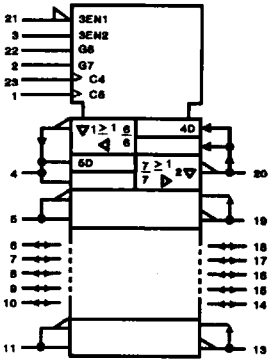
* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

CD54/74FCT651, CD54/74FCT651AT TYPES

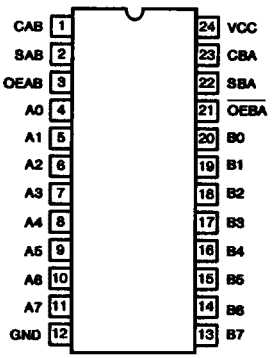


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT652, CD54/74FCT652AT TYPES



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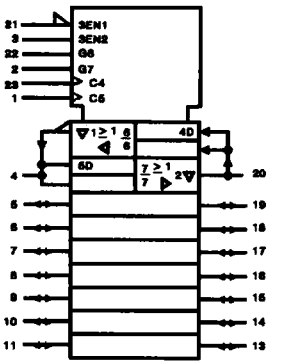


IEC LOGIC SYMBOL

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT651, 652 AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	CD54/74FCT651AT, 652AT AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Maximum Frequency	fMAX	5†	-	85	-	85	-					-	MHz
Data to Clock Setup Time	tSU	5		4	-	4.5	-					-	ns
Data to Clock Hold Time	tH	5		2	-	2	-					-	ns
Clock Pulse Width	tW	5		6	-	6	-			-		-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

SWITCHING CHARACTERISTICS

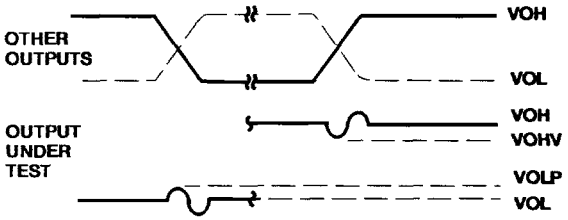
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	VCC (V)	CD54/74FCT651, 652 AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	CD54/74FCT651AT, 652AT AMBIENT TEMPERATURE (T_A) +25°C TYP	0°C to +70°C MIN	0°C to +70°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNITS
Propagation Delays: Store $\overline{An}$ → Bn, Store $\overline{Bn}$ → An	FCT651/AT	tPLH, tPHL	5†	6.8	2	9	2	11						ns
Store An → Bn, Store Bn → An	FCT652/AT	tPLH, tPHL	5	6.8	2	9	2	11						ns
$\overline{An}$ → Bn, $\overline{Bn}$ → An	FCT651/AT	tPLH, tPHL	5	6.8	2	9	2	10						ns
An → Bn, Bn → An	FCT652/AT	tPLH, tPHL	5	6.8	2	9	2	10						ns
Select to Data	FCT651/AT, FCT652/AT	tPLH, tPHL	5	8.3	2	11	2	12						ns
3-State Enabling Time Bus to Output or Register to Output	FCT651/AT	tPZL, tPZH	5	7.5	2	10	2	12						ns
	FCT652/AT	tPZL, tPZH	5	7.5	2	10	2	12						ns
3-State Disabling Time Bus to Output or Register to Output	FCT651/AT	tPLZ, tPHZ	5	7.5	2	10	2	12						ns
	FCT652/AT	tPLZ, tPHZ	5	7.5	2	10	2	12						ns
Power Dissipation Capacitance		CPD§	-											pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Figure 1	5	0.5 Typical @ +25°C										V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Figure 1	5	1 Typical @ +25°C										V
Input Capacitance		CI	-	-	-	10	-	10	-	-	10	-	10	pF
Input/Output Capacitance		$C_{I/O}$	-	-	-	15	-	15	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

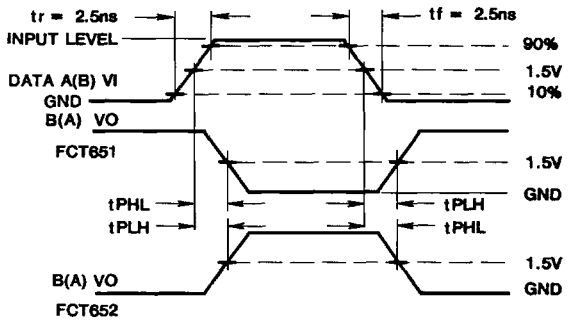


Figure 2 - Propagation delay times.

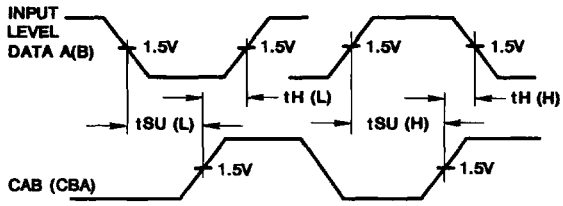
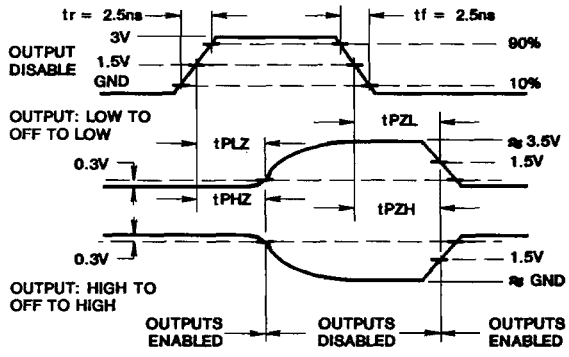
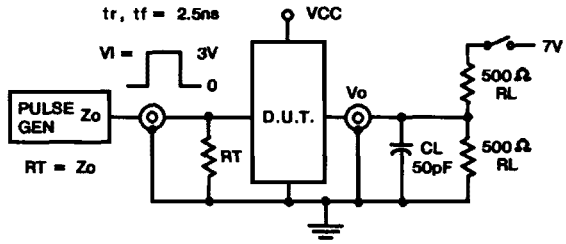


Figure 3 - Data setup and hold times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.