

74VHC4066

Quad Analog Switch

General Description

These devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the '4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The '4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are pro-

tected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μ A maximum (74VHC)
- Matched switch characteristics
- Individual switch controls
- Pin and function compatible with the 74HC4066

Ordering Code: See Section 6

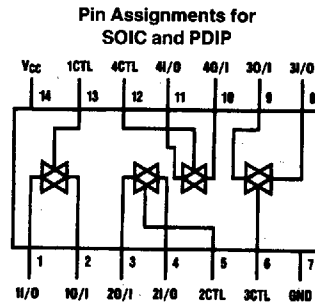
Commercial	Package Number	Package Description
74VHC4066M	M14A	14-Lead Molded JEDEC SOIC (.150" Wide)
74VHC4066WM	M14B	14-Lead Molded JEDEC SOIC (.300" Wide)
74VHC4066N	N14A	14-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

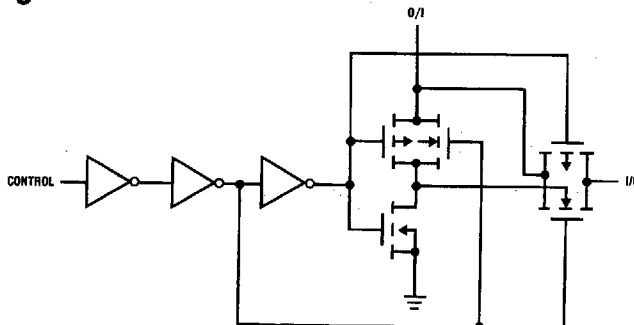
Connection Diagram



Top View

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Schematic Diagram



TL/F/11677-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	-0.5 to +15V
DC Control Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Switch I/O Voltage (V_{IO})	$V_{EE} - 0.5$ to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) 74VHC	-40	+85	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 9.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74VHC $T_A = -40$ to $85^\circ C$		Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V	
			4.5V		3.15	3.15	V	
			9.0V		6.3	5.3	V	
			12.0V		8.4	8.4	V	
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.5	0.5	V	
			4.5V		1.35	1.35	V	
			9.0V		2.7	2.7	V	
			12.0V		3.6	3.6	V	
R_{ON}	Maximum "ON" Resistance (See Note 5)	$V_{CTL} = V_{IH}, I_S = 2.0$ mA $V_{IS} = V_{CC}$ to GND (Figure 1)	4.5V	100	170	200	Ω	
			9.0V	50	85	105	Ω	
			12.0V	30	70	85	Ω	
		$V_{CTL} = V_{IH}, I_S = 2.0$ mA $V_{IS} = V_{CC}$ or GND (Figure 1)	2.0V	120	180	215	Ω	
			4.5V	50	80	100	Ω	
			9.0V	35	60	75	Ω	
12.0V	20	40	60	Ω				
R_{ON}	Maximum "ON" Resistance Matching	$V_{CTL} = V_{IH}$ $V_{IS} = V_{CC}$ to GND	4.5V	10	15	20	Ω	
			9.0V	5	10	15	Ω	
			12.0V	5	10	15	Ω	
I_{IN}	Maximum Control Input Current	$V_{IN} = V_{CC}$ or GND $V_{CC} = 2-6V$			± 0.05	± 0.5	μA	
I_{IZ}	Maximum Switch "OFF" Leakage Current	$V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ or V_{CC} $V_{CTL} = V_{IL}$ (Figure 2)	6.0V	10	± 60	± 600	nA	
			9.0V	15	± 80	± 800	nA	
			12.0V	20	± 100	± 1000	nA	
I_{IZ}	Maximum Switch "ON" Leakage Current	$V_{IS} = V_{CC}$ to GND $V_{CTL} = V_{IH}$ (Figure 3) $V_{OS} = OPEN$	6.0V	10	± 40	± 150	nA	
			9.0V	15	± 50	± 200	nA	
			12.0V	20	± 60	± 300	nA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		1.0	10	μA	
			9.0V		2.0	20	μA	
			12.0V		4.0	40	μA	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case on resistance (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages ($V_{CC}-GND$) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

$V_{CC} = 2.0V - 6.0V$ $V_{EE} = 0V - 12V$, $C_L = 50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74VHC		Units
						$T_A = -40$ to $85^\circ C$		
				Typ	Guaranteed Limits			
t_{PHL} , t_{PLH}	Maximum Propagation Delay Switch In to Out		3.3V	25	30	20	ns	
			4.5V	5	10	13	ns	
			9.0V	4	8	10	ns	
			12.0V	3	7	11	ns	
t_{PZL} , t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L = 1$ k Ω	3.3V	30	58	73	ns	
			4.5V	12	20	25	ns	
			9.0V	6	12	15	ns	
			12.0V	5	10	13	ns	
t_{PHZ} , t_{PLZ}	Maximum Switch Turn "OFF" Delay	$R_L = 1$ k Ω	3.3V	60	100	125	ns	
			4.5V	25	36	45	ns	
			9.0V	20	32	40	ns	
			12.0V	15	30	38	ns	
	Minimum Frequency Response (Figure 7)	$R_L = 600\Omega$ $V_{IS} = 2$ V _{PP} at ($V_{CC}/2$) (Notes 6 & 7)	4.5V 9.0V	40 100			MHz MHz	
	Crosstalk Between any Two Switches (Figure 8)	$R_L = 600\Omega$, $F = 1$ MHz (Notes 7 & 8)	4.5V 9.0V	-52 -50			dB dB	
	Peak Control to Switch Feedthrough Noise (Figure 9)	$R_L = 600\Omega$, $F = 1$ MHz $C_L = 50$ pF	4.5V 9.0V	100 250			mV mV	
	Switch OFF Signal Feedthrough Isolation (Figure 10)	$R_L = 600\Omega$, $F = 1$ MHz $V_{(CT)} V_{IL}$ (Notes 7 & 8)	4.5V 9.0V	-42 -44			dB dB	
THD	Total Harmonic Distortion (Figure 11)	$R_L = 10$ k Ω , $C_L = 50$ pF, $F = 1$ kHz $V_{IS} = 4$ V _{PP} $V_{IS} = 8$ V _{PP}	4.5V 9.0V	.013 .008			% %	
C_{IN}	Maximum Control Input Capacitance			5	10	10	pF	
C_{IN}	Maximum Switch Input Capacitance			20			pF	
C_{IN}	Maximum Feedthrough Capacitance	$V_{CTL} = GND$		0.5			pF	
C_{PD}	Power Dissipation Capacitance			15			pF	

Note 6: Adjust 0 dBm for $F = 1$ kHz (Null R_L/R_{ON} Attenuation).

Note 7: V_{IS} is centered at $V_{CC}/2$.

Note 8: Adjust input for 0 dBm.

AC Test Circuits and Switching Time Waveforms

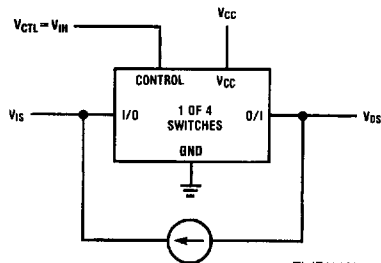


FIGURE 1. "ON" Resistance

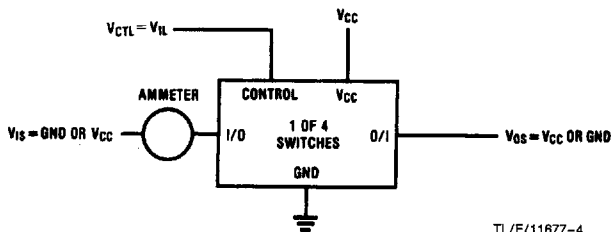


FIGURE 2. "OFF" Channel Leakage Current

AC Test Circuits and Switching Time Waveforms (Continued)

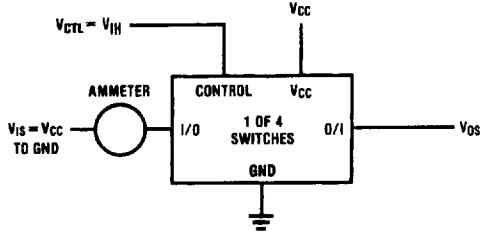


FIGURE 3. "ON" Channel Leakage Current

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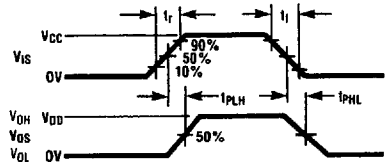
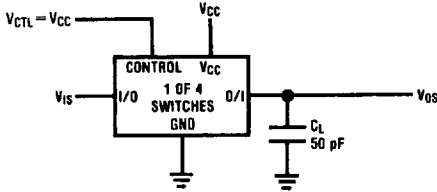


FIGURE 4. t_{PHL} , t_{PLH} Propagation Delay Time Signal Input to Signal Output

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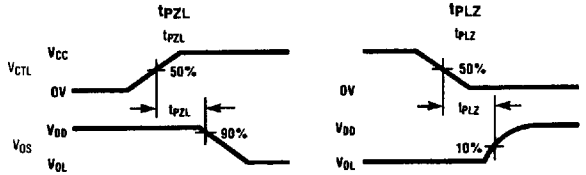
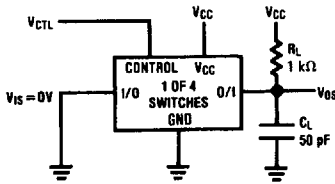


FIGURE 5. t_{PZL} , t_{PLZ} Propagation Delay Time Control to Signal Output

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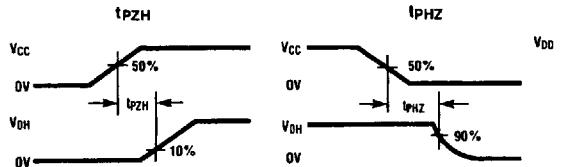
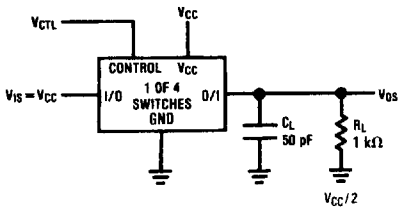


FIGURE 6. t_{PZH} , t_{PHZ} Propagation Delay Time Control to Signal Output

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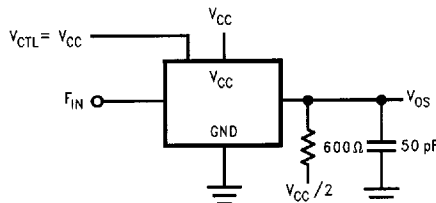


FIGURE 7. Frequency Response

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Crosstalk and Distortion Test Circuits

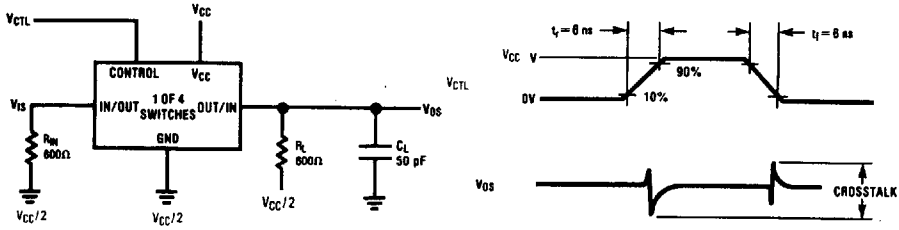


FIGURE 8. Crosstalk: Control Input to Signal Output

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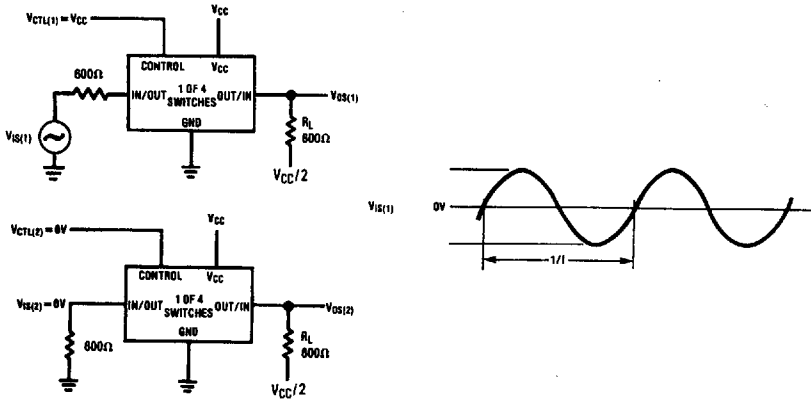


FIGURE 9. Crosstalk Between Any Two Switches

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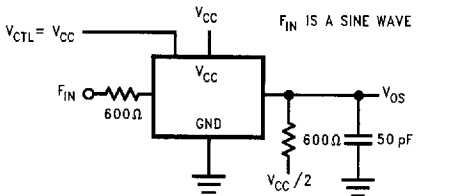


FIGURE 10. Switch OFF Signal Feedthrough Isolation

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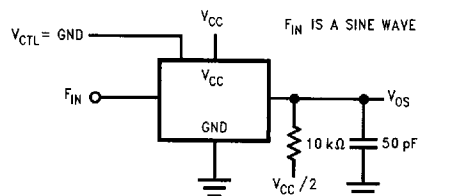
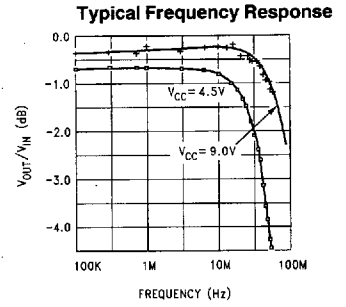
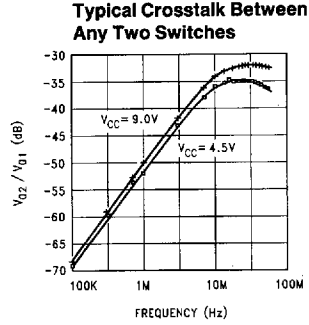
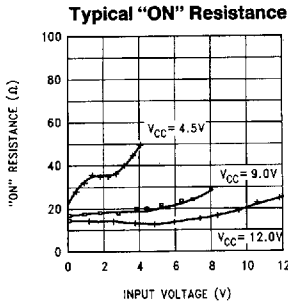


FIGURE 11. Sinewave Distortion

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Typical Performance Characteristics



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Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).