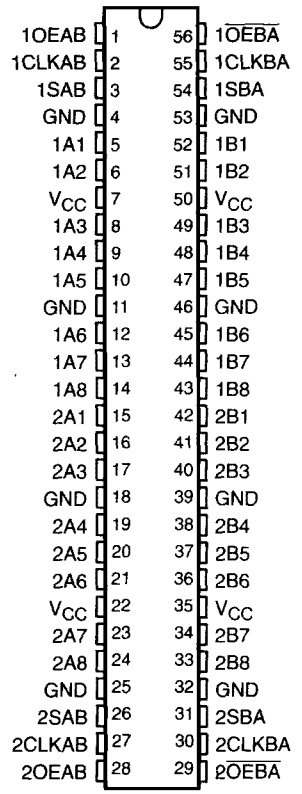
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16652 . . . WD PACKAGE
SN74LVT16652 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16652 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16652 is characterized for operation from −40°C to 85°C.

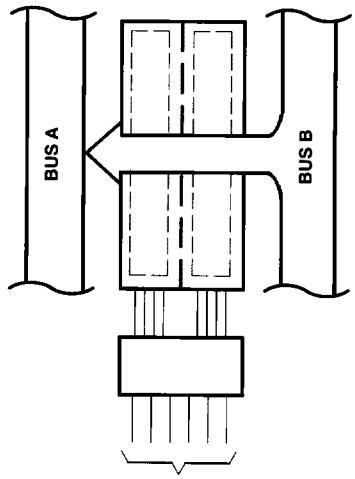
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

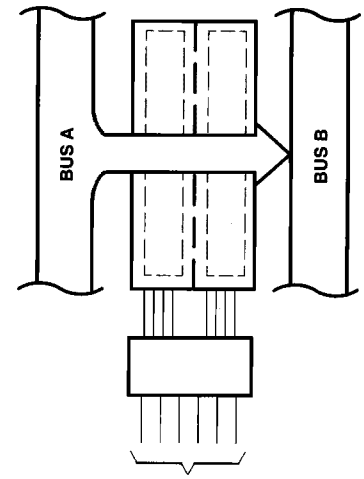
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



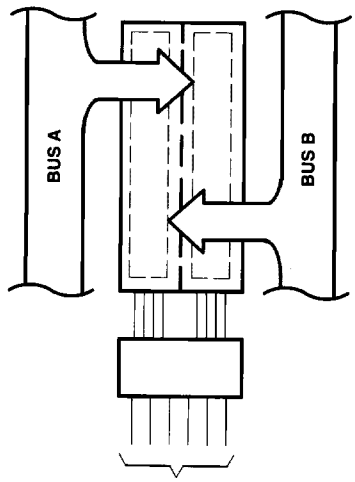
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



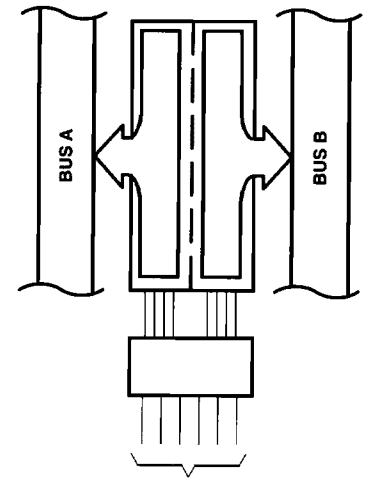
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

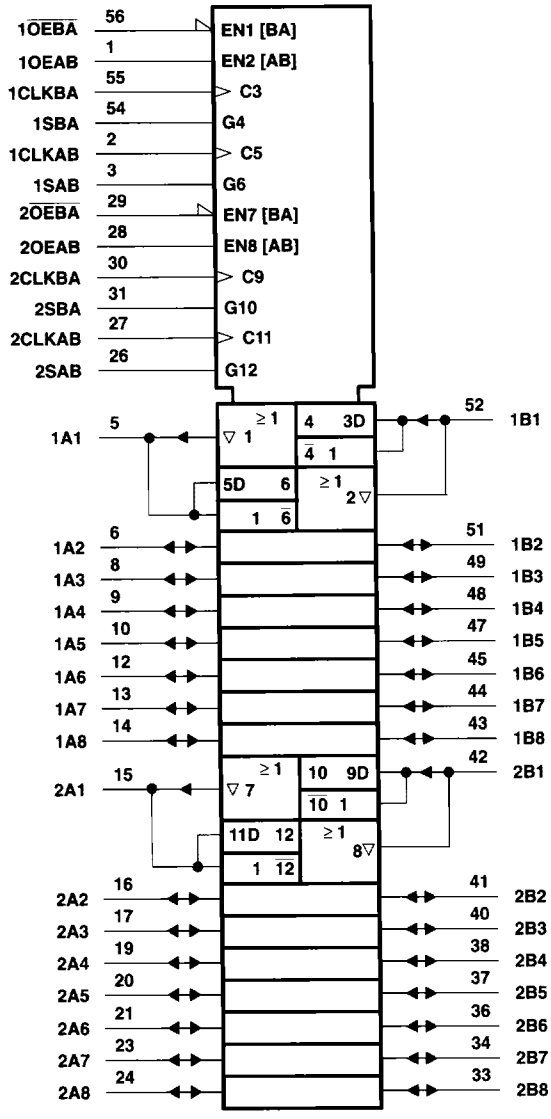
TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

PRODUCT PREVIEW

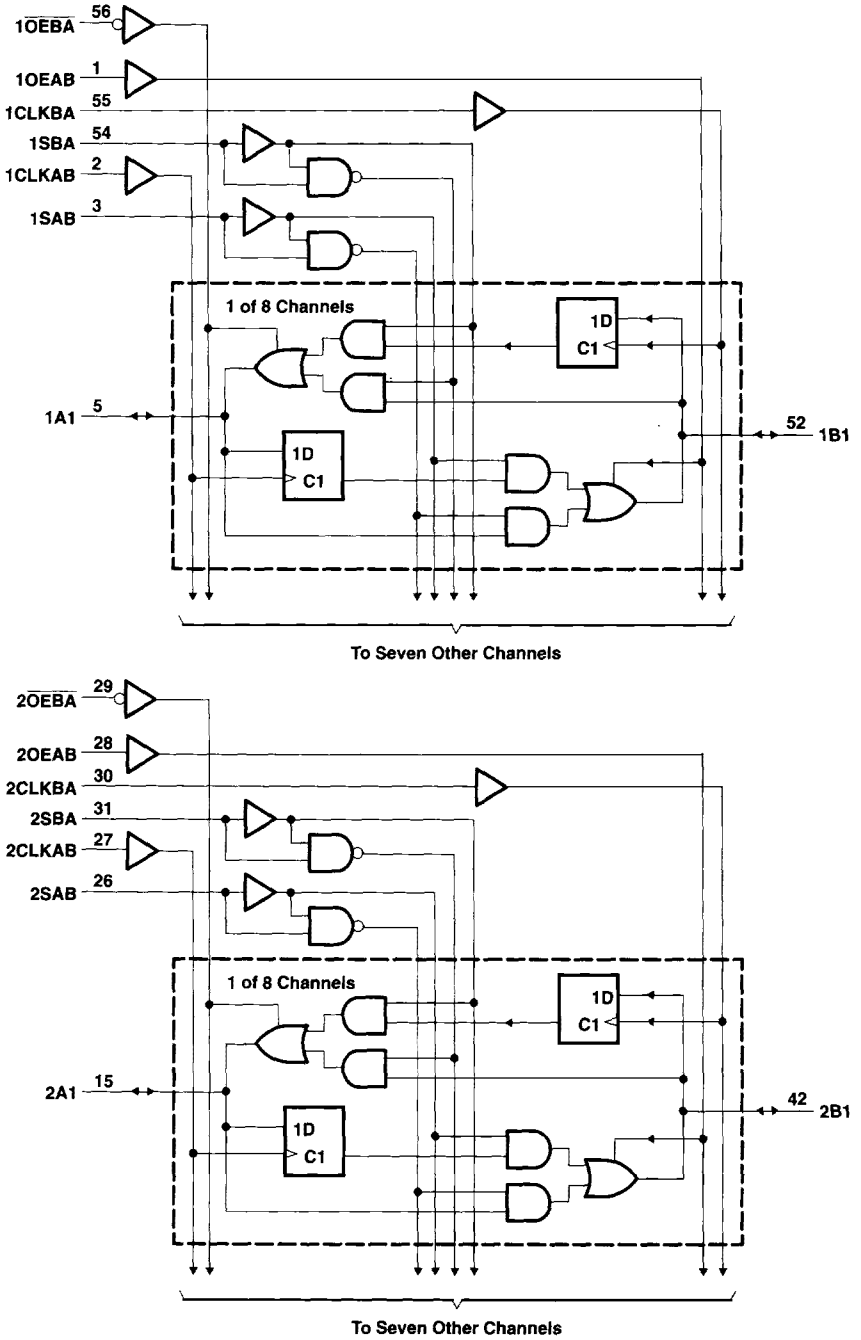
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16652 ..... 96 mA
SN74LVT16652 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16652 ..... 48 mA
SN74LVT16652 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT16652		SN74LVT16652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16652		SN74LVT16652		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2				
	V_{CC} = 3 V,	I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA			0.2		0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA			0.4		0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5		0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA			0.55			
	V_{CC} = 3 V,	I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V,	V_I = 5.5 V	A or B ports§		20		20	
	V_{CC} = 3.6 V,	V_I = V_{CC}			1		1	
	V_{CC} = 3.6 V,	V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW