



# HIGH-SPEED CMOS BUS INTERFACE 8-BIT LATCH

*IDTQS74FCT2373T/AT*

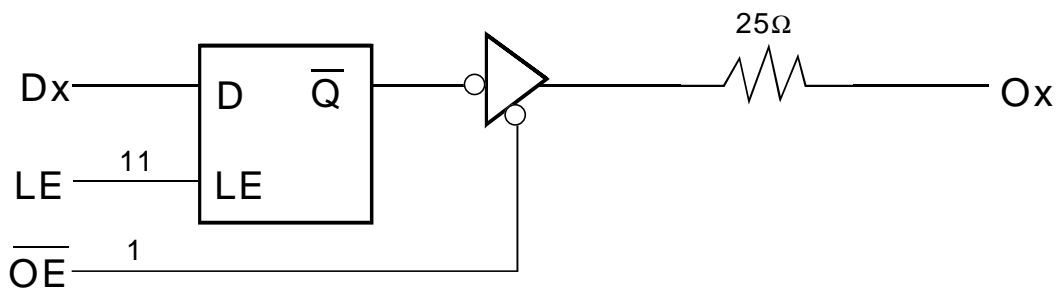
## FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. and A speed grades
- I<sub>OL</sub> = 12mA
- Available in SOIC and QSOP packages

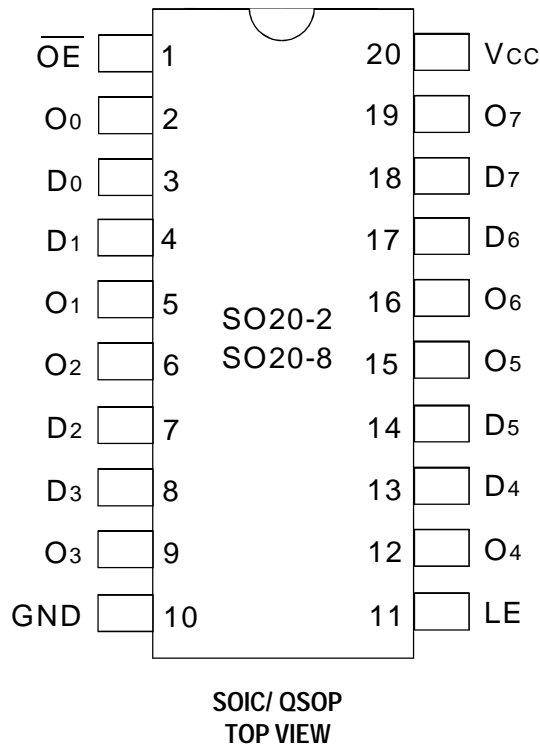
## DESCRIPTION:

The IDTQS74FCT2373T is an 8-bit high-speed CMOS TTL-compatible buffered latch, with three-state outputs that have 25Ω resistors at the output. This device is useful for driving transmission lines and reducing system noise. The 2373 series parts can replace the 373 series to reduce noise in existing designs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V<sub>CC</sub> is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	- 0.5 to +7	V
T <sub>STG</sub>	Storage Temperature	- 65 to +150	°C
I <sub>OUT</sub>	DC Output Current Max Sink Current/Pin	120	mA
I <sub>IK</sub>	Input Diode Current, V <sub>IN</sub> < 0	- 20	mA
I <sub>OK</sub>	Output Diode Current, V <sub>OUT</sub> < 0	- 50	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4	—	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	—	pF

**NOTE:**

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
Dx	I	Data Inputs
Ox	O	Data Outputs (3-State)
LE	I	Latch Enable Input (Active HIGH)
$\overline{OE}$	I	Output Enable Input (Active LOW)

## FUNCTION TABLE <sup>(1)</sup>

Inputs			Internal Q Value	Outputs Q <sub>x</sub>	Function
$\overline{OE}$	LE	Dx			
H	X	X	X	Z	Disable Outputs
L	L	X	H	H	Enable Outputs
L	L	X	L	L	
L	H	L	L	L	Pass Inputs
L	H	H	H	H	
L	L	X	Q	Q	Hold Prior Data

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
Q = Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{TTL}$ for all inputs		—	0.2	—	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} < V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current			—	—	$\pm 5$	$\mu\text{A}$
$I_{OZ}$	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OR}$	Current Drive	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(2)}$		50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(2)}$		—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	—	—	0.5	V
$R_{OUT}$	Output Resistance	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	20	28	40	$\Omega$

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
2. This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0	—	2	mA
$I_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

FCTL

### NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $I_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4.  $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_{CC} = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (\text{fCP}/2 + \text{fiNi})$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4\text{V}$ )  
 $\text{DH}$  = Duty Cycle for TTL Inputs High  
 $\text{NT}$  = Number of TTL Inputs at DH  
 $I_{CCD}$  = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)  
 $\text{fCP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $\text{fi}$  = Input Frequency  
 $\text{Ni}$  = Number of Inputs at fi  
 All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

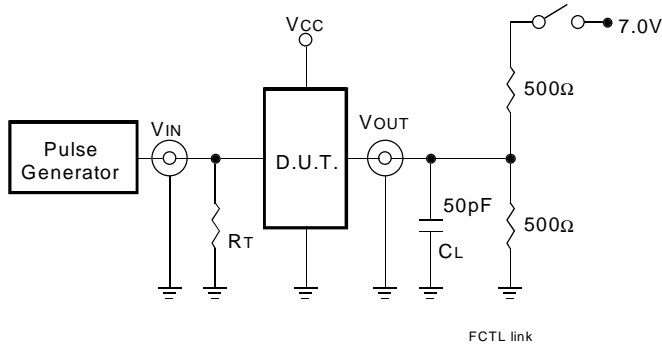
Symbol	Parameter <sup>(2)</sup>	74FCT2373T		74FCT2373AT		Unit
		Min.	Max.	Min.	Max.	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Data to O <sub>x</sub>	1.5	8	1.5	5.2	ns
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay LE to O <sub>x</sub>	2	13	2	8.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{\text{OE}}$ to Y <sub>x</sub>	1.5	11	1.5	6.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time <sup>(3)</sup> $\overline{\text{OE}}$ to Y <sub>x</sub>	1.5	7	1.5	5.5	ns
t <sub>s</sub>	Data Setup Time	2	—	2	—	ns
t <sub>H</sub>	Data hold Time	1.5	—	1.5	—	ns
t <sub>w</sub>	LE Pulse Width HIGH <sup>(3)</sup>	6	—	5	—	ns

### NOTES:

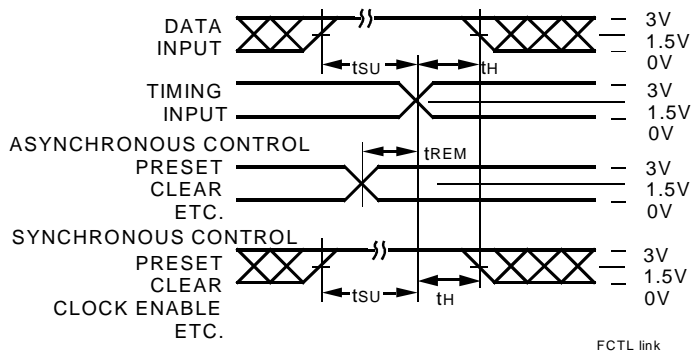
1. C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

## TEST CIRCUITS AND WAVEFORMS

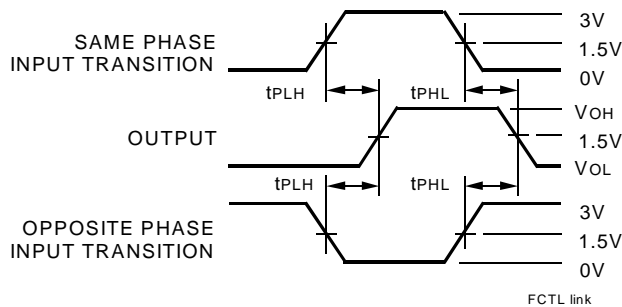
### TEST CIRCUITS FOR ALL OUTPUTS



### SET-UP, HOLD, AND RELEASE TIMES



### PROPAGATION DELAY



### SWITCH POSITION

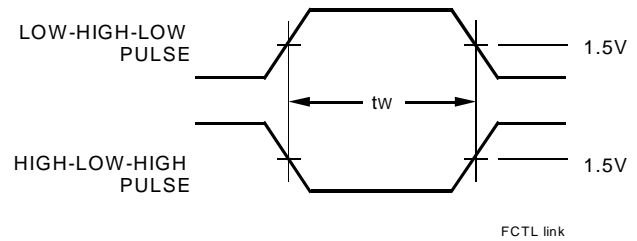
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

#### DEFINITIONS:

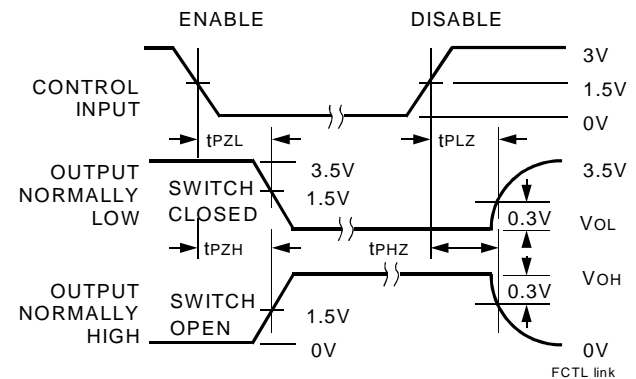
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

### PULSE WIDTH



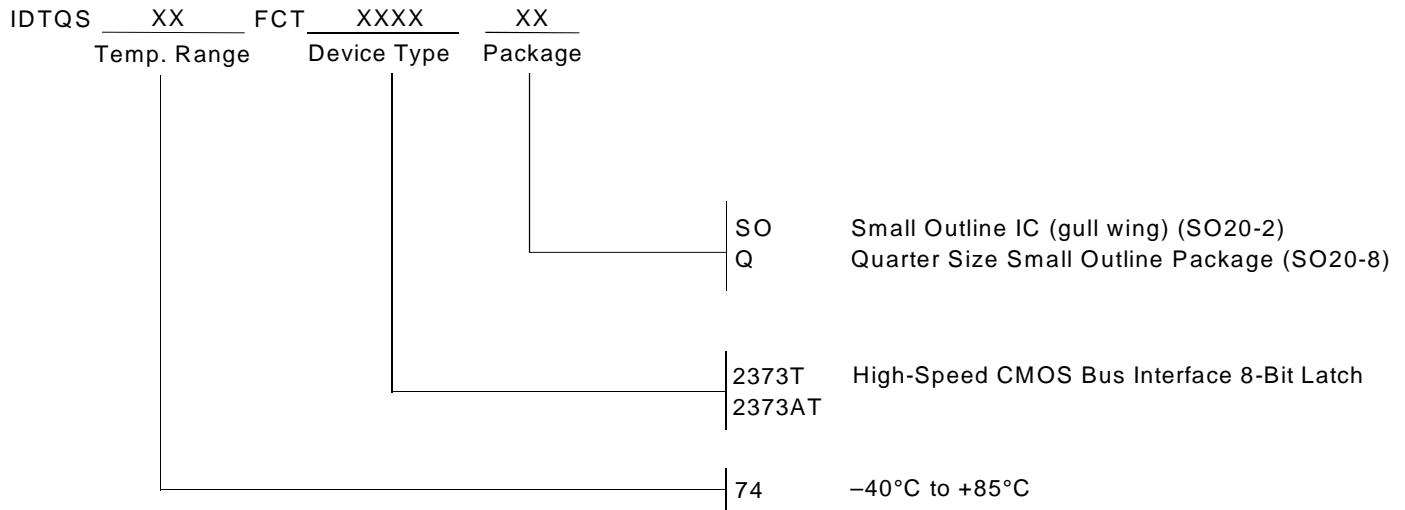
### ENABLE AND DISABLE TIMES



#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_f \leq$  2.5ns;  $t_r \leq$  2.5ns

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**

2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**

800-345-7015 or 408-727-6116  
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