



Integrated Device Technology, Inc.

3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, BUS-HOLD

IDT74ALVCH162543 ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP package
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH162543:

- Balanced Output Drivers: ±12mA
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

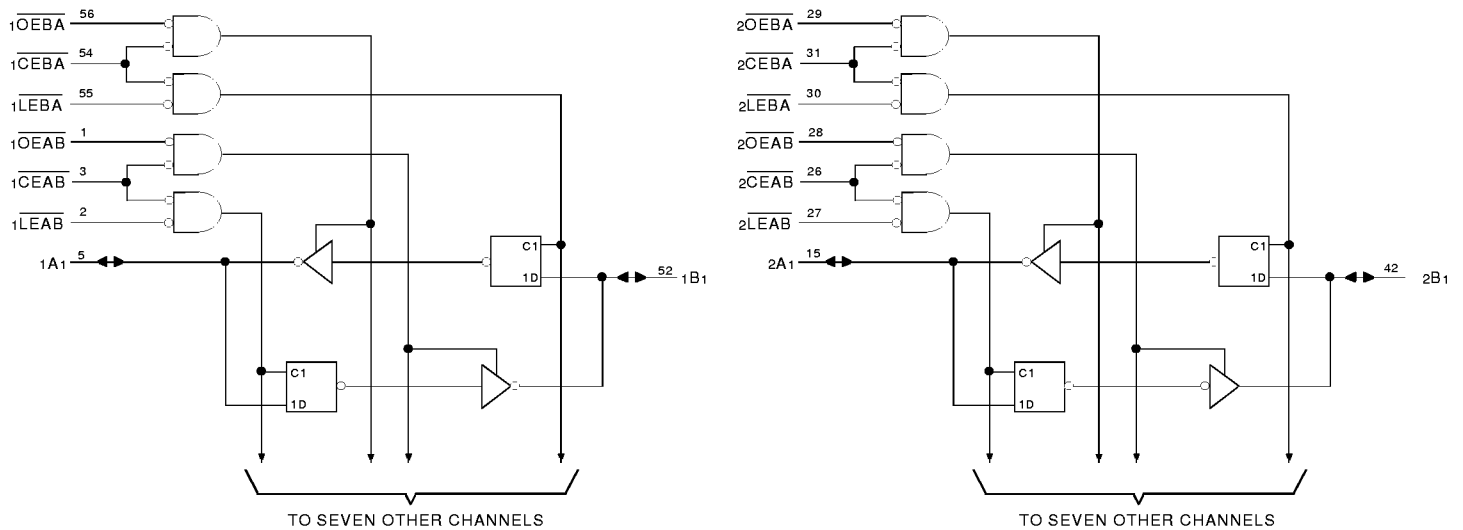
DESCRIPTION:

This 16-bit registered transceiver is built using advanced dual metal CMOS technology. The ALVCH162543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B enable (\overline{CEAB}) input must be low to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

The ALVCH162543 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

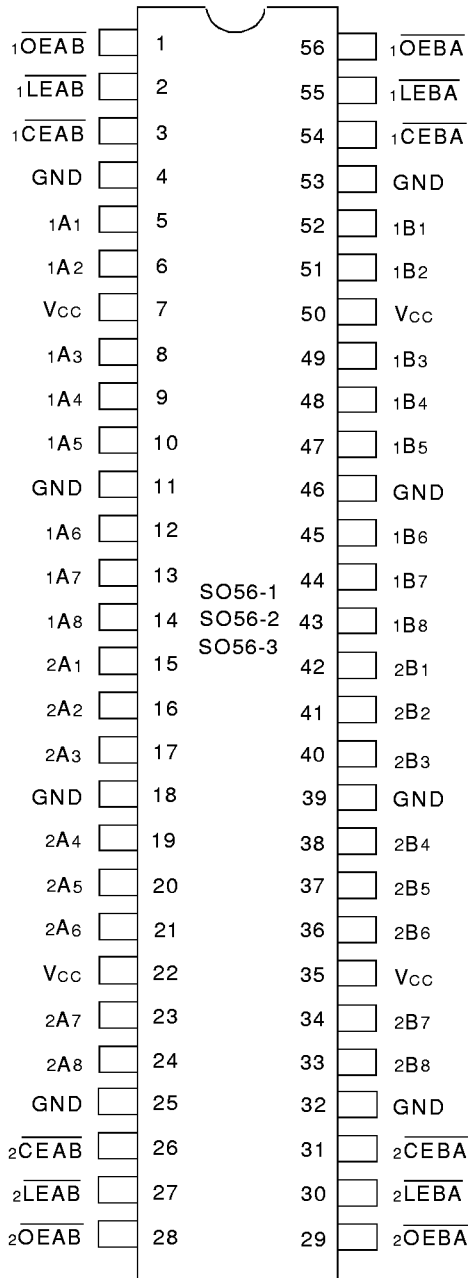
The ALVCH162543 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA

ALVC Link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

PIN DESCRIPTION

Pin Names	Description
x \overline{OEAB}	A-to-B Output Enable Inputs (Active LOW)
x \overline{OEBA}	B-to-A Output Enable Inputs (Active LOW)
x \overline{CEAB}	A-to-B Enable Inputs (Active LOW)
x \overline{CEBA}	B-to-A Enable Inputs (Active LOW)
x \overline{LEAB}	A-to-B Latch Enable Inputs (Active LOW)
x \overline{LEBA}	B-to-A Latch Enable Inputs (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

ALVC Link

NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit	
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V	
		V _{CC} = 2.7V to 3.6V		2	—	—		
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V	
		V _{CC} = 2.7V to 3.6V		—	—	0.8		
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA	
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5		
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA	
			V _O = GND	—	—	± 10	μA	
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V	
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV	
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA	
ΔI _{CC}		Quiescent Power Supply Current Variation		—	—	750		μA
		One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750		

ALVC Link

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -4mA	1.9	—	
			I _{OH} = -6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = -4mA	2.2	—	
			I _{OH} = -8mA	2	—	
		V _{CC} = 3.0V	I _{OH} = -6mA	2.4	—	
I _{OH} = -12mA	2		—			
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		V _{CC} = 3.0V	I _{OL} = 6mA	—	0.55	
I _{OL} = 12mA	—		0.8			

ALVC Link

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. TA = -40°C to +85°C.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH	Bus-Hold Input Sustain Current	$V_{CC} = 3.0V$	$V_I = 2.0V$	-75	—	—	μA
IBHL			$V_I = 0.8V$	75	—	—	
IBHH	Bus-Hold Input Sustain Current	$V_{CC} = 2.3V$	$V_I = 1.7V$	-45	—	—	μA
IBHL			$V_I = 0.7V$	45	—	—	
IBHHO	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6V$	$V_I = 0 \text{ to } 3.6V$	—	—	± 500	μA
IBHLO							

ALV6 Link

OPERATING CHARACTERISTICS, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	$C_L = 0pF, f = 10MHz$	—	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	—	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	1	6.2	—	5.5	1	4.9	ns
t _{PHL}	xAx to xBx or xBx to xAx							
t _{PLH}	Propagation Delay	1.1	7.6	—	6.9	1.1	5.6	ns
t _{PHL}	xLEAB to xBx or xLEBA to xAx							
t _{PZH}	Output Enable Time	1	8.2	—	7.6	1	6.2	ns
t _{PZL}	xCEAB to xBx or xCEBA to xAx							
t _{PHZ}	Output Disable Time	2	6.8	—	6.7	1.5	5.6	ns
t _{PLZ}	xCEAB, to xBx or xCEBA to xAx							
t _{PZH}	Output Enable Time	1	7.8	—	7	1	5.9	ns
t _{PZL}	xOEAB to xBx or xOEBA to xAx							
t _{PHZ}	Output Disable Time	1.6	6.4	—	5.3	1.1	5.1	ns
t _{PLZ}	xOEAB to xBx or xOEBA to xAx							
t _{SU}	Setup Time, data before $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	1.2	—	1.5	—	1.2	—	ns
t _H	Hold Time, data after $\overline{LE}\uparrow$ or $\overline{CE}\uparrow$	1.2	—	0.8	—	1.2	—	ns
t _w	Pulse Duration, \overline{LE} or \overline{CE} LOW	3.3	—	3.3	—	3.3	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:1. See test circuits and waveforms. $T_A = -40^\circ C$ to $+85^\circ C$.

2. Skew between any two outputs of the same package and switching in the same direction.

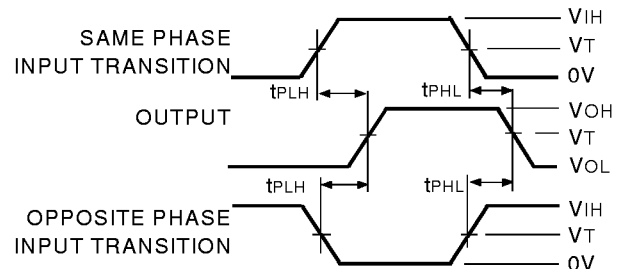
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	Vcc ⁽¹⁾ = 3.3V±0.3V	Vcc ⁽¹⁾ = 2.7V	Vcc ⁽²⁾ = 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
CL	50	50	30	pF

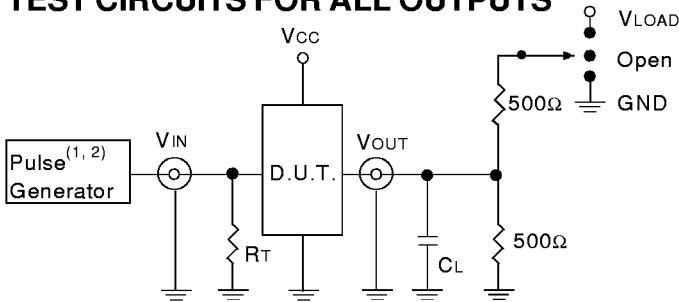
ALVC Link

PROPAGATION DELAY



ALVC Link

TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT= Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

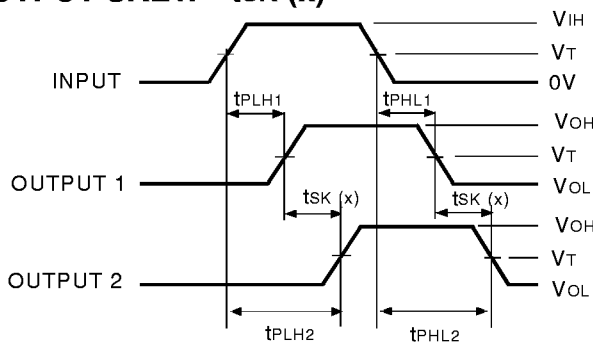
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION:

Test	Switch
Open Drain	V _{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

ALVC Link

OUTPUT SKEW - t_{SK} (x)



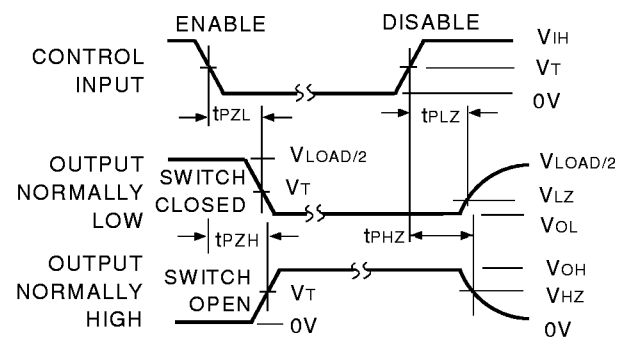
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

ENABLE AND DISABLE TIMES

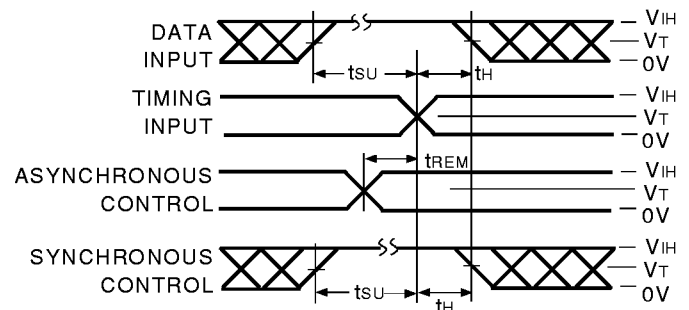


ALVC Link

NOTE:

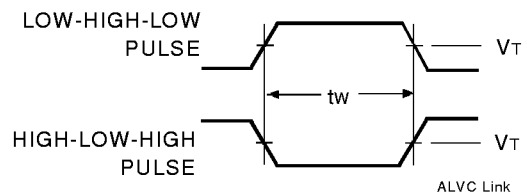
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION

