FAST CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT373T/AT/CT

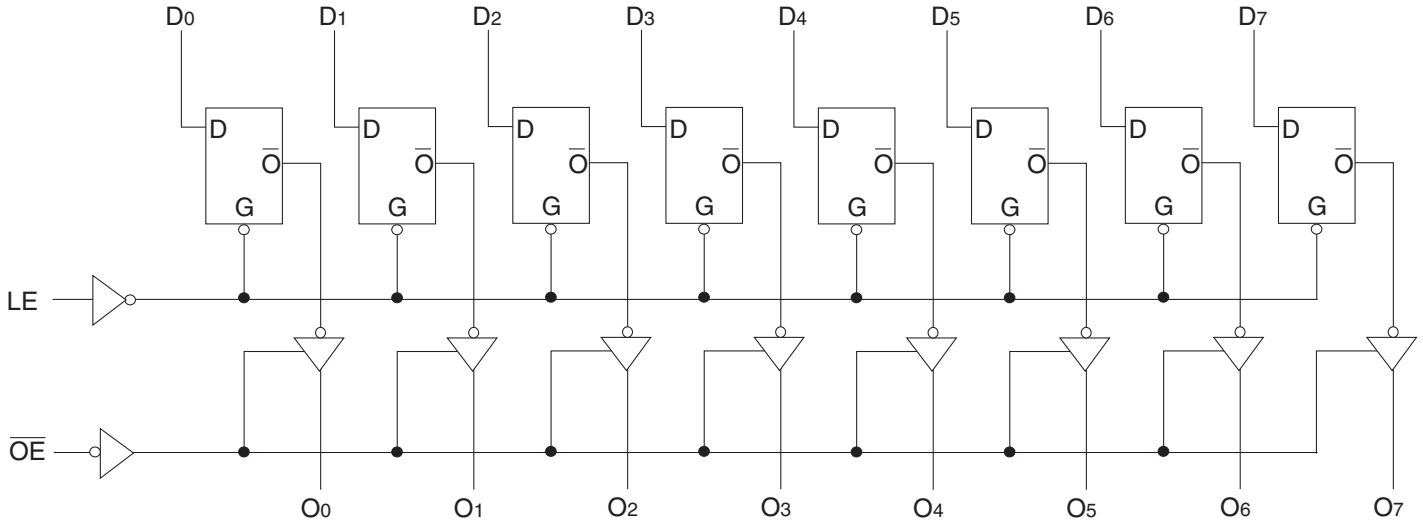
FEATURES:

- **Std., A, and C grades**
- **Low input and output leakage ≤1µA (max.)**
- **CMOS power levels**
- **True TTL input and output compatibility:**
  - *V_{OH} = 3.3V (typ.)*
  - *V_{OL} = 0.3V (typ.)*
- **High Drive outputs (-15mA I_{OH}, 48mA I_{OL})**
- **Meets or exceeds JEDEC standard 18 specifications**
- **Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)**
- **Power off disable outputs permit "live insertion"**
- **Available in the following packages:**
  - *Industrial: SOIC, SSOP, QSOP*
  - *Military: CERDIP, LCC*

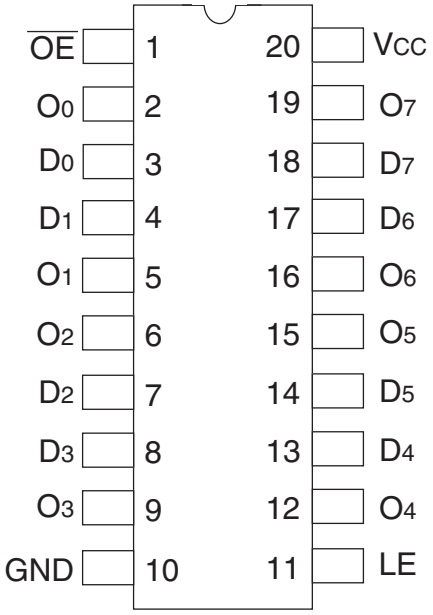
DESCRIPTION:

The FCT373Tis an octal transparent latch built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is high. When LE is low, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is low. When $\overline{OE}$ is high, the bus output is in the high-impedance state.

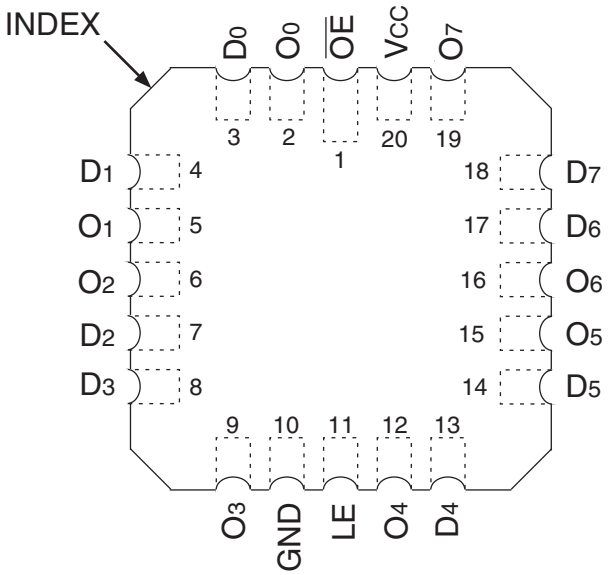
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC/ SSOP/ QSOP
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
Dx	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
Ox	3-State Outputs

FUNCTION TABLE(1)

Inputs			Outputs
Dx	**LE**	**$\overline{OE}$**	**Ox**
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL I_{OH} = –8mA IND	2.4	3.3	—	V
			I_{OH} = –12mA MIL I_{OH} = –15mA IND	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL I_{OL} = 48mA IND	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3	6[5]	mA
			V_{IN} = 3.4V V_{IN} = GND	—	5	14[5]	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Output Frequency
   N_i = Number of Outputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL

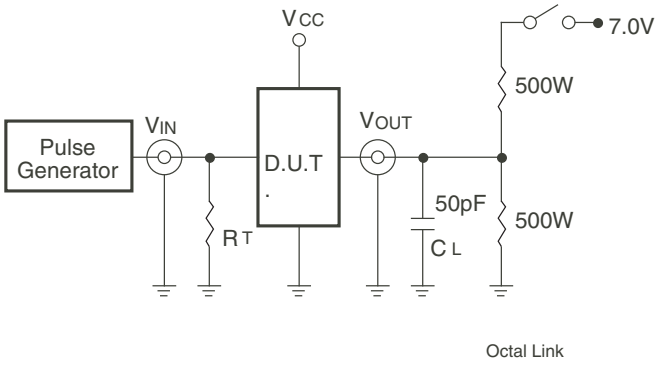
Symbol	Parameter	Condition[1]	74FCT373AT		74FCT373CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Dx to Ox	C_L = 50pF R_L = 500Ω	1.5	5.2	1.5	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Ox		2	8.5	2	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	6.5	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.5	1.5	5	ns
t_{SU}	Set-up Time HIGH or LOW, Dx to LE		2	—	2	—	ns
t_H	Hold Time HIGH or LOW, Dx to LE		1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH[3]		5	—	5	—	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

Symbol	Parameter	Condition[1]	54FCT373T		54FCT373AT		54FCT373CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Dx to Ox	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	5.6	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Ox		2	15	2	9.8	2	8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	13.5	1.5	7.5	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	10	1.5	6.5	1.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, Dx to LE		2	—	2	—	2	—	ns
t_H	Hold Time HIGH or LOW, Dx to LE		1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH[3]		6	—	6	—	6	—	ns

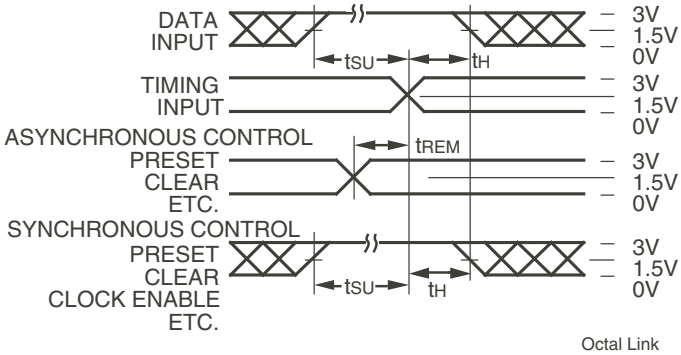
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS



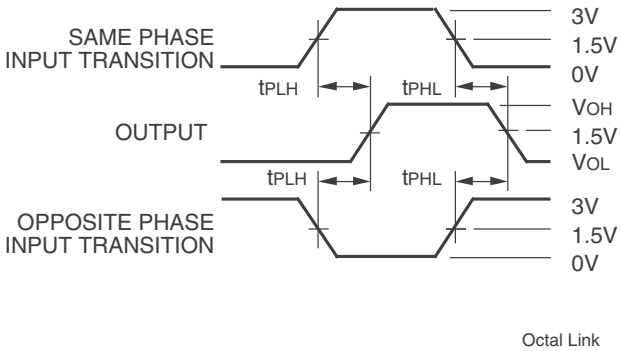
Octal Link

Test Circuits for All Outputs



Octal Link

Set-Up, Hold, and Release Times



Octal Link

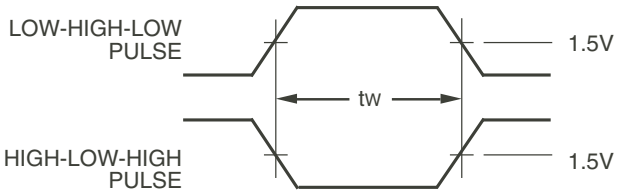
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

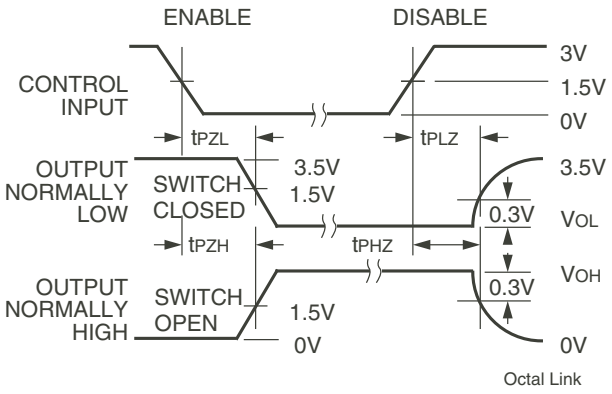
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

Octal Link



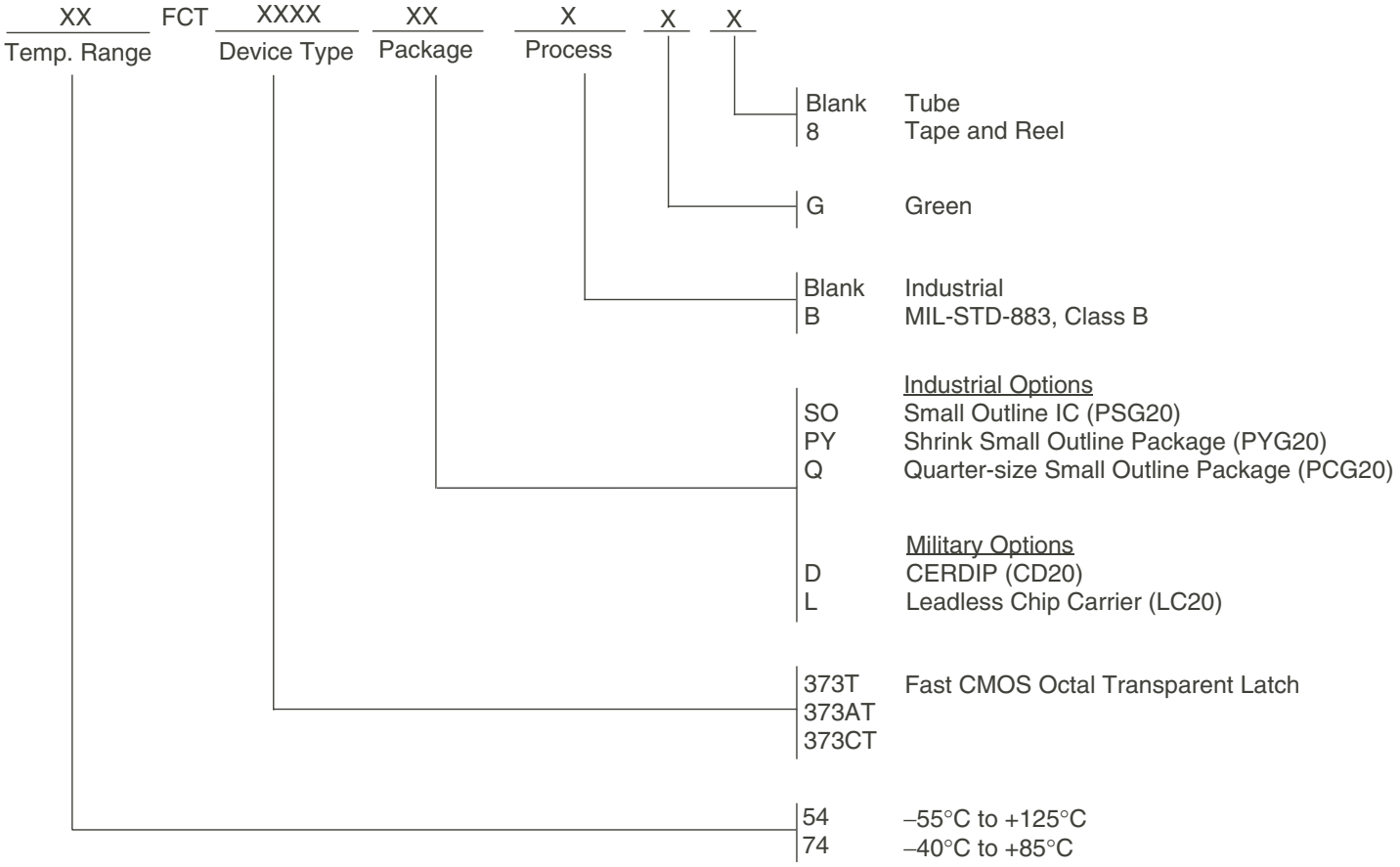
Octal Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



Datasheet Document History

10/03/2009	Pg. 7	Updated the ordering information by removing the "IDT" notation and non RoHS part.
12/01/2016	Pg. 7	Updated the ordering information by adding detailed package information and Tape & Reel.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.