74AUP1G00

Low-power 2-input NAND gate

Rev. 10 — 19 September 2024 | Product data sheet

1. General description

The 74AUP1G00 is a single 2-input NAND gate. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G00GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AUP1G00GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1G00GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AUP1G00GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74AUP1G00GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3
74AUP1G00GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking

Type number	Marking code [1]
74AUP1G00GW	pA
74AUP1G00GM	pA
74AUP1G00GN	pA
74AUP1G00GS	pA
74AUP1G00GX	pA
74AUP1G00GZ	pA

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

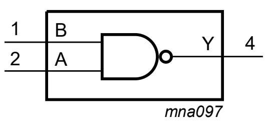


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

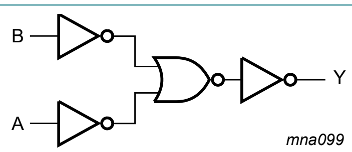
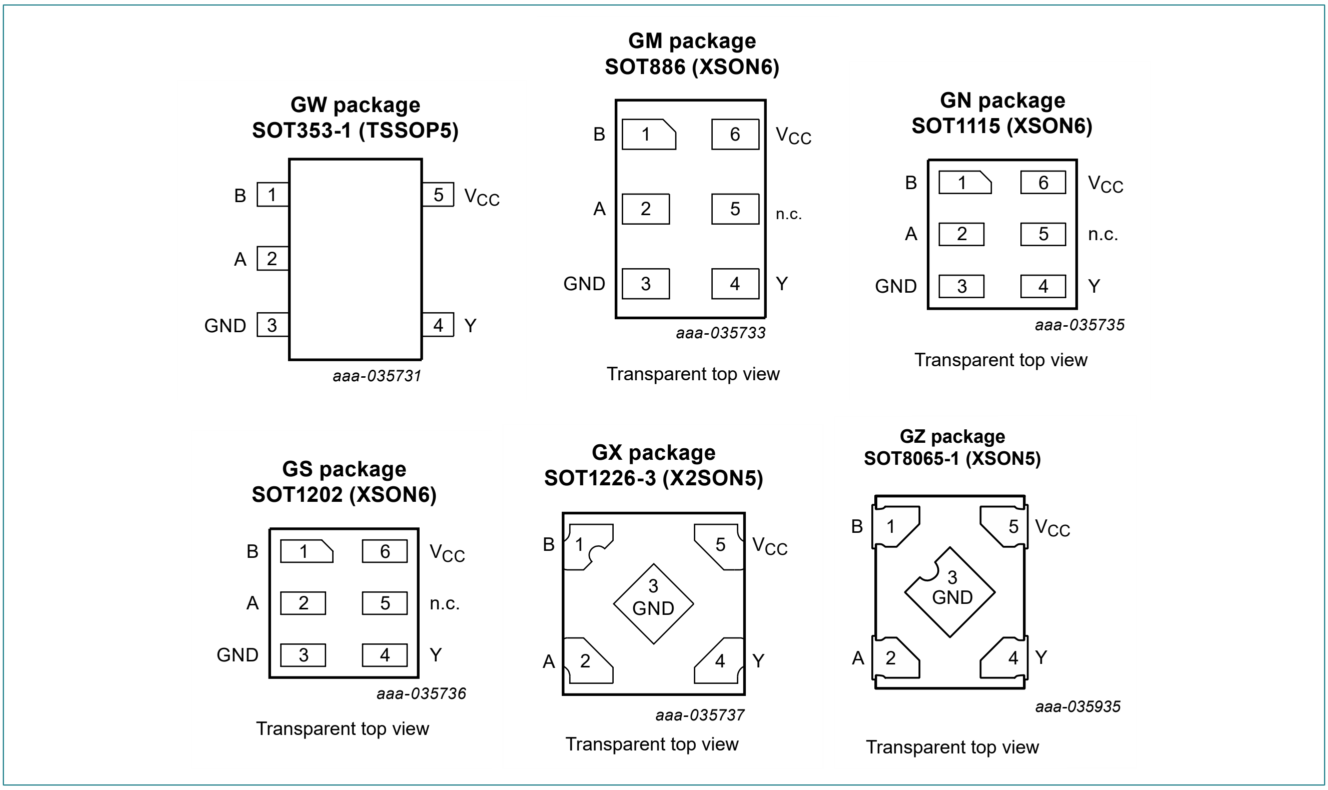


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5, X2SON5 and XSON5	XSON6	
B	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
V_O	output voltage	Active mode	[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}		-	±20	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.
For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 0.8 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70×V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65×V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	0.30×V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35×V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 μA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.75×V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3×V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	40	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	0.8	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.7	-	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V		0.70×V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V		0.65×V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V		-	-	0.30×V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V		-	-	0.35×V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20 μA; V_{CC} = 0.8 V to 3.6 V		V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V		0.7×V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V		1.03	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V		1.30	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V		1.97	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V		1.85	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V		2.67	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V		2.55	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V		-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V		-	-	0.3×V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V		-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V		-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.6	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V		-	-	0.9	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	50	μA
T_{amb} = -40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V		0.75×V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V		0.70×V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V		-	-	0.25×V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V		-	-	0.30×V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.9	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = -20 μA; V_{CC} = 0.8 V to 3.6 V		V_{CC} - 0.11	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V		0.6×V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V		0.93	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V		1.17	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V		1.77	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V		1.67	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V		2.40	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V		2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V		-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V		-	-	0.33×V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V		-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V		-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.75	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.75	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.75	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V		-	-	1.4	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	75	μA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
T_{amb} = 25 °C; C_L = 5 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4	[2]				
		V_{CC} = 0.8 V		-	17.5	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.5	5.3	11.0	ns
		V_{CC} = 1.4 V to 1.6 V		2.0	3.8	6.8	ns
		V_{CC} = 1.65 V to 1.95 V		1.6	3.1	5.3	ns
		V_{CC} = 2.3 V to 2.7 V		1.3	2.5	4.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.2	3.6	ns

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
T_{amb} = 25 °C; C_L = 10 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4	[2]				
		V_{CC} = 0.8 V		-	21.0	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.4	6.1	13.0	ns
		V_{CC} = 1.4 V to 1.6 V		2.4	4.4	7.9	ns
		V_{CC} = 1.65 V to 1.95 V		2.0	3.7	6.2	ns
		V_{CC} = 2.3 V to 2.7 V		1.4	3.0	4.7	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.8	4.3	ns
T_{amb} = 25 °C; C_L = 15 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4	[2]				
		V_{CC} = 0.8 V		-	24.5	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.4	6.9	14.8	ns
		V_{CC} = 1.4 V to 1.6 V		2.8	5.0	8.9	ns
		V_{CC} = 1.65 V to 1.95 V		2.0	4.1	7.0	ns
		V_{CC} = 2.3 V to 2.7 V		1.7	3.5	5.3	ns
		V_{CC} = 3.0 V to 3.6 V		1.6	3.2	4.9	ns
T_{amb} = 25 °C; C_L = 30 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4	[2]				
		V_{CC} = 0.8 V		-	34.8	-	ns
		V_{CC} = 1.1 V to 1.3 V		4.6	9.2	20.1	ns
		V_{CC} = 1.4 V to 1.6 V		3.0	6.5	11.8	ns
		V_{CC} = 1.65 V to 1.95 V		2.6	5.4	9.3	ns
		V_{CC} = 2.3 V to 2.7 V		2.4	4.6	7.1	ns
		V_{CC} = 3.0 V to 3.6 V		2.3	4.3	6.5	ns
T_{amb} = 25 °C							
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC}	[3]				
		V_{CC} = 0.8 V		-	2.6	-	pF
		V_{CC} = 1.1 V to 1.3 V		-	2.8	-	pF
		V_{CC} = 1.4 V to 1.6 V		-	2.9	-	pF
		V_{CC} = 1.65 V to 1.95 V		-	3.1	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	3.6	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	4.2	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

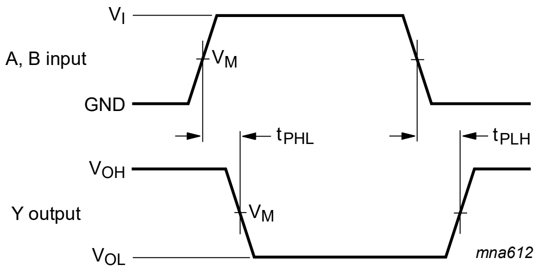
Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
C_L = 5 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V_{CC} = 1.1 V to 1.3 V	2.1	12.2	2.1	13.5	ns
		V_{CC} = 1.4 V to 1.6 V	1.8	7.8	1.8	8.6	ns
		V_{CC} = 1.65 V to 1.95 V	1.4	6.2	1.4	6.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.1	4.7	1.1	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	4.2	1.0	4.7	ns
C_L = 10 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V_{CC} = 1.1 V to 1.3 V	2.2	14.4	2.2	15.9	ns
		V_{CC} = 1.4 V to 1.6 V	2.2	9.2	2.2	10.2	ns
		V_{CC} = 1.65 V to 1.95 V	1.9	7.3	1.9	8.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.3	5.6	1.3	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	4.9	1.2	5.4	ns
C_L = 15 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V_{CC} = 1.1 V to 1.3 V	3.1	16.5	3.1	18.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	10.5	2.5	11.6	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	8.3	2.0	9.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	6.4	1.5	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	5.7	1.4	6.3	ns
C_L = 30 pF							
t_{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V_{CC} = 1.1 V to 1.3 V	4.1	22.6	4.1	24.9	ns
		V_{CC} = 1.4 V to 1.6 V	2.9	14.0	2.9	15.4	ns
		V_{CC} = 1.65 V to 1.95 V	2.3	11.1	2.3	12.3	ns
		V_{CC} = 2.3 V to 2.7 V	2.1	8.5	2.1	9.4	ns
		V_{CC} = 3.0 V to 3.6 V	2.1	7.6	2.1	8.4	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

11.1. Waveforms and test circuit



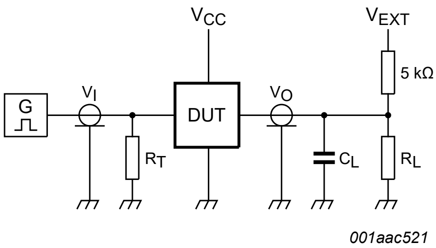
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig. 4. The data input (A or B) to output (Y) propagation delays

Table 10. Measurement points

Supply voltage	Input			Output
V_{CC}	V_M	V_I	$t_r = t_f$	V_M
0.8 V to 3.6 V	0.5 × V_{CC}	V_{CC}	≤ 3.0 ns	0.5 × V_{CC}



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

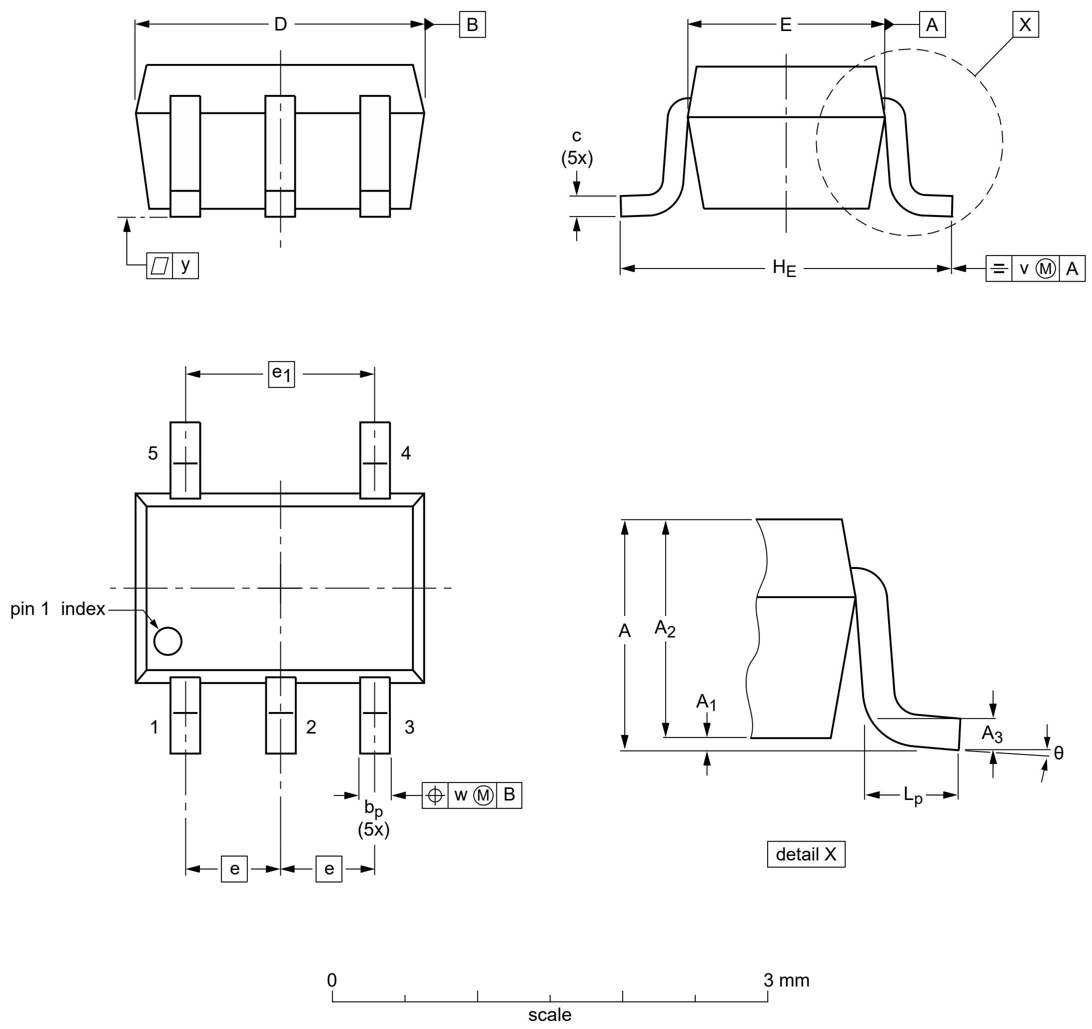
Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V_{CC}

[1] For measuring enable and disable times R_L = 5 kΩ.
For measuring propagation delays, setup and hold times and pulse width R_L = 1 MΩ.

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

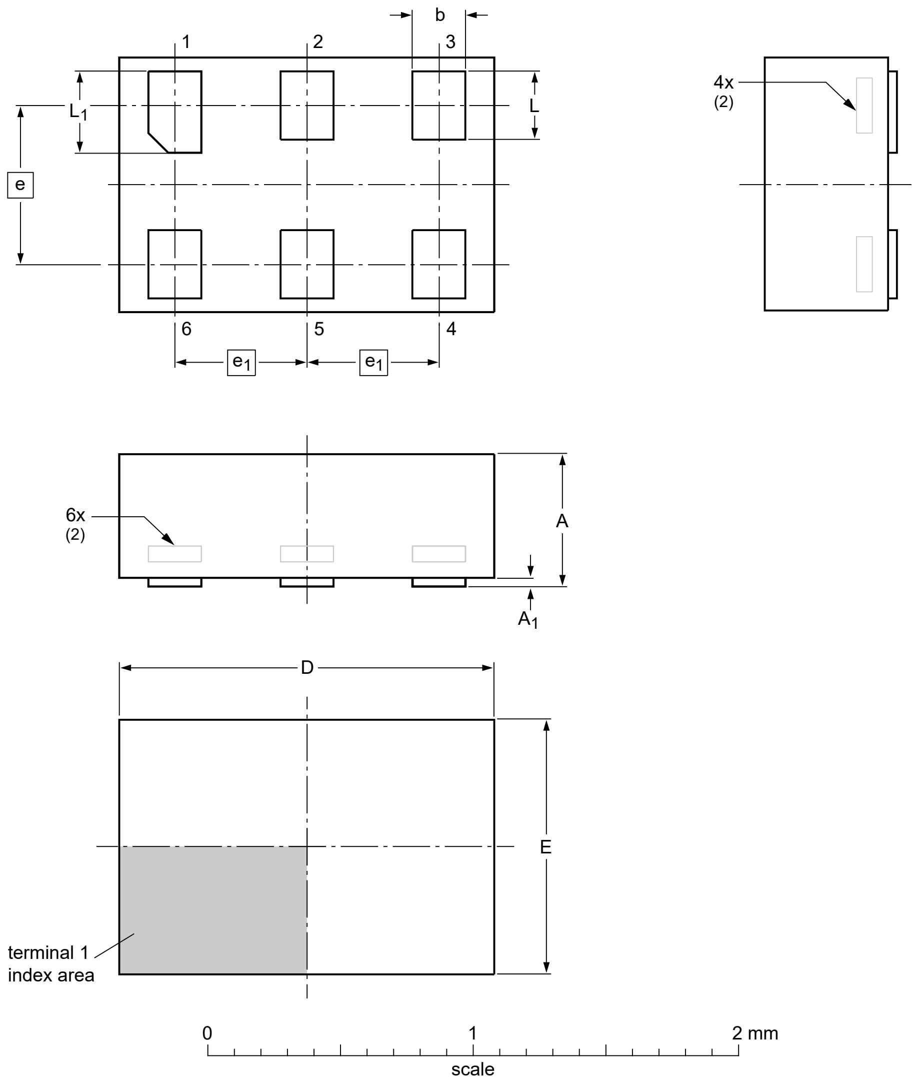
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 6. Package outline SOT353-1 (TSSOP5)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

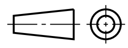
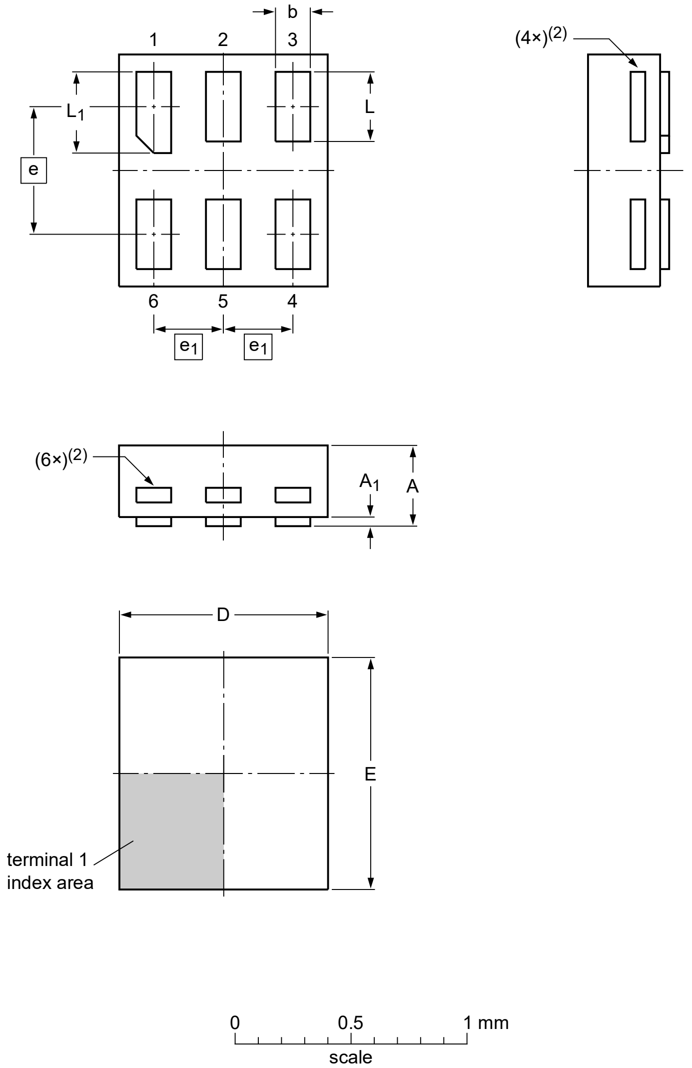
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 7. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

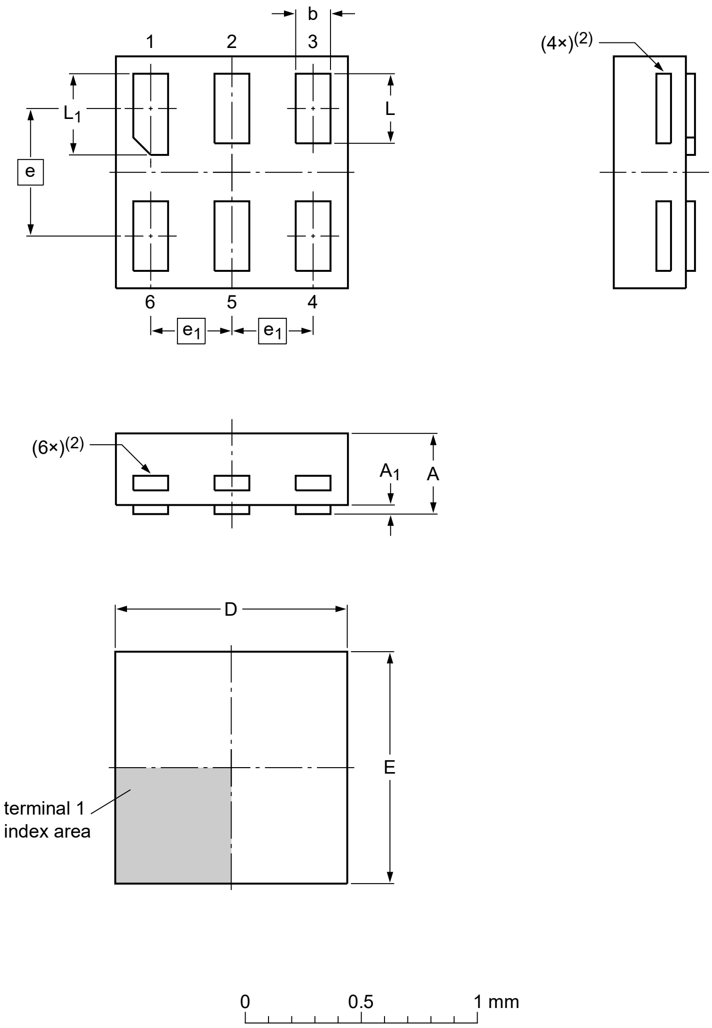
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Fig. 8. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

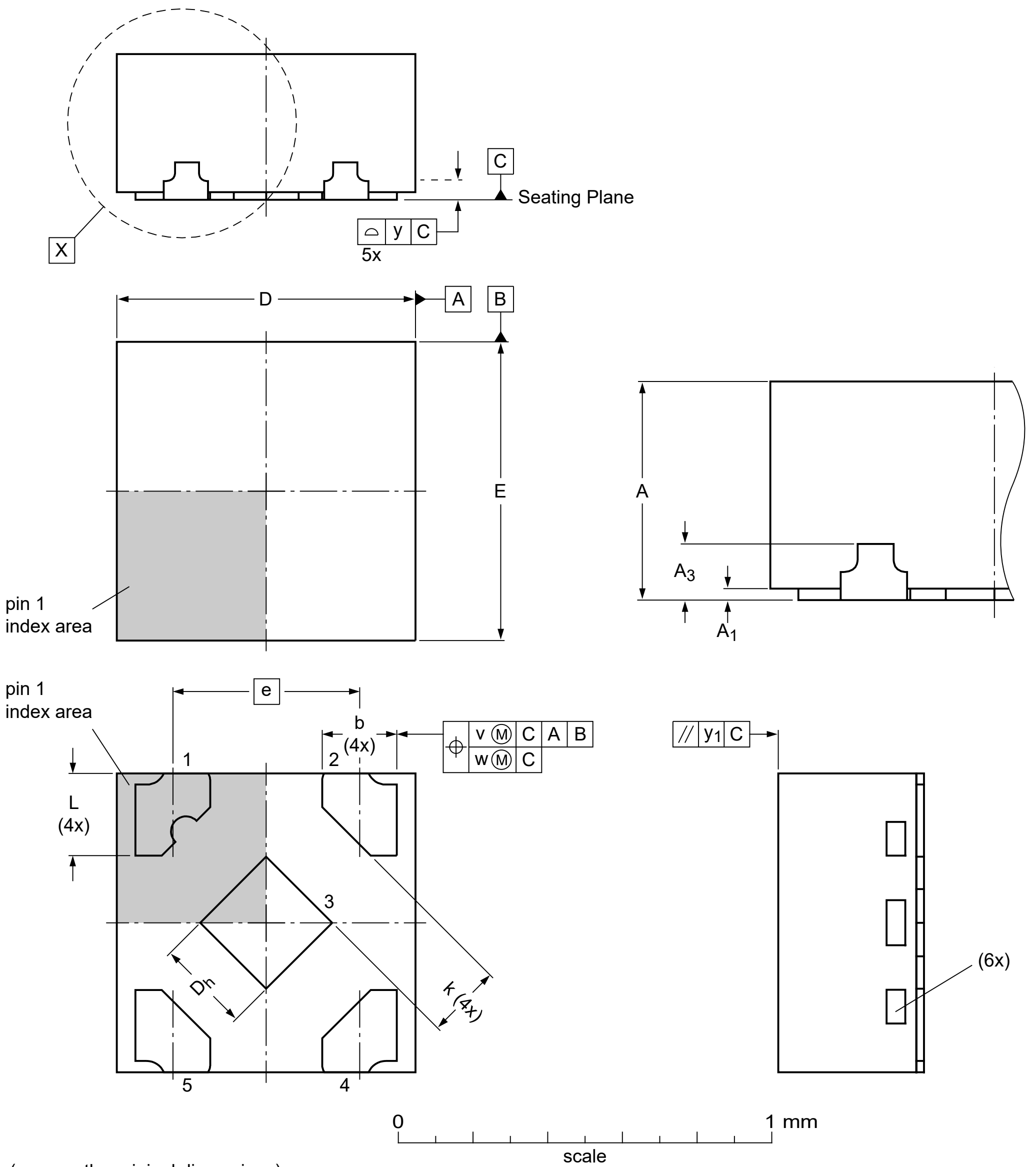
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References IEC	JEDEC	JEITA		European projection	Issue date
SOT1202						~~10-04-02~~ 10-04-06

Fig. 9. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm **SOT1226-3**



Dimensions (mm are the original dimensions)

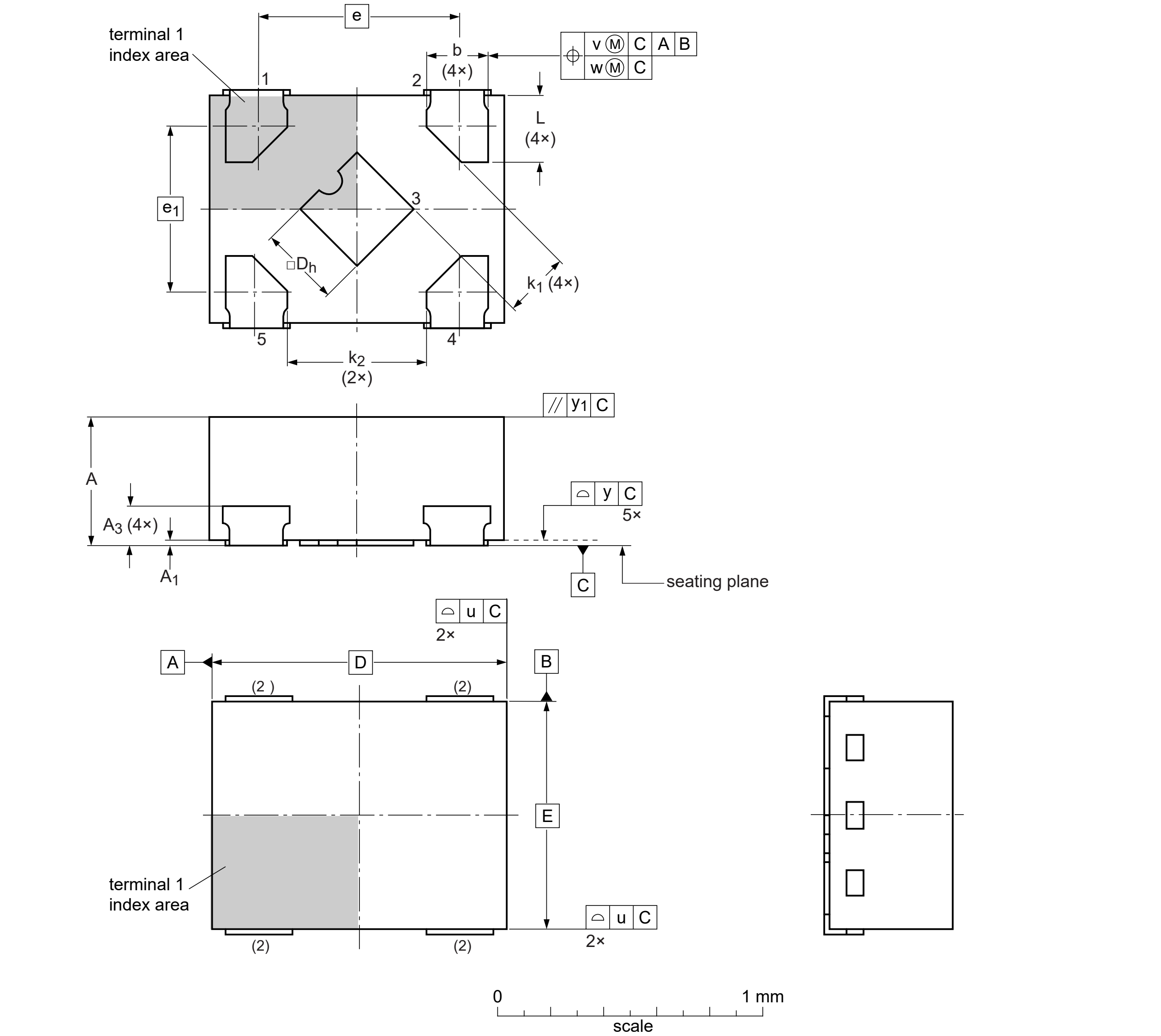
Unit		A	A1	A3	D	Dh	E	b	e	K	L	v	w	y	y1
mm	max	0.35	0.04		0.85	0.30	0.85	0.25			0.27				
	nom	0.32	0.02	0.10 (Typ.)	0.80	0.25	0.80	0.20	0.50		0.22	0.1	0.05	0.05	0.05
	min	0.30	0.00		0.75	0.20	0.75	0.15		0.20	0.17				

sot1226-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT1226-3		- - -				~~19-11-06~~ 19-11-07

Fig. 10. Package outline SOT1226-3 (X2SON5)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm **SOT8065-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	A_3	b	$D^{(1)}$	D_h	$E^{(1)}$	e	e_1	k_1	k_2	L	u	v	w	y	y_1
mm	max	0.50	0.040		0.28		0.35						0.30					
	nom	0.47	0.020	0.135 (typ)	0.23	1.10	0.30	0.85	0.75	0.6			0.25	0.05	0.1	0.05	0.05	0.05
	min	0.44	0.005		0.20		0.27				0.2	0.45	0.22					

Note:
1. Plastic or metal protrusions per side are not included.
2. Side wettable flanks (SWF), protrusion max. 0.02 mm.

sot8065-1_po

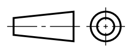
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8065-1		MO-340				~~24-07-09~~ 24-08-27

Fig. 11. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G00 v.10	20240919	Product data sheet	-	74AUP1G00 v.9.1
Modifications:	• Type number 74AUP1G00GZ (SOT8065-1/XSON5) added.			
74AUP1G00 v.9.1	20230711	Product data sheet	-	74AUP1G00 v.8
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AUP1G00 v.8	20220113	Product data sheet	-	74AUP1G00 v.7
Modifications:	• Section 1 and Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated. • Type number 74AUP1G00GF (SOT891) removed. • SOT1226 (X2SON5) package changed to SOT1226-3 (X2SON5) package. • Fig. 6: Package outline drawing for SOT353-1 (TSSOP5) has changed.			
74AUP1G00 v.7	20190423	Product data sheet	-	74AUP1G00 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Pin configuration drawing SOT1226 (X2SON5) updated.			
74AUP1G00 v.6	20120627	Product data sheet	-	74AUP1G00 v.5
Modifications:	• Added type number 74AUP1G00GX (SOT1226).			
74AUP1G00 v.5	20120316	Product data sheet	-	74AUP1G00 v.4
Modifications:	• Package outline drawing of SOT886 (Fig. 7) modified.			
74AUP1G00 v.4	20111115	Product data sheet	-	74AUP1G00 v.3
Modifications:	• Legal pages updated.			
74AUP1G00 v.3	20101007	Product data sheet	-	74AUP1G00 v.2
74AUP1G00 v.2	20060629	Product data sheet	-	74AUP1G00 v.1
74AUP1G00 v.1	20050711	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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