

# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# MC74VHCT541A

## Octal Bus Buffer

The MC74VHCT541A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT541A is a noninverting, 3-state, buffer/line driver/line receiver. When either  $\overline{OE1}$  or  $\overline{OE2}$  is high, the terminal outputs are in the high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT541A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage–input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

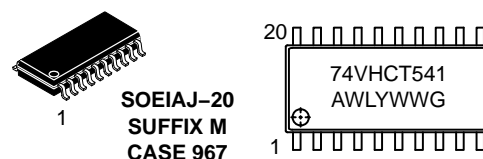
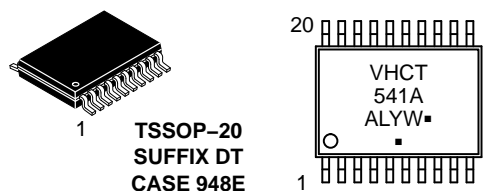
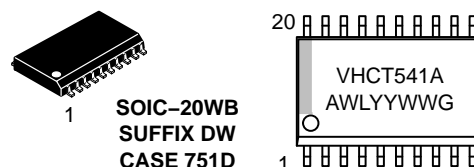
- High Speed:  $t_{PD} = 5.4$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 1.6$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74VHCT541A

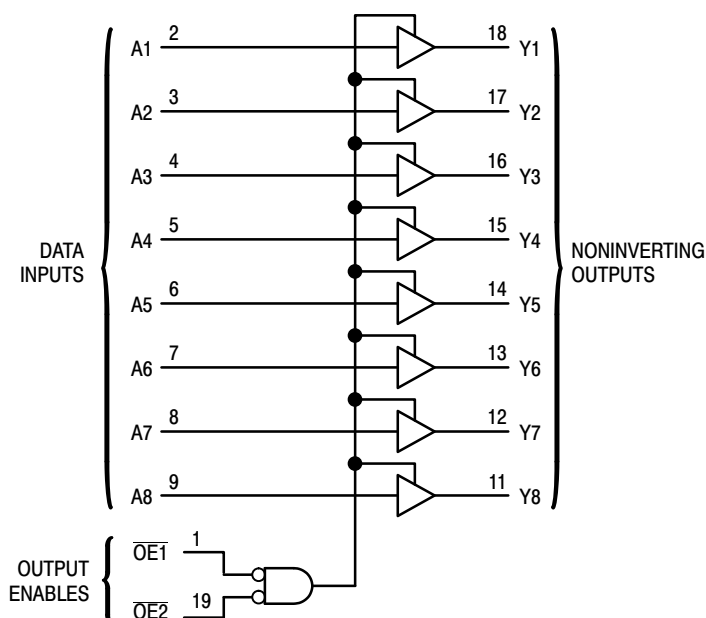


Figure 1. Logic Diagram

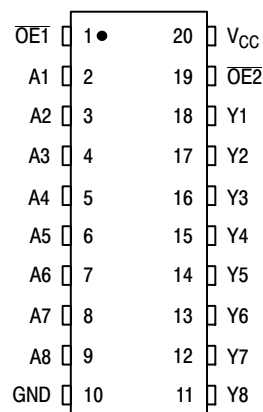


Figure 2. Pin Assignment

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage	- 0.5 to + 7.0	V
$V_{out}$	DC Output Voltage Outputs in 3-State High or Low State	- 0.5 to + 7.0 - 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	- 20	mA
$I_{OK}$	Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	4.5	5.5	V
$V_{in}$	DC Input Voltage	0	5.5	V
$V_{out}$	DC Output Voltage Outputs in 3-State High or Low State	0 0	5.5 $V_{CC}$	V
$T_A$	Operating Temperature	- 40	+ 85	°C
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 5.0V \pm 0.5V$		ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# MC74VHCT541A

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = - 50μA	4.5	4.4	4.5		4.4		V
		I <sub>OH</sub> = - 8mA	4.5	3.94			3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5		0.0	0.1		0.1	V
		I <sub>OL</sub> = 8mA	4.5			0.36		0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5			± 0.25		± 2.5	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μA
I <sub>CCT</sub>	Quiescent Supply Current	Per Input: V <sub>IN</sub> = 3.4V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5V	0			0.5		5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to Y	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.0 5.5	6.9 7.9	1.0 1.0	8.0 9.0	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OE to Y	V <sub>CC</sub> = 5.0 ± 0.5V R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF		8.3 8.8	11.3 12.3	1.0 1.0	13.0 14.0	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OE to Y	V <sub>CC</sub> = 5.0 ± 0.5V R <sub>L</sub> = 1kΩ		9.4	11.9	1.0	13.5	ns
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF (Note 1)			1.0		1.0	ns
C <sub>in</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>out</sub>	Maximum 3-State Output Capacitance (Output in High Impedance State)			9				pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)	<b>Typical @ 25°C, V<sub>CC</sub> = 5.0V</b>					pF
		19					

- Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.
- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50pF, V<sub>CC</sub> = 5.0V)

Symbol	Parameter	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	1.2	1.6	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.2	-1.6	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

# MC74VHCT541A

## ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT541ADWG	SOIC-20WB (Pb-Free)	38 Units / Rail
MC74VHCT541ADWRG	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74VHCT541ADTG	TSSOP-20 (Pb-Free)	75 Units / Rail
MC74VHCT541ADTRG	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
NLV74VHCT541ADTRG*	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
MC74VHCT541AMELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

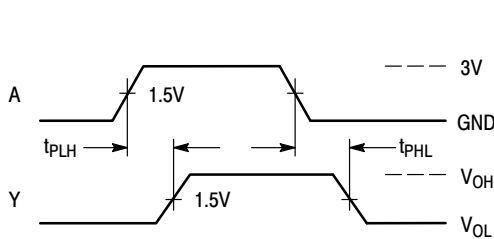


Figure 3. Switching Waveform

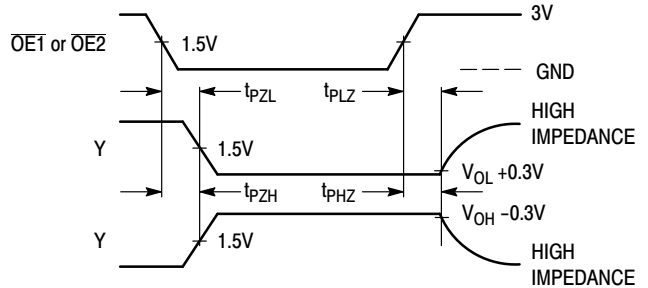
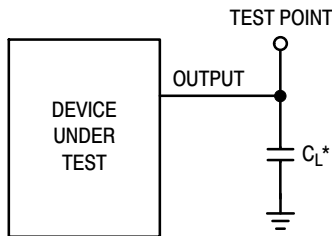
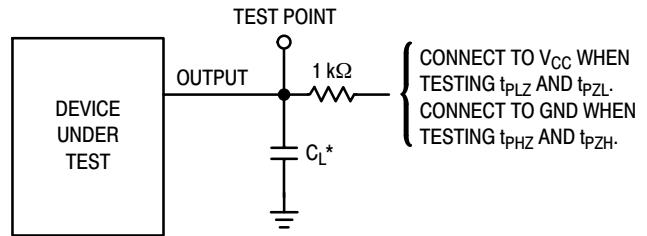


Figure 4. Switching Waveform



\*Includes all probe and jig capacitance

Figure 5. Test Circuit



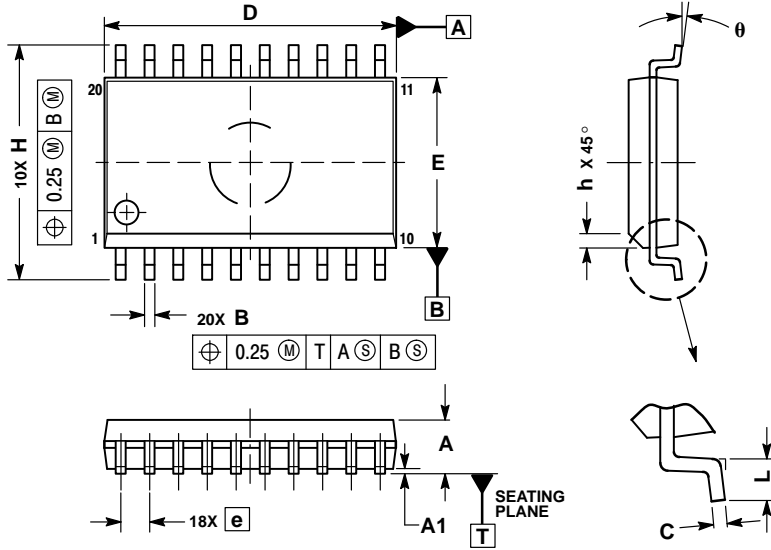
\*Includes all probe and jig capacitance

Figure 6. Test Circuit

# MC74VHCT541A

## PACKAGE DIMENSIONS

SOIC-20 WB  
DW SUFFIX  
CASE 751D-05  
ISSUE G



NOTES:

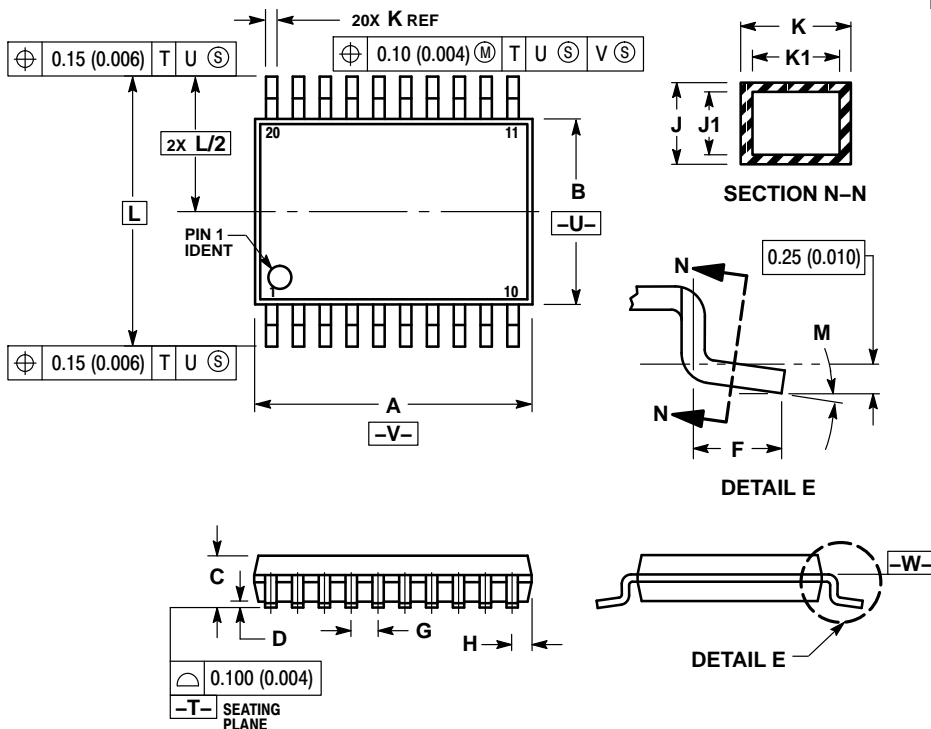
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

# MC74VHCT541A

## PACKAGE DIMENSIONS

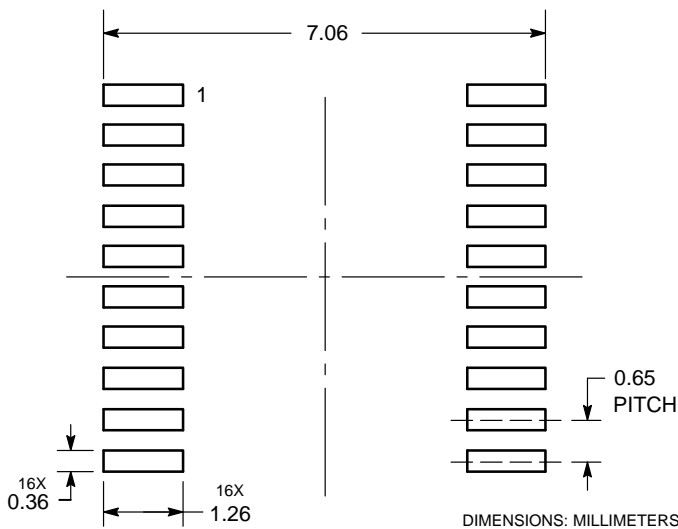
TSSOP-20  
CASE 948E-02  
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

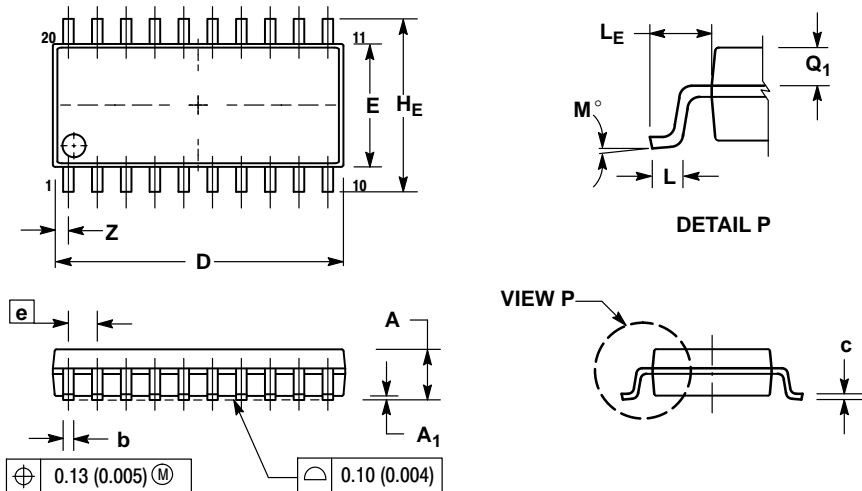
### SOLDERING FOOTPRINT



# MC74VHCT541A

## PACKAGE DIMENSIONS


SOEIAJ-20  
M SUFFIX  
CASE 967  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative