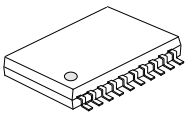
U74AHC573

CMOS IC

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



TSSOP-20

■ DESCRIPTION

The **U74AHC573** is an octal transparent D-type latch with 3-state outputs, and it has 8 channels.

When the $\overline{OE}$ input is low and the LE input is high, the Q outputs follow the D inputs. When $\overline{OE}$ is low and LE is low, the Q outputs are latched at the logic levels of the D inputs.

When the $\overline{OE}$ input is high, the outputs are in the high-impedance. The $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* Operate from 2V to 5.5V
* Inputs Accept Voltages to 5.5V
* Max t_{PD} of 13ns at V_{CC}=3.3V, C_L=15pF
* Typ V_{OL}< 0.36V at V_{CC}=4.5V, I_{OL}=8mA, T_A=25°C
* Typ V_{OH}> 3.94V at V_{CC}=4.5V, I_{OH}=-8mA, T_A=25°C

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC573L-P20-R	U74AHC573G-P20-R	TSSOP-20	Tape Reel

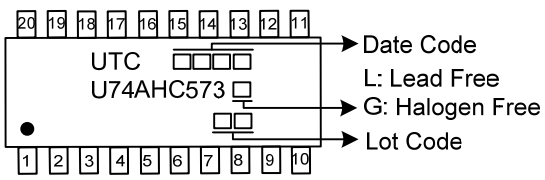
U74AHC573G-P20-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel

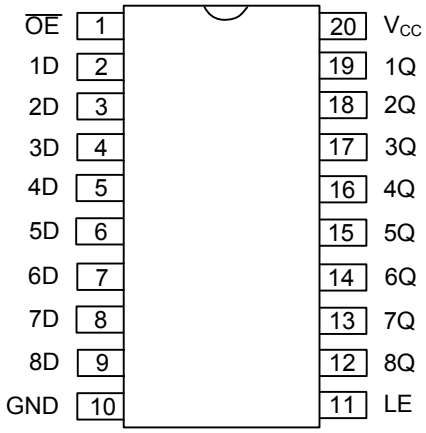
(2) P20: TSSOP-20

(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

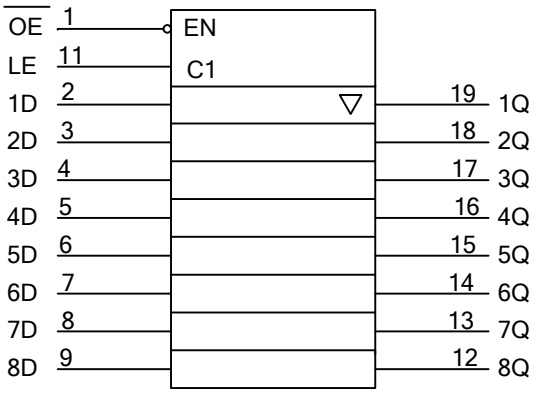


■ FUNCTION TABLE

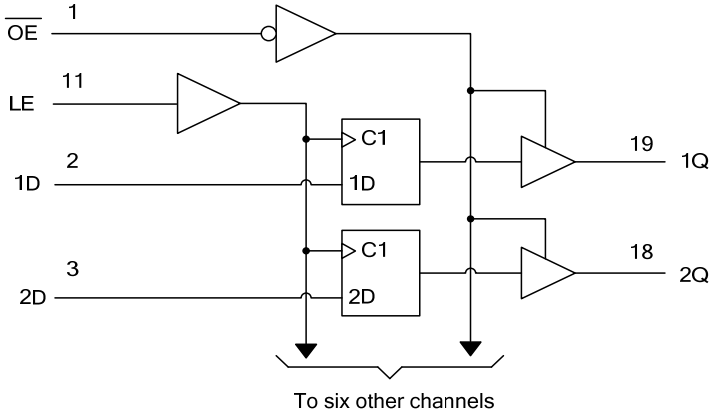
INPUTS($\overline{OE}$)	INPUTS(LE)	INPUTS(D)	OUTPUT(Q)
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Note: H: HIGH voltage level, L: LOW voltage level.

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage	V_{CC}	-0.5 ~ 7	V
Input voltage (Note 2)	V_I	-0.5 ~ 7	V
Output voltage (Note 2)	V_O	-0.5 ~ V_{CC} +0.5	V
Input clamp current	I_{IK}	-20	mA
Output clamp current	I_{OK}	±20	mA
Output current	I_O	±25	mA
V_{CC} or GND current	I_{CC}	±75	mA
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2		5.5	V
High-Level Input Voltage	V_{IH}	V_{CC} = 2 V	1.5			V
		V_{CC} = 3 V	2.1			
		V_{CC} = 5.5V	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2 V			0.5	V
		V_{CC} = 3 V			0.9	
		V_{CC} = 5.5V			1.65	
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-Level Output Current	I_{OH}	V_{CC} = 2 V			-50	μA
		V_{CC} = 3.3 V ± 0.3 V			-4	mA
		V_{CC} = 5 V ± 0.5 V			-8	
Low-Level Output Current	I_{OL}	V_{CC} = 2 V			50	μA
		V_{CC} = 3.3 V ± 0.3 V			4	mA
		V_{CC} = 5 V ± 0.5 V			8	
Input Rise or Fall Times	t_R, t_F	V_{CC} = 3.3 V ± 0.3 V			100	ns/V
		V_{CC} = 5 V ± 0.5 V			20	

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-50μA	1.9			V
		V_{CC}=3V, I_{OH}=-50μA	2.9			
		V_{CC}=4.5V, I_{OH}=-50μA	4.4			
		V_{CC}=3V, I_{OH}=-4mA	2.58			
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OL}=50μA			0.1	V
		V_{CC}=3V, I_{OL}=50μA			0.1	
		V_{CC}=4.5V, I_{OL}=50μA			0.1	
		V_{CC}=3V, I_{OL}=4mA			0.36	
		V_{CC}=4.5V, I_{OL}=8mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V ~ 5.5V, V_{IN}=0 or 5.5V			±0.1	μA
Leakage Current (For output in high-impedance state)	I_{OZ}	V_{CC}=5.5V, V_{IN}=V_{IH} or V_{IH}, V_{OUT}=0 or 5.5V			±0.25	μA
Quiescent Supply Current	I_Q	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA
Input Capacitance	C_I	V_{CC}=5V, V_{IN}=V_{CC} or GND		2.5	10	pF
Output Capacitance	C_O	V_{CC}=5V, V_{OUT}=V_{CC} or GND		3.5		pF

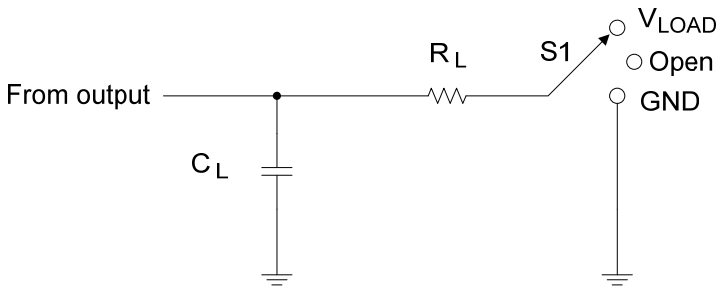
■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From D to Q	t_{PLH}/t_{PHL}	V_{CC}=3.3V±0.3V, C_L=15pF		7	11	ns
		V_{CC}=3.3V±0.3V, C_L=50pF		9.5	14.5	
		V_{CC}=5V±0.5V, C_L=15pF		4.5	6.8	
		V_{CC}=5V±0.5V, C_L=50pF		6	8.8	
From LE to Q		V_{CC}=3.3V±0.3V, C_L=15pF		7.6	11.9	
		V_{CC}=3.3V±0.3V, C_L=50pF		10.1	15.4	
		V_{CC}=5V±0.5V, C_L=15pF		5	7.7	
		V_{CC}=5V±0.5V, C_L=50pF		6.5	9.7	
From $\overline{OE}$ to Q	t_{PZL}/t_{PZH}	V_{CC}=3.3V±0.3V, C_L=15pF		7.3	11.5	ns
		V_{CC}=3.3V±0.3V, C_L=50pF		9.8	15	
		V_{CC}=5V±0.5V, C_L=15pF		5.2	7.7	
		V_{CC}=5V±0.5V, C_L=50pF		6.7	9.7	
From $\overline{OE}$ to Q	t_{PLZ}/t_{PHZ}	V_{CC}=3.3V±0.3V, C_L=15pF		8.3	11	ns
		V_{CC}=3.3V±0.3V, C_L=50pF		10.7	14.5	
		V_{CC}=5V±0.5V, C_L=15pF		5.2	7.7	
		V_{CC}=5V±0.5V, C_L=50pF		6.7	9.7	
Pulse Width, LE high	t_W	V_{CC}=3.3V±0.3V	5			ns
		V_{CC}=5V±0.5V	5			
Setup Time, data before LE ↓	t_{SU}	V_{CC}=3.3V±0.3V	3.5			ns
		V_{CC}=5V±0.5V	3.5			
Hold Time, data after LE ↓	t_H	V_{CC}=3.3V±0.3V	1.5			ns
		V_{CC}=5V±0.5V	1.5			

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	No load, f=1MHz	16	pF

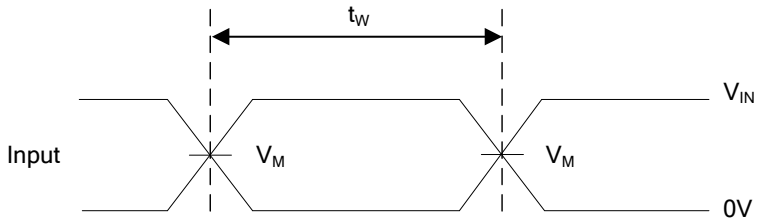
■ TEST CIRCUIT AND WAVEFORMS



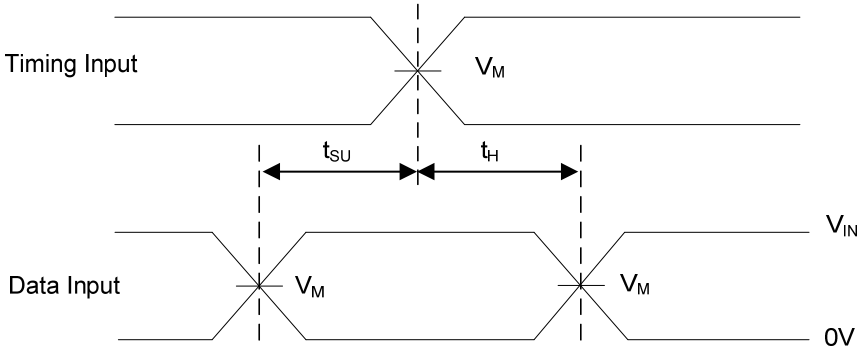
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
3.3V±0.3V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF 50pF	1kΩ	0.3V
5V±0.5V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF 50pF	1kΩ	0.5V

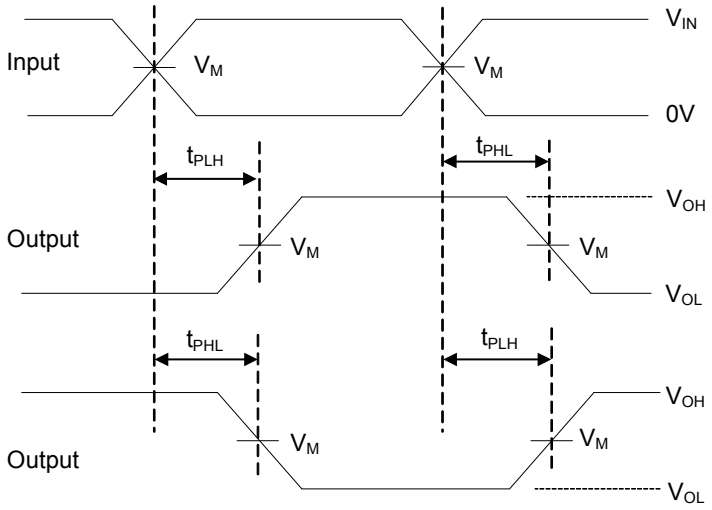


Pulse Duration

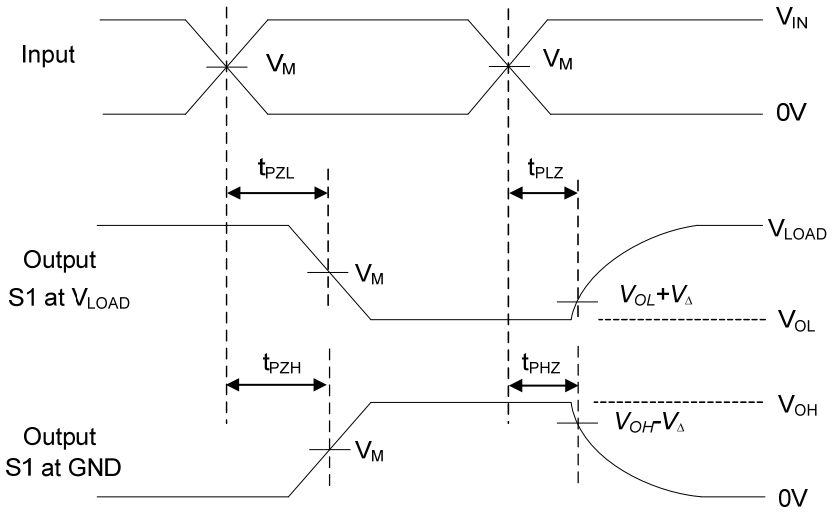


Setup and Hold Times

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enble and Disable Times

Note: A. C_L includes probe and jig capacitance.
Note: B. P_{RR} ≤1MHz, Z_O = 50Ω, t_R ≤3ns, t_F ≤3ns.