

# 54AC374,54ACT374

*54AC374 54ACT374 Octal D Flip-Flop with TRI-STATE Outputs*



Literature Number: SNOS105

## 54AC374 • 54ACT374 Octal D Flip-Flop with TRI-STATE® Outputs

### General Description

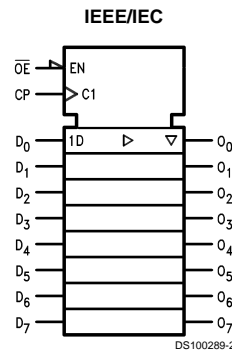
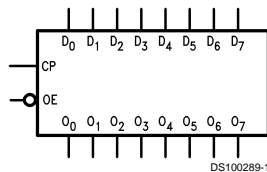
The 'AC/ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications

- Outputs source/sink 24 mA
- See '273 for reset version
- See '377 for clock enable version
- See '373 for transparent latch version
- See '574 for broadside pinout version
- See '564 for broadside pinout version with inverted outputs
- 'ACT374 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC374: 5962-87694
  - 'ACT374: 5962-87631

### Logic Symbols

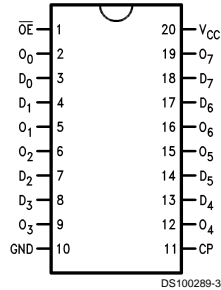


Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs

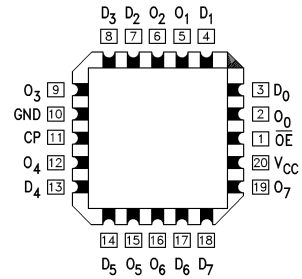
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## Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC



## Functional Description

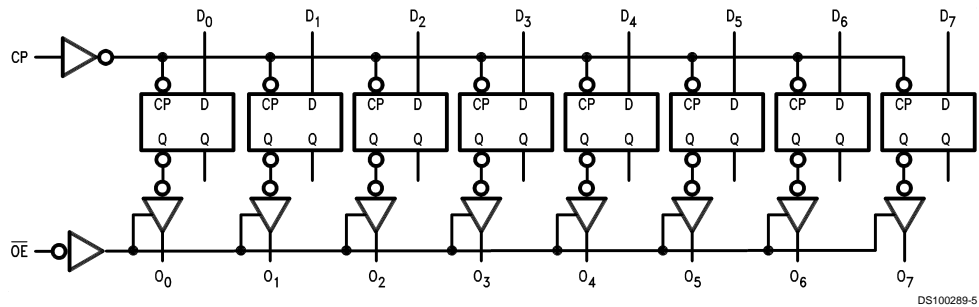
The 'AC/ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs			Outputs
$D_n$	CP	$\overline{OE}$	$O_n$
H	↗	L	H
L	↗	L	L
X	X	H	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

## DC Characteristics for 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54AC		Units	Conditions
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			
			Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
			3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH}$
			4.5	3.7		
			5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
			3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL}$
			4.5	0.50		
			5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OZ}$	Maximum TRI-STATE Current	5.5	±5.0	$\mu A$	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$	

### DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54AC		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
I <sub>OLD</sub>	(Note 3) Minimum Dynamic Output Current	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5	-50			
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

### DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4		V	I <sub>OUT</sub> = -50 μA
		5.5	5.4			
		4.5	3.70		V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -24 mA -24 mA
		5.5	4.70			
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1		V	I <sub>OUT</sub> = 50 μA
		5.5	0.1			
		4.5	0.50		V	(Note 5) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> 24 mA 24 mA
	5.5	0.50				
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum TRI-STATE Current	5.5	±5.0		μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	(Note 6) Minimum Dynamic Output Current	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5	-50			
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 7:** I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	60 95		MHz	
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	3.3 5.0	3.0 3.0	16.5 12.0	ns	
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	3.3 5.0	3.0 3.0	15.0 11.0	ns	
t <sub>PZH</sub>	Output Enable Time	3.3 5.0	1.0 1.5	14.0 10.5	ns	
t <sub>PZL</sub>	Output Enable Time	3.3 5.0	1.0 1.5	14.0 10.5	ns	
t <sub>PHZ</sub>	Output Disable Time	3.3 5.0	1.0 1.5	16.0 12.5	ns	
t <sub>PLZ</sub>	Output Disable Time	3.3 5.0	1.0 1.5	13.0 10.5	ns	

**Note 8:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	6.5 5.0		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	1.0 1.5		ns	
t <sub>w</sub>	CP Pulse Width, HIGH or LOW	3.3 5.0	6.5 5.0		ns	

**Note 9:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54ACT		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	5.0	70		MHz
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.5	12.0	ns
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.5	11.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	11.5	ns

## AC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54ACT		Units
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Min	Max	
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	11.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	13.0	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	11.0	ns

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

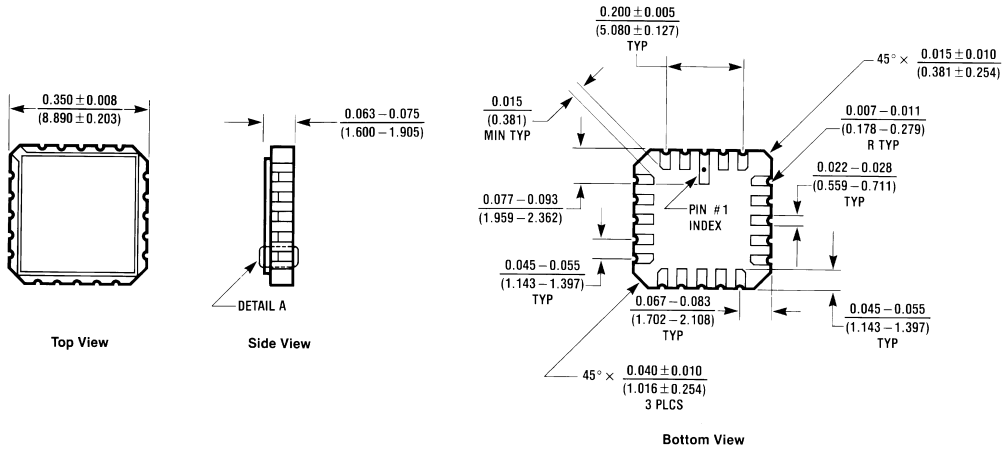
Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	5.5		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.5		ns	
t <sub>w</sub>	CP Pulse Width, HIGH or LOW	5.0	5.0		ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

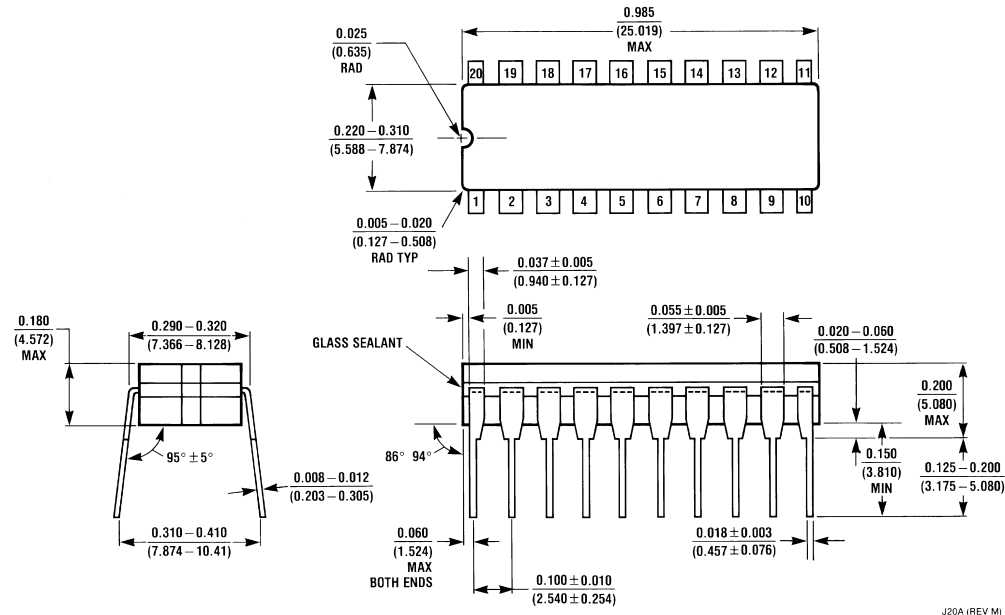
## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	40	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



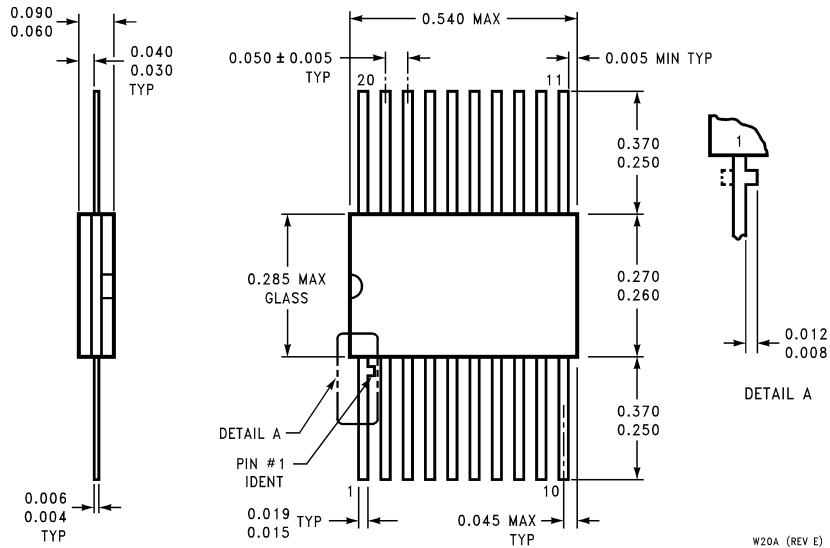
**20 Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E20A



**20 Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J20A



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20 Lead Ceramic Flatpak (F)  
NS Package Number W20A**

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