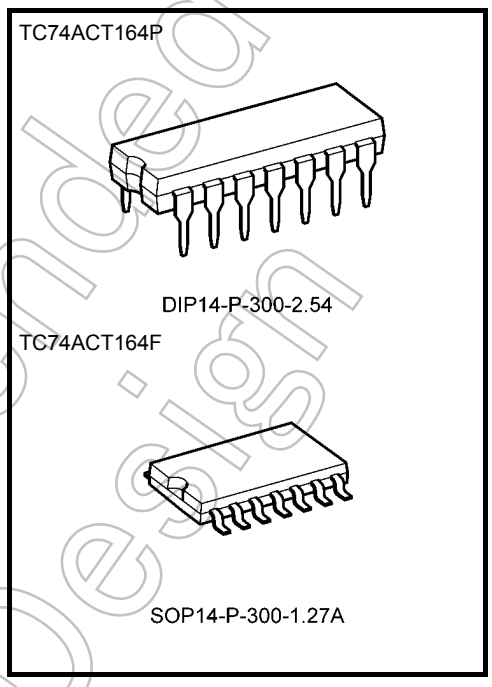
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74ACT164P, TC74ACT164F

8-Bit Shift Register (S-IN, P-OUT)



Weight
DIP14-P-300-2.54 : 0.96 g (typ.)
SOP14-P-300-1.27A : 0.18 g (typ.)

The TC74ACT164 is an advanced high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding $\overline{\text{CLEAR}}$ input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

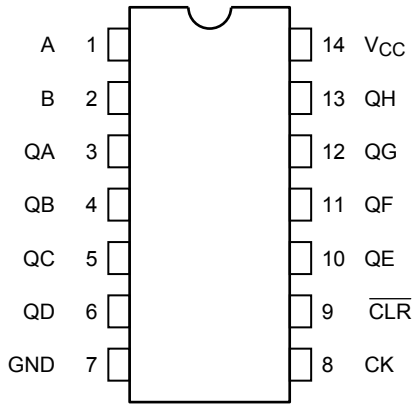
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: f_{max} = 200 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 8 μA (max) at Ta = 25°C
- Compatible with TTL outputs: V_{IL} = 0.8 V (max)
  V_{IH} = 2.0 V (max)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74F164

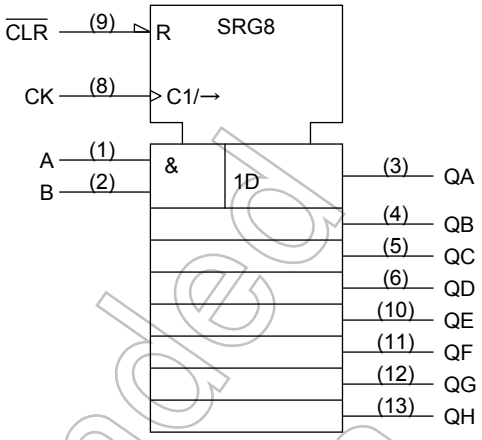
Start of commercial production
1989-11

Pin Assignment



(top view)

IEC Logic Symbol



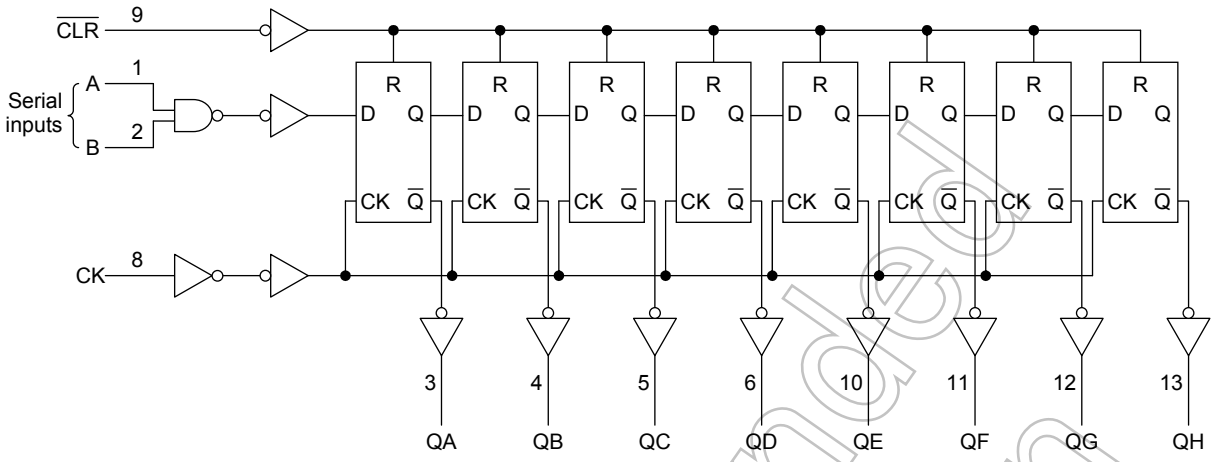
Truth Table

Inputs				Outputs			
$\overline{CLR}$	CK	Serial IN		QA	QB	…	QH
		A	B				
L	X	X	X	L	L	…	L
H	↓	X	X	No change			
H	↑	L	X	L	QA_n	…	QG_n
H	↑	X	L	L	QA_n	…	QG_n
H	↑	H	H	H	QA_n	…	QG_n

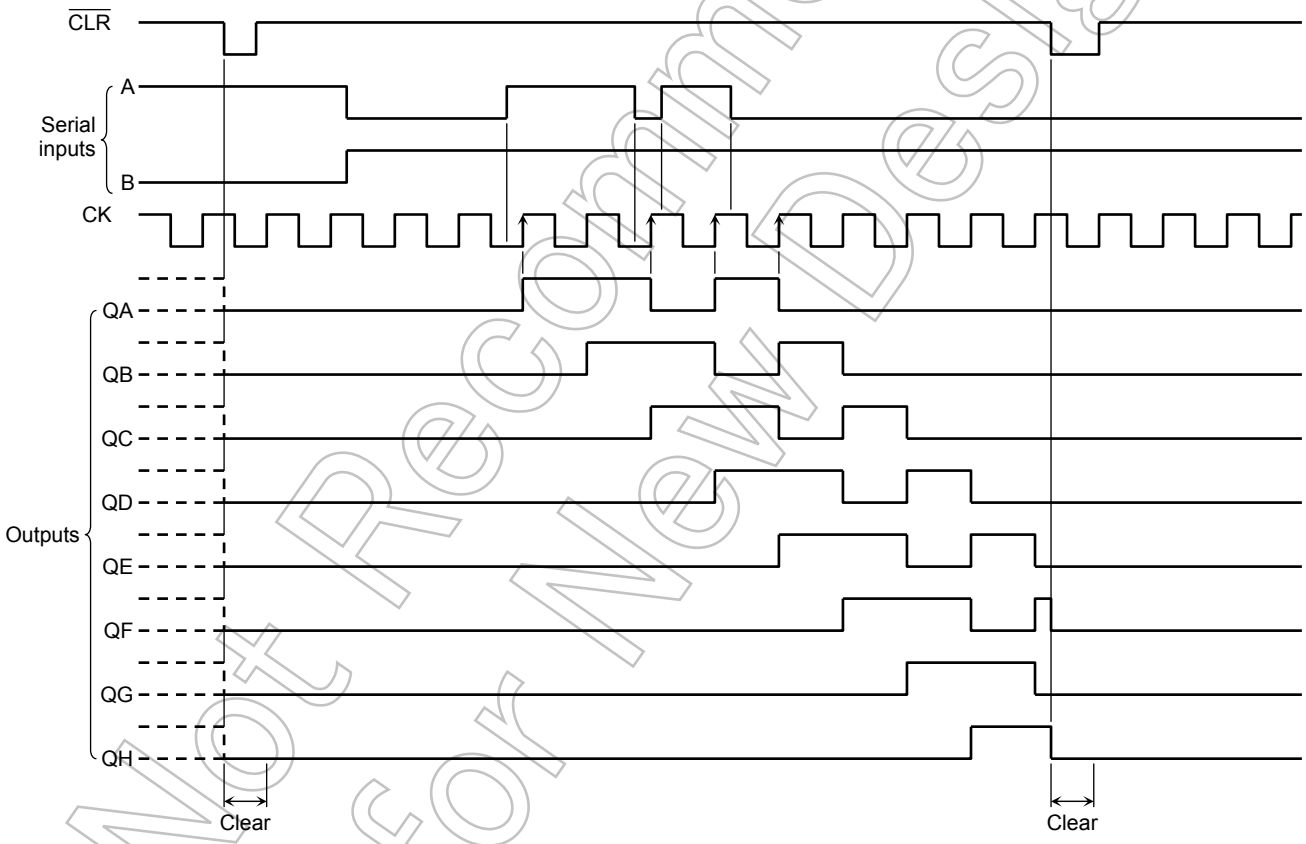
X : Don't care

QA_n~QG_n: The level of QA~QG, respectively, before the most recent positive edge of the clock.

System Diagram



Timing Chart



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC}/ground current	I_{CC}	±200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}			4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}			4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA I_{OH} = −24 mA I_{OH} = −75 mA (Note)	4.5 4.5 5.5	4.4 3.94 —	4.5 — —	— — —	4.4 3.80 3.85	— — —	V
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 24 mA I_{OL} = 75 mA (Note)	4.5 4.5 5.5	— — —	0.0 — —	0.1 0.36 —	— — —	0.1 0.44 1.65	V
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA
	I_C	PER Input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40 to 85°C Limit	Unit
Minimum pulse width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0 ± 0.5	—	5.0	5.0	ns
Minimum pulse width ($\overline{CLR}$)	$t_{W(L)}$		5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t_s		5.0 ± 0.5	—	3.0	3.0	
Minimum hold time	t_h		5.0 ± 0.5	—	2.6	2.6	
Minimum removal time ($\overline{CLR}$)	t_{rem}		5.0 ± 0.5	—	2.0	2.0	

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	—	6.6	11.0	1.0	12.5	ns
Propagation delay time (CLR -Q)	t_{pHL}		5.0 ± 0.5	—	6.9	11.0	1.0	12.5	
Maximum clock frequency	f_{max}		5.0 ± 0.5	80	150	—	80	—	MHz
Input capacitance	C_{IN}			—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)			—	101	—	—	—	

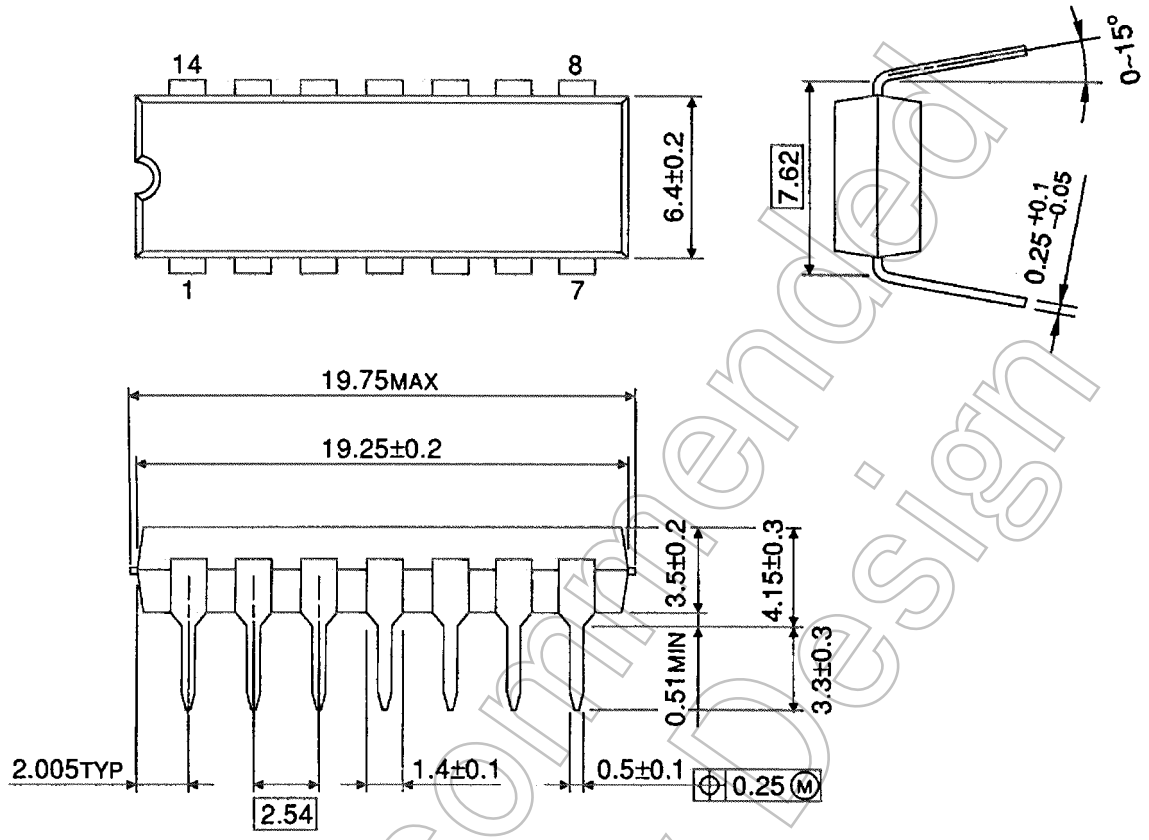
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

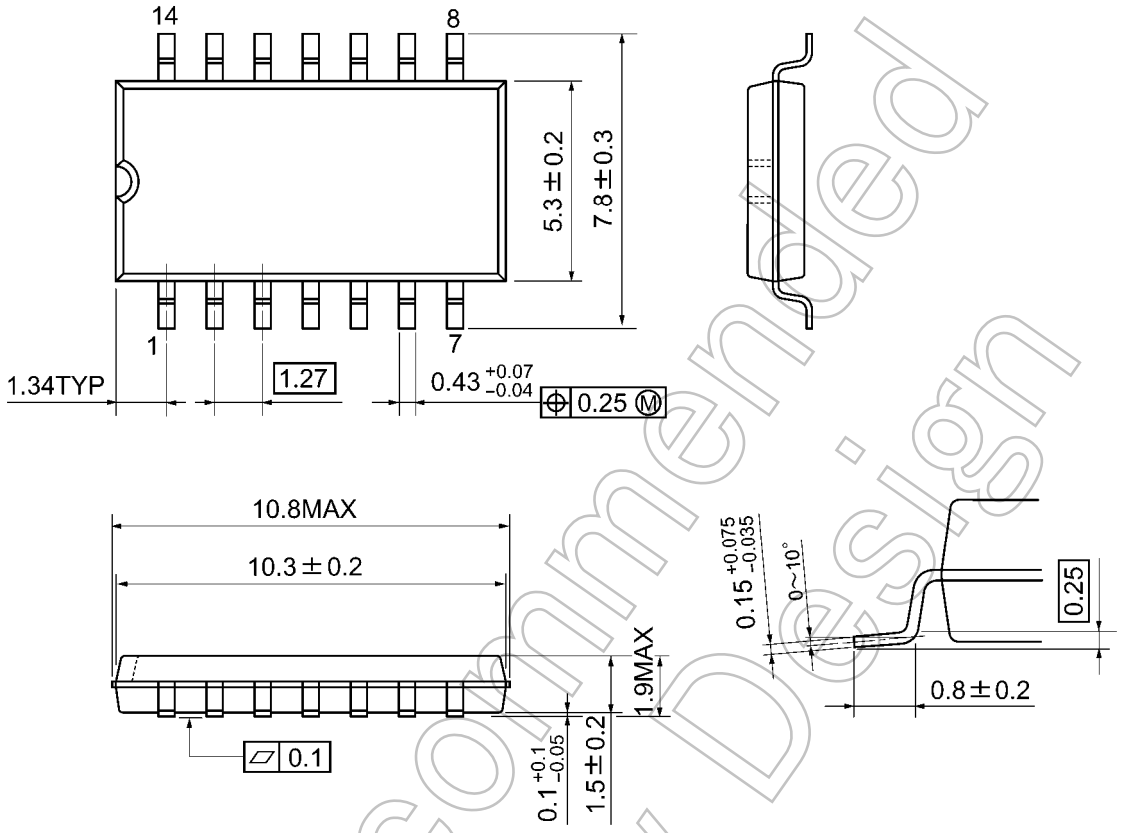
DIP14-P-300-2.54 Unit : mm



Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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