FAIRCHILD SEMICONDUCTOR™

July 1989
Revised October 2000

74ACQ240 • 74ACTQ240
Quiet Series™ Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The ACQ/ACTQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

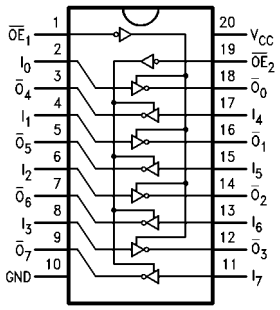
- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inverting 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard ACT240

Ordering Code:

Order Number	Package Number	Package Description
74ACQ240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACQ240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACQ240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACTQ240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACTQ240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ240QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
74ACTQ240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

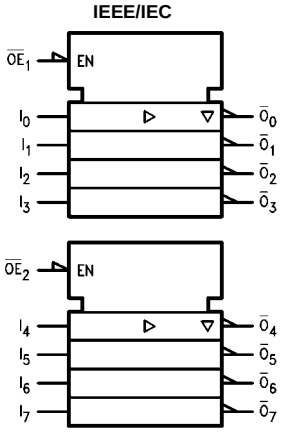
Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Logic Symbol



Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or	
Sink Current	±300 mA
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACQ	2.0V to 6.0V
ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	
ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC}	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
		(V)	Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V_{CC} − 0.1V
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V_{CC} − 0.1V
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V_{IN} = V_{CC} or GND
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

DC Electrical Characteristics for ACQ (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figures 1, 2 (Note 5)(Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	Figures 1, 2 (Note 5)(Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Note 5)(Note 7)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Note 5)(Note 7)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: Plastic DIP package.

Note 6: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 7: Max number of data inputs (n) switching. (n −1) inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 8)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 8)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	Minimum Dynamic Output Current (Note 9)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figures 1, 2 (Note 10)(Note 11)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	Figures 1, 2 (Note 10)(Note 11)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 10)(Note 12)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 10)(Note 12)

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

Note 10: Plastic DIP package.

Note 11: Max number of Data Inputs defined as (n). n−1 Data Inputs are driven 0V to 3V. One Data Input @ V_{IN} = GND.

Note 12: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V) (Note 13)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	3.3	2.0	7.0	10.0	2.0	10.5	ns
t_{PLH}	Data to Output	5.0	1.5	5.0	6.5	1.5	7.0	
t_{PZL}	Output Enable Time	3.3	2.5	8.0	12.0	2.5	12.5	ns
t_{PZH}		5.0	1.5	5.5	8.0	1.5	8.5	
t_{PHZ}	Output Disable Time	3.3	1.0	8.5	13.5	1.0	14.0	ns
t_{PLZ}		5.0	1.0	6.0	9.0	1.0	9.5	
t_{OSHL}	Output to Output Skew	3.3		1.0	1.5		1.5	ns
t_{OSLH}	Data to Output (Note 14)	5.0		0.5	1.0		1.0	

Note 13: Voltage Range 5.0 is 5.0V ± 0.5V

Voltage Range 3.3 is 3.3 ± 0.3V.

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V) (Note 15)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL}	Propagation Delay	5.0	1.5	5.5	7.0	1.5	7.5	ns
t_{PLH}	Data to Output							
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	6.5	8.5	1.5	9.0	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	7.0	9.5	1.0	10.0	ns
t_{OSHL}	Output to Output Skew	5.0		0.5	1.0		1.0	ns
t_{OSLH}	Data to Output (Note 16)							

Note 15: Voltage Range 5.0 is 5.0V ± 0.5V

Note 16: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

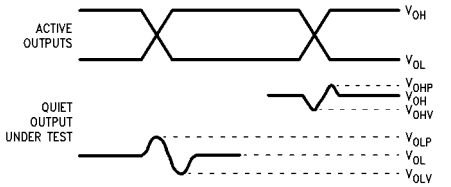
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Note 17: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 18: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

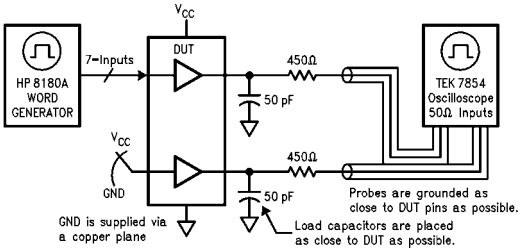
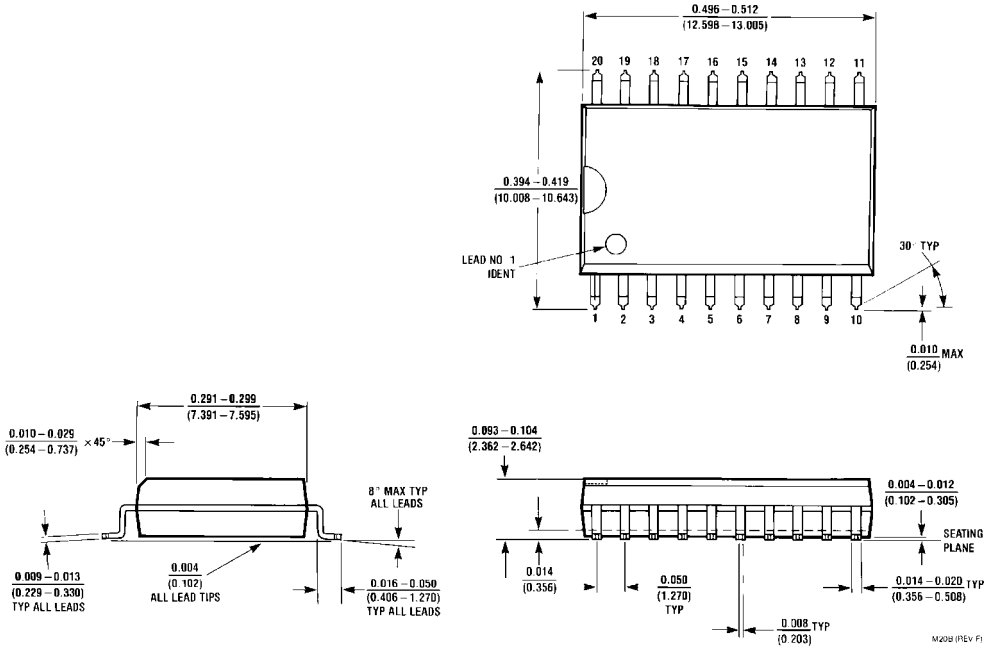


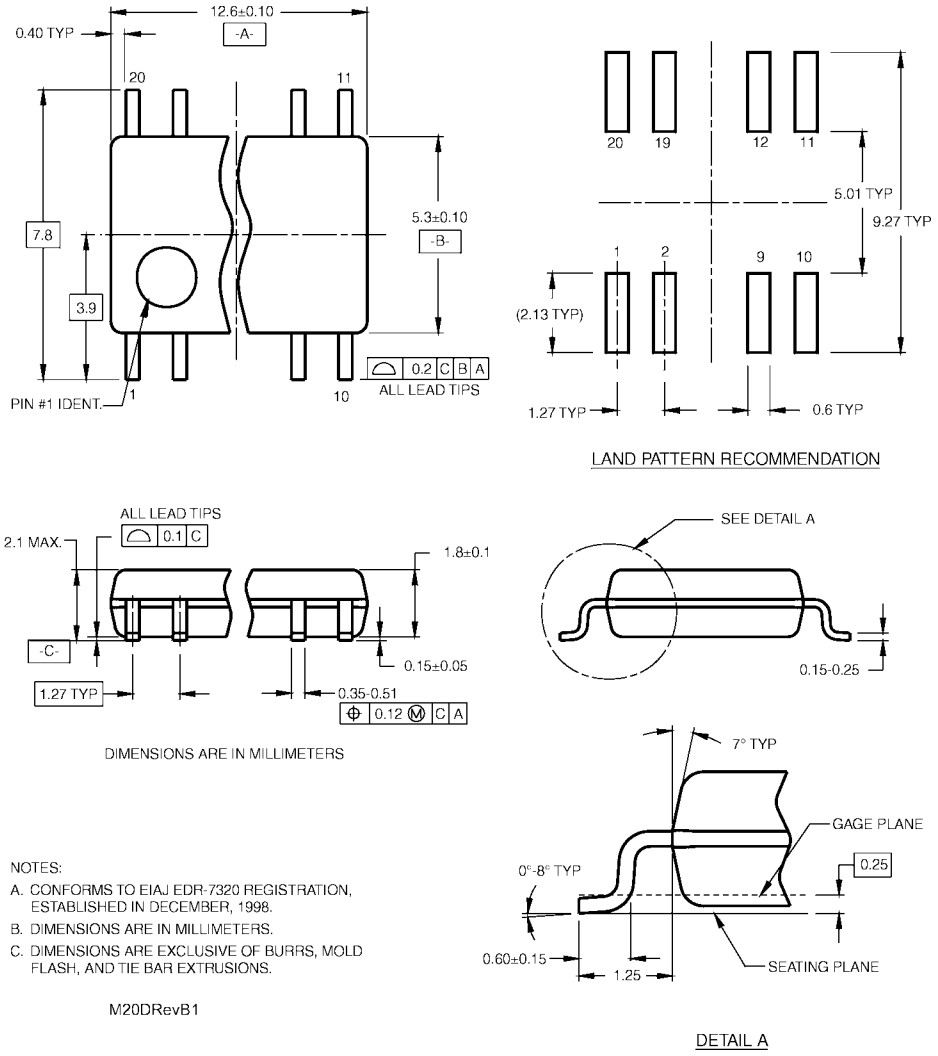
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

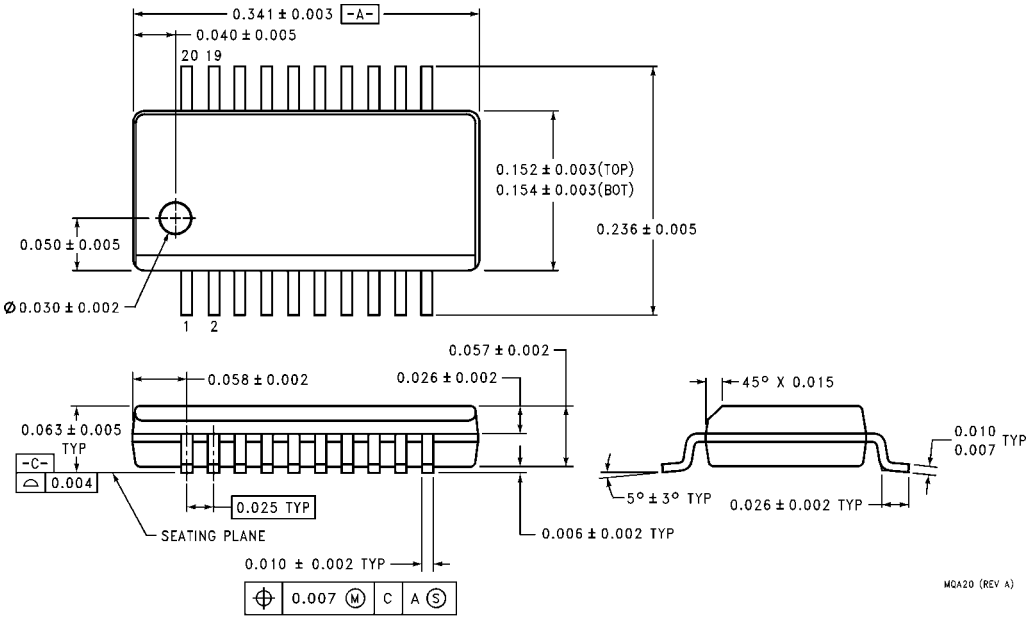
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

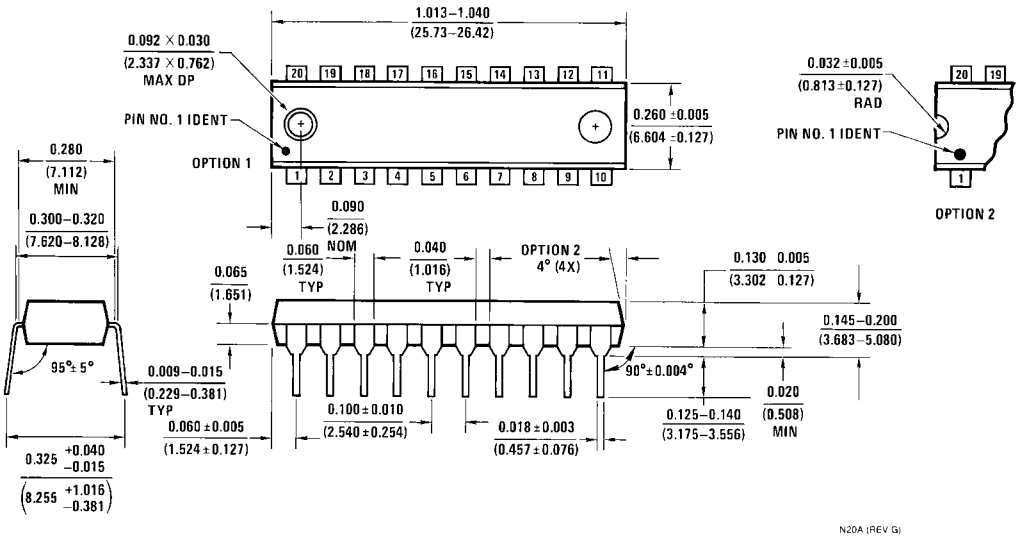
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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