- **High-Performance Floating-Point Digital Signal Processor (DSP)**
  - **TMS320C30-50 (5 V)**
    40-ns Instruction Cycle Time
    275 MOPS, 50 MFLOPS, 25 MIPS
  - **TMS320C30-40 (5 V)**
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
  - **TMS320C30-33 (5 V)**
    60-ns Instruction Cycle Time
    183.3 MOPS, 33.3 MFLOPS, 16.7 MIPS
  - **TMS320C30-27 (5 V)**
    74-ns Instruction Cycle Time
    148.5 MOPS, 27 MFLOPS, 13.5 MIPS
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **32-Bit Instruction Word, 24-Bit Addresses**
- **Two 1K × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks**
- **One 4K × 32-Bit Single-Cycle Dual-Access On-Chip ROM Block**
- **On-Chip Memory-Mapped Peripherals:**
  - **Two Serial Ports**
  - **Two 32-Bit Timers**
  - **One-Channel Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation**
- **Two 32-Bit External Ports**
- **24- and 13-Bit Addresses**
- **0.7-μm Enhanced Performance Implanted CMOS (EPIC™) Technology**
- **208-Pin Plastic Quad Flat Package (PPM Suffix)**
- **181-Pin Grid Array Ceramic Package (GEL Suffix)**
- **Eight Extended-Precision Registers**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two- and Three-Operand Instructions**
- **Parallel Arithmetic and Logic Unit (ALU) and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **Two Sets of Memory Strobes ($\overline{\text{STRB}}$ and $\overline{\text{MSTRB}}$) and One I/O Strobe ($\overline{\text{IOSTRB}}$)**
- **Separate Bus-Control Registers for Each Strobe-Control Wait-State Generation**

description

The TMS320C30 is the newest member of the TMS320C3x generation of DSPs from Texas Instruments (TI™). The TMS320C30 is a 32-bit floating-point processor manufactured in 0.7-μm triple-level-metal CMOS technology.

The TMS320C30's internal busing and special DSP instruction set have the speed and flexibility to execute up to 50 MFLOPS (million floating-point operations per second). The TMS320C30 optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The TMS320C30 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

General-purpose applications are enhanced greatly by the large address space, multiprocessor interface, internally and externally generated wait states, two external interface ports, two timers, serial ports, and multiple interrupt structure. The TMS320C30 supports a wide variety of system applications from host processor to dedicated coprocessor.

description (continued)

High-level language support is implemented easily through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

pinout and pin assignments

TMS320C30 GEL pinout and pin assignments

The TMS320C30 digital signal processor is available in a 181-pin grid array (PGA) package. The pinout of this package is shown in the following two illustrations. The pin assignments are listed in the TMS320C30 GEL pin assignments (alphabetical) table and the TMS320C30 GEL pin assignments (numerical) table.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	H3	D2	D3	D7	D10	D13	D16	D17	D19	D22	D25	D28	XA0	XA1	XA5
B	X2/CLKIN	CV_{SS}	H1	D4	D8	D11	D15	D18	D20	D24	D27	D31	XA4	IV_{SS}	XA6
C	EMU5	X1	DV_{SS}	D0	D5	D9	D14	V_{SS}	D21	D26	D30	XA3	DV_{SS}	XA7	XA10
D	$XR/\overline{W}$	$\overline{XRDY}$	V_{BBP}	DDV_{DD}	D1	D6	D12	V_{DD}	D23	D29	XA2	ADV_{DD}	XA9	XA11	$MC/\overline{MP}$
E	$\overline{RDY}$	$\overline{HOLDA}$	$\overline{MSTRB}$	V_{SUBS}	LOCATOR			DDV_{DD}				XA8	XA12	EMU3	EMU1
F	$\overline{RESET}$	$\overline{STRB}$	$\overline{HOLD}$	$\overline{IOSTRB}$								$EMU4/\overline{SHZ}$	EMU2	EMU0	A0
G	$\overline{IACK}$	XF0	XF1	$R/\overline{W}$								A1	A2	A3	A4
H	$\overline{INT1}$	$\overline{INT0}$	V_{SS}	V_{DD}	MDV_{DD}			TMS320C30 Top View			ADV_{DD}	V_{DD}	V_{SS}	A6	A5
J	$\overline{INT2}$	$\overline{INT3}$	RSV0	RSV1								A11	A9	A8	A7
K	RSV2	RSV3	RSV5	RSV7								A17	A14	A12	A10
L	RSV4	RSV6	RSV9	CLKR1				$IODV_{DD}$				A22	A18	A15	A13
M	RSV8	RSV10	FSR1	PDV_{DD}	CLKX0	EMU6	XD5	V_{DD}	XD16	XD22	XD27	$IODV_{DD}$	A21	A19	A16
N	DR1	CLKX1	DV_{SS}	CLKR0	TCLK1	XD2	XD7	V_{SS}	XD14	XD19	XD23	XD28	DV_{SS}	A23	A20
P	FSX1	DX1	FSR0	TCLK0	XD1	XD4	XD8	XD10	XD13	XD17	XD20	XD24	XD29	CV_{SS}	XD31
R	DR0	FSX0	DX0	XD0	XD3	XD6	XD9	XD11	XD12	XD15	XD18	XD21	XD25	XD26	XD30

TMS320C30 GEL Pinout (Top View)

TMS320C30 GEL pinout and pin assignments (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	XA5	XA1	XA0	D28	D25	D22	D19	D17	D16	D13	D10	D7	D3	D2	H3
B	XA6	IV_{SS}	XA4	D31	D27	D24	D20	D18	D15	D11	D8	D4	H1	CV_{SS}	X2/CLKIN
C	XA10	XA7	DV_{SS}	XA3	D30	D26	D21	V_{SS}	D14	D9	D5	D0	DV_{SS}	X1	EMU5
D	MC/$\overline{\text{MP}}$	XA11	XA9	ADV_{DD}	XA2	D29	D23	V_{DD}	D12	D6	D1	DDV_{DD}	V_{BBP}	$\overline{\text{XRDY}}$	XR/$\overline{\text{W}}$
E	EMU1	EMU3	XA12	XA8				DDV_{DD}			LOCATOR	V_{SUBS}	$\overline{\text{MSTRB}}$	$\overline{\text{HOLDA}}$	$\overline{\text{RDY}}$
F	A0	EMU0	EMU2	EMU4/$\overline{\text{SHZ}}$								$\overline{\text{IOSTRB}}$	$\overline{\text{HOLD}}$	$\overline{\text{STRB}}$	$\overline{\text{RESET}}$
G	A4	A3	A2	A1								R/$\overline{\text{W}}$	XF1	XF0	$\overline{\text{IACK}}$
H	A5	A6	V_{SS}	V_{DD}	ADV_{DD}			TMS320C30 Bottom View			MDV_{DD}	V_{DD}	V_{SS}	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$
J	A7	A8	A9	A11								RSV1	RSV0	$\overline{\text{INT3}}$	$\overline{\text{INT2}}$
K	A10	A12	A14	A17								RSV7	RSV5	RSV3	RSV2
L	A13	A15	A18	A22				$IODV_{DD}$				CLKR1	RSV9	RSV6	RSV4
M	A16	A19	A21	$IODV_{DD}$	XD27	XD22	XD16	V_{DD}	XD5	EMU6	CLKX0	PDV_{DD}	FSR1	RSV10	RSV8
N	A20	A23	DV_{SS}	XD28	XD23	XD19	XD14	V_{SS}	XD7	XD2	TCLK1	CLKR0	DV_{SS}	CLKX1	DR1
P	XD31	CV_{SS}	XD29	XD24	XD20	XD17	XD13	XD10	XD8	XD4	XD1	TCLK0	FSR0	DX1	FSX1
R	XD30	XD26	XD25	XD21	XD18	XD15	XD12	XD11	XD9	XD6	XD3	XD0	DX0	FSX0	DR0

TMS320C30 GEL Pinout (Bottom View)

TMS320C30 GEL Pin Assignments (Alphabetical)†

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
A0	F15	D8	B5	EMU6	M6	V_{BBP}	D3	XD15	R10
A1	G12	D9	C6	FSR0	P3	V_{DD}	D8	XD16	M9
A2	G13	D10	A5	FSR1	M3	V_{DD}	H4	XD17	P10
A3	G14	D11	B6	FSX0	R2	V_{DD}	H12	XD18	R11
A4	G15	D12	D7	FSX1	P1	V_{DD}	M8	XD19	N10
A5	H15	D13	A6	H1	B3	V_{SS}	C8	XD20	P11
A6	H14	D14	C7	H3	A1	V_{SS}	H3	XD21	R12
A7	J15	D15	B7	$\overline{HOLD}$	F3	V_{SS}	H13	XD22	M10
A8	J14	D16	A7	$\overline{HOLDA}$	E2	V_{SS}	N8	XD23	N11
A9	J13	D17	A8	$\overline{IACK}$	G1	V_{SUBS}	E4	XD24	P12
A10	K15	D18	B8	$\overline{INT0}$	H2	X1	C2	XD25	R13
A11	J12	D19	A9	$\overline{INT1}$	H1	X2/CLKIN	B1	XD26	R14
A12	K14	D20	B9	$\overline{INT2}$	J1	XA0	A13	XD27	M11
A13	L15	D21	C9	$\overline{INT3}$	J2	XA1	A14	XD28	N12
A14	K13	D22	A10	$IODV_{DD}$	L8	XA2	D11	XD29	P13
A15	L14	D23	D9	$IODV_{DD}$	M12	XA3	C12	XD30	R15
A16	M15	D24	B10	$\overline{IOSTRB}$	F4	XA4	B13	XD31	P15
A17	K12	D25	A11	IV_{SS}	B14	XA5	A15	XF0	G2
A18	L13	D26	C10	LOCATOR	E5	XA6	B15	XF1	G3
A19	M14	D27	B11	MC/$\overline{MP}$	D15	XA7	C14	$\overline{XRDY}$	D2
A20	N15	D28	A12	MDV_{DD}	H5	XA8	E12	XR/$\overline{W}$	D1
A21	M13	D29	D10	$\overline{MSTRB}$	E3	XA9	D13		
A22	L12	D30	C11	PDV_{DD}	M4	XA10	C15		
A23	N14	D31	B12	$\overline{RDY}$	E1	XA11	D14		
ADV_{DD}	D12	DDV_{DD}	D4	$\overline{RESET}$	F1	XA12	E13		
ADV_{DD}	H11	DDV_{DD}	E8	RSV0	J3	XD0	R4		
CLKR0	N4	DR0	R1	RSV1	J4	XD1	P5		
CLKR1	L4	DR1	N1	RSV2	K1	XD2	N6		
CLKX0	M5	DV_{SS}	C3	RSV3	K2	XD3	R5		
CLKX1	N2	DV_{SS}	C13	RSV4	L1	XD4	P6		
CV_{SS}	B2	DV_{SS}	N3	RSV5	K3	XD5	M7		
CV_{SS}	P14	DV_{SS}	N13	RSV6	L2	XD6	R6		
D0	C4	DX0	R3	RSV7	K4	XD7	N7		
D1	D5	DX1	P2	RSV8	M1	XD8	P7		
D2	A2	EMU0	F14	RSV9	L3	XD9	R7		
D3	A3	EMU1	E15	RSV10	M2	XD10	P8		
D4	B4	EMU2	F13	R/$\overline{W}$	G4	XD11	R8		
D5	C5	EMU3	E14	$\overline{STRB}$	F2	XD12	R9		
D6	D6	EMU4/$\overline{SHZ}$	F12	TCLK0	P4	XD13	P9		
D7	A4	EMU5	C1	TCLK1	N5	XD14	N9		

† ADV_{DD}, CV_{SS}, DDV_{DD}, DV_{SS}, $IODV_{DD}$, IV_{SS}, MDV_{DD}, PDV_{DD}, V_{DD}, and V_{SS} pins are on a common plane internal to the device.

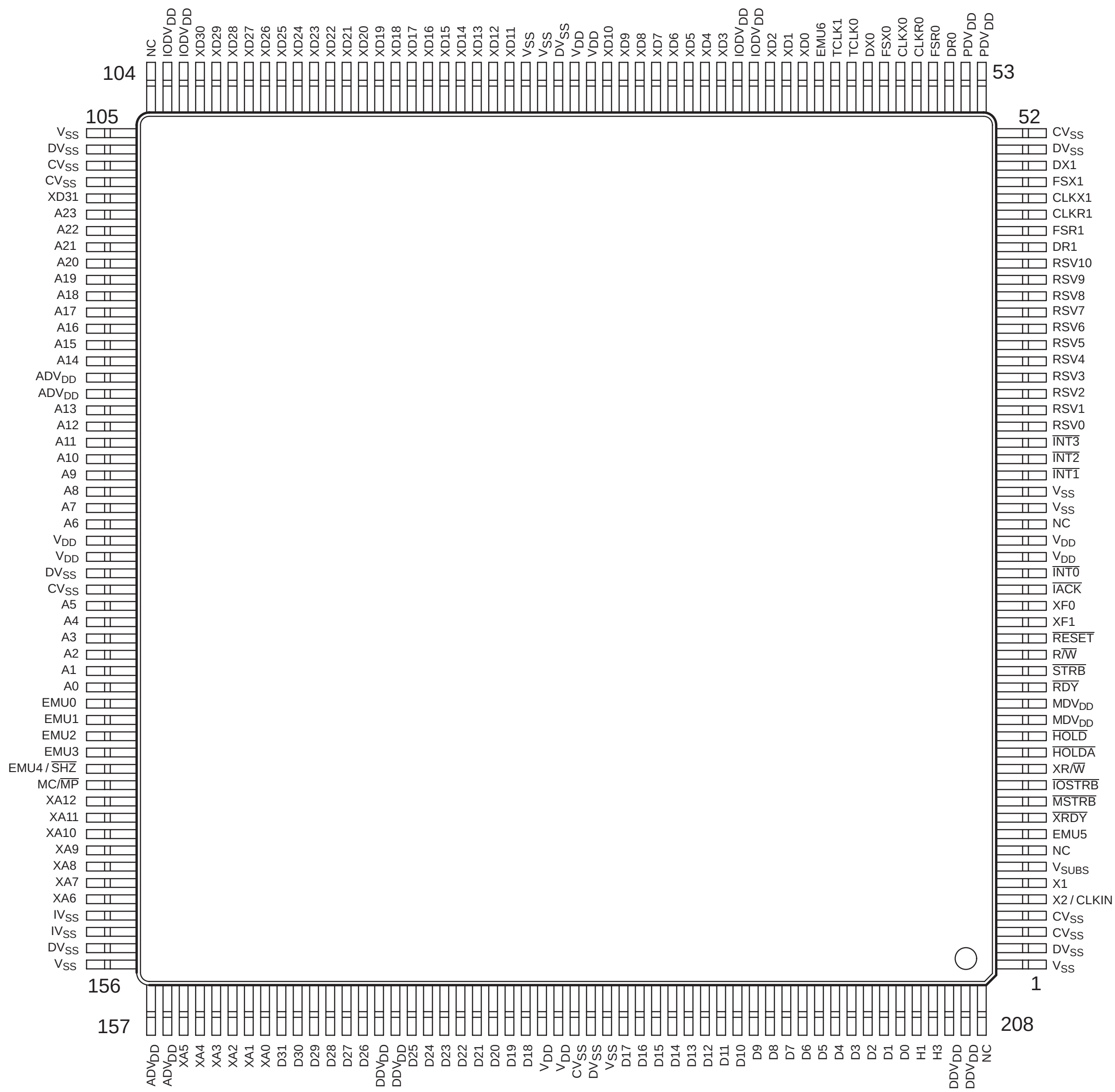
TMS320C30 GEL Pin Assignments (Numerical)†

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
H3	A1	D30	C11	XF1	G3	A13	L15	XD17	P10
D2	A2	XA3	C12	R/$\overline{W}$	G4	RSV8	M1	XD20	P11
D3	A3	DV_{SS}	C13	A1	G12	RSV10	M2	XD24	P12
D7	A4	XA7	C14	A2	G13	FSR1	M3	XD29	P13
D10	A5	XA10	C15	A3	G14	PDV_{DD}	M4	CV_{SS}	P14
D13	A6	XR/$\overline{W}$	D1	A4	G15	CLKX0	M5	XD31	P15
D16	A7	$\overline{XRDY}$	D2	$\overline{INT1}$	H1	EMU6	M6	DR0	R1
D17	A8	V_{BBP}	D3	$\overline{INT0}$	H2	XD5	M7	FSX0	R2
D19	A9	DDV_{DD}	D4	V_{SS}	H3	V_{DD}	M8	DX0	R3
D22	A10	D1	D5	V_{DD}	H4	XD16	M9	XD0	R4
D25	A11	D6	D6	MDV_{DD}	H5	XD22	M10	XD3	R5
D28	A12	D12	D7	ADV_{DD}	H11	XD27	M11	XD6	R6
XA0	A13	V_{DD}	D8	V_{DD}	H12	$IODV_{DD}$	M12	XD9	R7
XA1	A14	D23	D9	V_{SS}	H13	A21	M13	XD11	R8
XA5	A15	D29	D10	A6	H14	A19	M14	XD12	R9
X2/CLKIN	B1	XA2	D11	A5	H15	A16	M15	XD15	R10
CV_{SS}	B2	ADV_{DD}	D12	$\overline{INT2}$	J1	DR1	N1	XD18	R11
H1	B3	XA9	D13	$\overline{INT3}$	J2	CLKX1	N2	XD21	R12
D4	B4	XA11	D14	RSV0	J3	DV_{SS}	N3	XD25	R13
D8	B5	MC/$\overline{MP}$	D15	RSV1	J4	CLKR0	N4	XD26	R14
D11	B6	$\overline{RDY}$	E1	A11	J12	TCLK1	N5	XD30	R15
D15	B7	$\overline{HOLDA}$	E2	A9	J13	XD2	N6		
D18	B8	$\overline{MSTRB}$	E3	A8	J14	XD7	N7		
D20	B9	V_{SUBS}	E4	A7	J15	V_{SS}	N8		
D24	B10	LOCATOR	E5	RSV2	K1	XD14	N9		
D27	B11	DDV_{DD}	E8	RSV3	K2	XD19	N10		
D31	B12	XA8	E12	RSV5	K3	XD23	N11		
XA4	B13	XA12	E13	RSV7	K4	XD28	N12		
IV_{SS}	B14	EMU3	E14	A17	K12	DV_{SS}	N13		
XA6	B15	EMU1	E15	A14	K13	A23	N14		
EMU5	C1	$\overline{RESET}$	F1	A12	K14	A20	N15		
X1	C2	$\overline{STRB}$	F2	A10	K15	FSX1	P1		
DV_{SS}	C3	$\overline{HOLD}$	F3	RSV4	L1	DX1	P2		
D0	C4	$\overline{IOSTRB}$	F4	RSV6	L2	FSR0	P3		
D5	C5	EMU4/$\overline{SHZ}$	F12	RSV9	L3	TCLK0	P4		
D9	C6	EMU2	F13	CLKR1	L4	XD1	P5		
D14	C7	EMU0	F14	$IODV_{DD}$	L8	XD4	P6		
V_{SS}	C8	A0	F15	A22	L12	XD8	P7		
D21	C9	$\overline{IACK}$	G1	A18	L13	XD10	P8		
D26	C10	XF0	G2	A15	L14	XD13	P9		

† ADV_{DD}, CV_{SS}, DDV_{DD}, DV_{SS}, $IODV_{DD}$, IV_{SS}, MDV_{DD}, PDV_{DD}, V_{DD}, and V_{SS} pins are on a common plane internal to the device.

TMS320C30 PPM pinout and pin assignments

The TMS320C30 PPM device is packaged in a 208-pin plastic quad flatpack (PQFP) JEDEC standard package. The following illustration shows the pinout for this package. The pin assignments are listed in the TMS320C30 PPM pin assignments (alphabetical) table and the TMS320C30 PPM pin assignments (numerical) table.



TMS320C30 PPM Pinout

TMS320C30 PPM Pin Assignments (Alphabetical)†

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
A0	139	CV_{SS}	107	D31	165	$\overline{INT2}$	32	TCLK1	62	XD2	66
A1	138	CV_{SS}	108	DDV_{DD}	171	$\overline{INT3}$	33	V_{DD}	26	XD3	69
A2	137	CV_{SS}	133	DDV_{DD}	172	$IODV_{DD}$	67	V_{DD}	27	XD4	70
A3	136	CV_{SS}	183	DDV_{DD}	206	$IODV_{DD}$	68	V_{DD}	77	XD5	71
A4	135	D0	203	DDV_{DD}	207	$IODV_{DD}$	102	V_{DD}	78	XD6	72
A5	134	D1	202	DR0	55	$IODV_{DD}$	103	V_{DD}	130	XD7	73
A6	129	D2	201	DR1	45	$\overline{IOSTRB}$	12	V_{DD}	131	XD8	74
A7	128	D3	200	DV_{SS}	2	IV_{SS}	153	V_{DD}	181	XD9	75
A8	127	D4	199	DV_{SS}	51	IV_{SS}	154	V_{DD}	182	XD10	76
A9	126	D5	198	DV_{SS}	105	MC/$\overline{MP}$	145	V_{SS}	1	XD11	82
A10	125	D6	197	DV_{SS}	106	MDV_{DD}	16	V_{SS}	29	XD12	83
A11	124	D7	196	DV_{SS}	132	MDV_{DD}	17	V_{SS}	30	XD13	84
A12	123	D8	195	DV_{SS}	155	$\overline{MSTRB}$	11	V_{SS}	80	XD14	85
A13	122	D9	194	DV_{SS}	156	NC	8	V_{SS}	81	XD15	86
A14	119	D10	193	DV_{SS}	184	NC	28	V_{SS}	105	XD16	87
A15	118	D11	192	DX0	60	NC	104	V_{SS}	156	XD17	88
A16	117	D12	191	DX1	50	NC	208	V_{SS}	185	XD18	89
A17	116	D13	190	EMU0	140	PDV_{DD}	53	V_{SUBS}	7	XD19	90
A18	115	D14	189	EMU1	141	PDV_{DD}	54	X1	6	XD20	91
A19	114	D15	188	EMU2	142	$\overline{RDY}$	18	X2/CLKIN	5	XD21	92
A20	113	D16	187	EMU3	143	$\overline{RESET}$	21	XA0	164	XD22	93
A21	112	D17	186	EMU4/$\overline{SHZ}$	144	RSV0	34	XA1	163	XD23	94
A22	111	D18	180	EMU5	9	RSV1	35	XA2	162	XD24	95
A23	110	D19	179	EMU6	63	RSV2	36	XA3	161	XD25	96
ADV_{DD}	120	D20	178	FSR0	56	RSV3	37	XA4	160	XD26	97
ADV_{DD}	121	D21	177	FSR1	46	RSV4	38	XA5	159	XD27	98
ADV_{DD}	157	D22	176	FSX0	59	RSV5	39	XA6	152	XD28	99
ADV_{DD}	158	D23	175	FSX1	49	RSV6	40	XA7	151	XD29	100
CLKR0	57	D24	174	H1	204	RSV7	41	XA8	150	XD30	101
CLKR1	47	D25	173	H3	205	RSV8	42	XA9	148	XD31	109
CLKX0	58	D26	170	$\overline{HOLD}$	15	RSV9	43	XA10	149	XF0	23
CLKX1	48	D27	169	$\overline{HOLDA}$	14	RSV10	44	XA11	147	XF1	22
CV_{SS}	3	D28	168	$\overline{IACK}$	24	R/$\overline{W}$	20	XA12	146	$\overline{XRDY}$	10
CV_{SS}	4	D29	167	$\overline{INT0}$	25	$\overline{STRB}$	19	XD0	64	XR/$\overline{W}$	13
CV_{SS}	52	D30	166	$\overline{INT1}$	31	TCLK0	61	XD1	65		

† ADV_{DD}, CV_{SS}, DDV_{DD}, DV_{SS}, $IODV_{DD}$, IV_{SS}, MDV_{DD}, PDV_{DD}, V_{DD}, and V_{SS} pins are on a common plane internal to the device.

TMS320C30 PPM Pin Assignments (Numerical)†

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	RSV9	85	XD14	127	A8	169	D27
2	DV_{SS}	44	RSV10	86	XD15	128	A7	170	D26
3	CV_{SS}	45	DR1	87	XD16	129	A6	171	DDV_{DD}
4	CV_{SS}	46	FSR1	88	XD17	130	V_{DD}	172	DDV_{DD}
5	X2/CLKIN	47	CLKR1	89	XD18	131	V_{DD}	173	D25
6	X1	48	CLKX1	90	XD19	132	DV_{SS}	174	D24
7	V_{SUBS}	49	FSX1	91	XD20	133	CV_{SS}	175	D23
8	NC	50	DX1	92	XD21	134	A5	176	D22
9	EMU5	51	DV_{SS}	93	XD22	135	A4	177	D21
10	$\overline{XRDY}$	52	CV_{SS}	94	XD23	136	A3	178	D20
11	$\overline{MSTRB}$	53	PDV_{DD}	95	XD24	137	A2	179	D19
12	$\overline{IOSTRB}$	54	PDV_{DD}	96	XD25	138	A1	180	D18
13	$XR/\overline{W}$	55	DR0	97	XD26	139	A0	181	V_{DD}
14	$\overline{HOLDA}$	56	FSR0	98	XD27	140	EMU0	182	V_{DD}
15	$\overline{HOLD}$	57	CLKR0	99	XD28	141	EMU1	183	CV_{SS}
16	MDV_{DD}	58	CLKX0	100	XD29	142	EMU2	184	DV_{SS}
17	MDV_{DD}	59	FSX0	101	XD30	143	EMU3	185	V_{SS}
18	$\overline{RDY}$	60	DX0	102	$IODV_{DD}$	144	$EMU4/\overline{SHZ}$	186	D17
19	$\overline{STRB}$	61	TCLK0	103	$IODV_{DD}$	145	$MC/\overline{MP}$	187	D16
20	$R/\overline{W}$	62	TCLK1	104	NC	146	XA12	188	D15
21	$\overline{RESET}$	63	EMU6	105	V_{SS}	147	XA11	189	D14
22	XF1	64	XD0	106	DV_{SS}	148	XA10	190	D13
23	XF0	65	XD1	107	CV_{SS}	149	XA9	191	D12
24	$\overline{IACK}$	66	XD2	108	CV_{SS}	150	XA8	192	D11
25	$\overline{INT0}$	67	$IODV_{DD}$	109	XD31	151	XA7	193	D10
26	V_{DD}	68	$IODV_{DD}$	110	A23	152	XA6	194	D9
27	V_{DD}	69	XD3	111	A22	153	IV_{SS}	195	D8
28	NC	70	XD4	112	A21	154	IV_{SS}	196	D7
29	V_{SS}	71	XD5	113	A20	155	DV_{SS}	197	D6
30	V_{SS}	72	XD6	114	A19	156	V_{SS}	198	D5
31	$\overline{INT1}$	73	XD7	115	A18	157	ADV_{DD}	199	D4
32	$\overline{INT2}$	74	XD8	116	A17	158	ADV_{DD}	200	D3
33	$\overline{INT3}$	75	XD9	117	A16	159	XA5	201	D2
34	RSV0	76	XD10	118	A15	160	XA4	202	D1
35	RSV1	77	V_{DD}	119	A14	161	XA3	203	D0
36	RSV2	78	V_{DD}	120	ADV_{DD}	162	XA2	204	H1
37	RSV3	79	DV_{SS}	121	ADV_{DD}	163	XA1	205	H3
38	RSV4	80	V_{SS}	122	A13	164	XA0	206	DDV_{DD}
39	RSV5	81	V_{SS}	123	A12	165	D31	207	DDV_{DD}
40	RSV6	82	XD11	124	A11	166	D30	208	NC
41	RSV7	83	XD12	125	A10	167	D29		
42	RSV8	84	XD13	126	A9	168	D28		

† ADV_{DD}, CV_{SS}, DDV_{DD}, DV_{SS}, $IODV_{DD}$, IV_{SS}, MDV_{DD}, PDV_{DD}, V_{DD}, and V_{SS} pins are on a common plane internal to the device.

pin functions

This section provides signal descriptions for the TMS320C30 in the microprocessor mode. The following tables list each signal, the number of pins, type of operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z), and a brief description of its function. All pins labeled NC have special functions and should not be connected by the user. A line over a signal name (for example, $\overline{\text{RESET}}$) indicates that the signal is active low (true at logic 0 level). The signals are grouped according to function.

TMS320C30 Pin Functions

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§		
PRIMARY BUS INTERFACE						
D31–D0	32	I/O/Z	32-bit data port of the primary bus interface	S	H	R
A23–A0	24	O/Z	24-bit address port of the primary bus interface	S	H	R
R/$\overline{\text{W}}$	1	O/Z	Read/write for primary bus interface. R/$\overline{\text{W}}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{\text{STRB}}$	1	O/Z	External access strobe for the primary bus interface	S	H	
$\overline{\text{RDY}}$	1	I	Ready. $\overline{\text{RDY}}$ indicates that the external device is prepared for a primary-bus-interface transaction to complete.			
$\overline{\text{HOLD}}$	1	I	Hold for primary bus interface. When $\overline{\text{HOLD}}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and all transactions over the primary bus interface are held until $\overline{\text{HOLD}}$ becomes a logic high or the NOHOLD bit of the primary-bus-control register is set.			
$\overline{\text{HOLDA}}$	1	O/Z	Hold acknowledge for primary bus interface. $\overline{\text{HOLDA}}$ is generated in response to a logic low on $\overline{\text{HOLD}}$. $\overline{\text{HOLDA}}$ indicates that A23–A0, D31–D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{\text{HOLDA}}$ is high in response to a logic high of $\overline{\text{HOLD}}$ or when the NOHOLD bit of the primary-bus-control register is set.	S		
EXPANSION BUS INTERFACE						
XD31–XD0	32	I/O/Z	32-bit data port of the expansion bus interface	S		R
XA12–XA0	13	O/Z	13-bit address port of the expansion bus interface	S		R
XR/$\overline{\text{W}}$	1	O/Z	Read/write signal for expansion bus interface. When a read is performed, XR/$\overline{\text{W}}$ is held high; when a write is performed, XR/$\overline{\text{W}}$ is low.	S		R
$\overline{\text{MSTRB}}$	1	O/Z	External memory access strobe for the expansion bus interface	S		
$\overline{\text{IOSTRB}}$	1	O/Z	External I/O access strobe for the expansion bus interface	S		
$\overline{\text{XRDY}}$	1	I	Ready signal. $\overline{\text{XRDY}}$ indicates that the external device is prepared for an expansion-bus-interface transaction to complete.			
CONTROL SIGNALS						
$\overline{\text{RESET}}$	1	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When $\overline{\text{RESET}}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{\text{INT3}}$–$\overline{\text{INT0}}$	4	I	External interrupts			
$\overline{\text{IACK}}$	1	O/Z	Interrupt acknowledge. $\overline{\text{IACK}}$ is generated by the IACK instruction. $\overline{\text{IACK}}$ can be used to indicate the beginning or end of an interrupt-service routine.	S		
MC/$\overline{\text{MP}}$	1	I	Microcomputer/microprocessor mode			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instructions.	S		R

† I = input, O = output, Z = high-impedance state. All pins labeled NC have specified functions and should not be connected by the user.
‡ Quantity is the same for GEL and PPM packages unless otherwise noted.
§ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active

TMS320C30 Pin Functions (Continued)

PIN NAME	QTY‡		TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§	
SERIAL PORT 0 SIGNALS						
CLKX0	1		I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S	R
DX0	1		I/O/Z	Data transmit output. Serial port 0 transmits serial data on DX0.	S	R
FSX0	1		I/O/Z	Frame synchronization pulse for transmit. The FSX0 pulse initiates the transmit data process over DX0.	S	R
CLKR0	1		I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S	R
DR0	1		I/O/Z	Data receive. Serial port 0 receives serial data on DR0.	S	R
FSR0	1		I/O/Z	Frame synchronization pulse for receive. The FSR0 pulse initiates the receive data process over DR0.	S	R
SERIAL PORT 1 SIGNALS						
CLKX1	1		I/O/Z	Serial port 1 transmit clock. CLKX1 is the serial shift clock for the serial port 1 transmitter.	S	R
DX1	1		I/O/Z	Data transmit output. Serial port 1 transmits serial data on DX1.	S	R
FSX1	1		I/O/Z	Frame synchronization pulse for transmit. The FSX1 pulse initiates the transmit data process over DX1.	S	R
CLKR1	1		I/O/Z	Serial port 1 receive clock. CLKR1 is the serial shift clock for the serial port 1 receiver.	S	R
DR1	1		I/O/Z	Data receive. Serial port 1 receives serial data on DR1.	S	R
FSR1	1		I/O/Z	Frame synchronization pulse for receive. The FSR1 pulse initiates the receive data process over DR1.	S	R
TIMER 0 SIGNAL						
TCLK0	1		I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TIMER 1 SIGNAL						
TCLK1	1		I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS						
	GEL	PPM				
V_{DD}	4	8	I	5 V supply¶		
$IODV_{DD}$	2	4	I	5 V supply¶		
ADV_{DD}	2	4	I	5 V supply¶		
PDV_{DD}	1	2	I	5 V supply¶		
DDV_{DD}	2	4	I	5 V supply¶		
MDV_{DD}	1	2	I	5 V supply¶		
V_{SS}	4	8	I	Ground		
DV_{SS}	4	8	I	Ground		
CV_{SS}	2	4	I	Ground		
IV_{SS}	2	1	I	Ground		

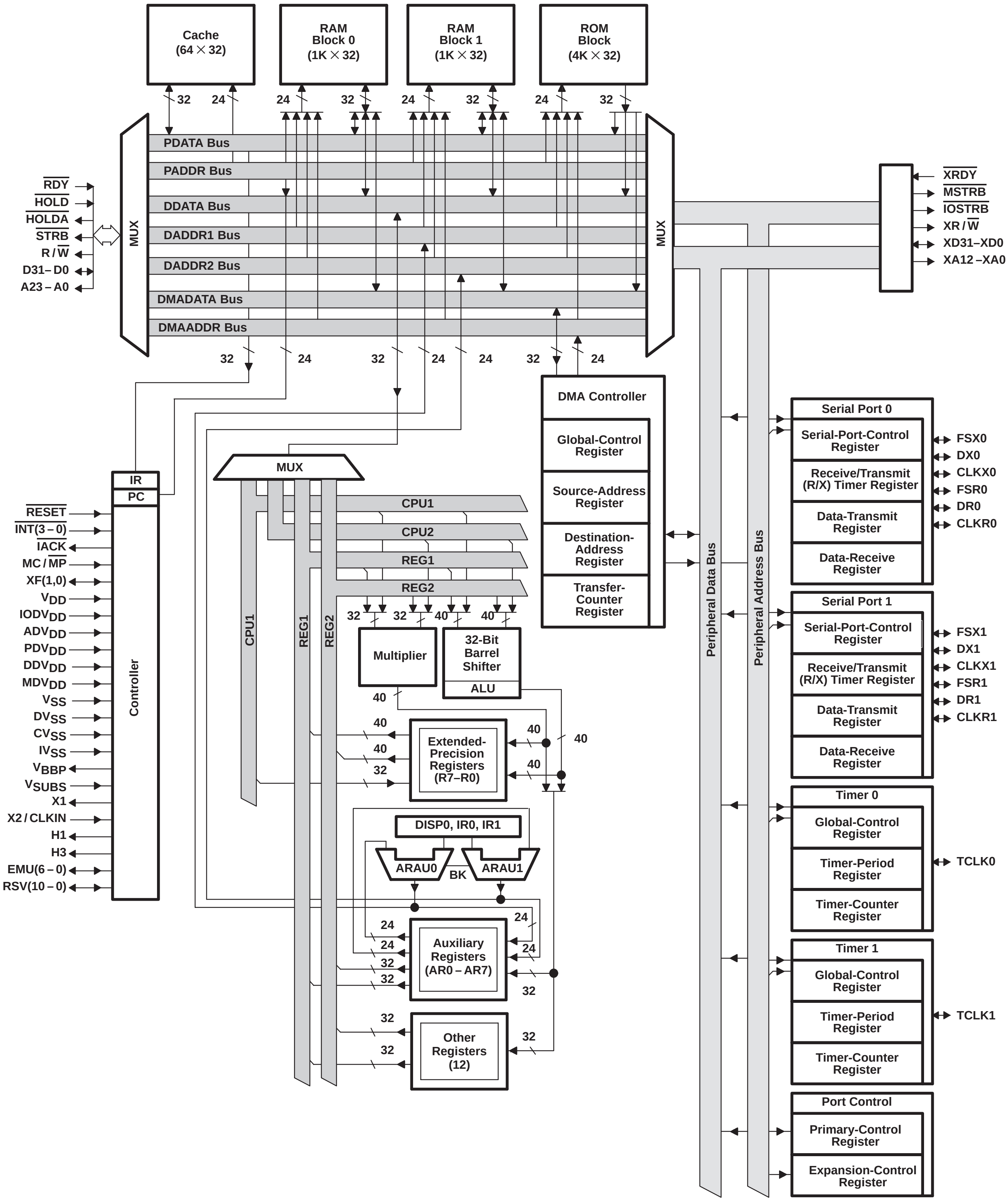
† I = input, O = output, Z = high-impedance state. All pins labeled NC have special functions and should not be connected by the user.
‡ Quantity is the same for GEL and PPM packages unless otherwise noted.
§ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
¶ Recommended decoupling capacitor is 0.1 μF.

TMS320C30 Pin Functions (Continued)

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§
SUPPLY AND OSCILLATOR SIGNALS (CONTINUED)				
V_{BBP}	1	NC	V_{BB} pump oscillator output	
V_{SUBS}	1	I	Substrate terminal. Tie to ground.	
X1	1	O	Output from the internal oscillator for the crystal. If a crystal is not used, X1 should be left unconnected.	
X2/CLKIN	1	I	Input to the internal oscillator from the crystal or a clock	
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
RESERVED¶				
EMU0–EMU2	3	I	Reserved. Use pullup resistors to 5 V.	
EMU3	1	O/Z	Reserved	S
EMU4/$\overline{SHZ}$	1	I	Shutdown high impedance. When active, EMU4/$\overline{SHZ}$ shuts down the TMS320C30 and places all pins in the high-impedance state. EMU4/$\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts TMS320C30 memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.	
EMU5, EMU6	2	NC	Reserved	
RSV10–RSV5	6	I/O	Reserved. Use pullup resistors to 5 V.	
RSV4–RSV0	5	I	Reserved. Tie pins directly to 5 V.	
Locator	1#	NC	Reserved	

† I = input, O = output, Z = high-impedance state. All pins labeled NC have special functions and should not be connected by the user.
‡ Quantity is the same for GEL and PPM packages unless otherwise noted.
§ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
¶ Follow the connections specified for the reserved pins. Use 18-kΩ – 22-kΩ pullup resistors for best results. All 5-V supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.
# For the GEL package only. There is no locator in the PPM package.

functional block diagram



memory map

Figure 1 depicts the memory map for the TMS320C30. Refer to the *TMS320C3x User's Guide* (literature number SPRU031) for a detailed description of this memory mapping. Figure 2 shows the reset, interrupt, and trap vector/branches memory-map locations. Figure 3 shows the peripheral bus memory-mapped registers.

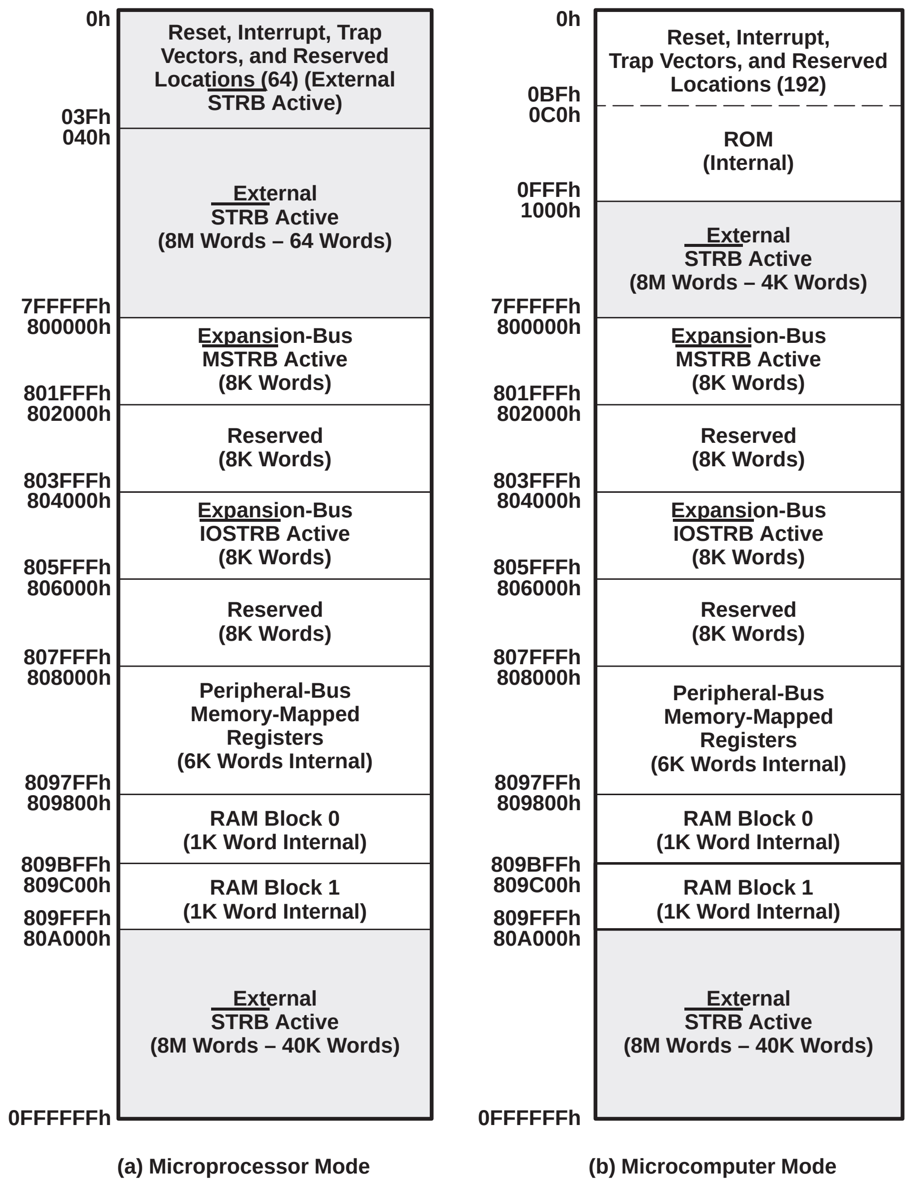


Figure 1. TMS320C30 Memory Map

memory map (continued)

00h	Reset
01h	$\overline{\text{INT0}}$
02h	$\overline{\text{INT1}}$
03h	$\overline{\text{INT2}}$
04h	$\overline{\text{INT3}}$
05h	XINT0
06h	RINT0
07h	XINT1
08h	RINT1
09h	TINT0
0Ah	TINT1
0Bh	DINT
0Ch–1Fh	Reserved
20h	TRAP 0
	. . .
3Bh	TRAP 27
3Ch–3Fh	Reserved

(a) Microprocessor Mode

00h	Reset
01h	$\overline{\text{INT0}}$
02h	$\overline{\text{INT1}}$
03h	$\overline{\text{INT2}}$
04h	$\overline{\text{INT3}}$
05h	XINT0
06h	RINT0
07h	XINT1
08h	RINT1
09h	TINT0
0Ah	TINT1
0Bh	DINT
0Ch–1Fh	Reserved
20h	TRAP 0
	. . .
3Bh	TRAP 27
3Ch–BFh	Reserved

(a) Microcomputer Mode

Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Port 0 Global Control
808042h	FSX/DX/CLKX Serial Port 0 Control
808043h	FSR/DR/CLKR Serial Port 0 Control
808044h	Serial Port 0 R/X Timer Control
808045h	Serial Port 0 R/X Timer Counter
808046h	Serial Port 0 R/X Timer Period
808048h	Serial Port 0 Data Transmit
80804Ch	Serial Port 0 Data Receive
808050h	Serial Port 1 Global Control
808052h	FSX/DX/CLKX Serial Port 1 Control
808053h	FSR/DR/CLKR Serial Port 1 Control
808054h	Serial Port 1 R/X Timer Control
808055h	Serial Port 1 R/X Timer Counter
808056h	Serial Port 1 R/X Timer Period
808058h	Serial Port 1 Data Transmit
80805Ch	Serial Port 1 Data Receive
808060h	Expansion-Bus Control
808064h	Primary-Bus Control

† Shading denotes reserved address locations

Figure 3. Peripheral Bus Memory-Mapped Registers†

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.3 V to 7 V
Input voltage range, V_I . . . . – 0.3 V to 7 V
Output voltage range, V_O . . . . –0.3 V to 7 V
Continuous power dissipation (see Note 2) . . . . 3.15 W
Operating case temperature range, T_C . . . . 0°C to 85°C
Storage temperature range, T_{stg} . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. Actual operating power is less. This value is obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 3)

			MIN	NOM‡	MAX	UNIT
V_{DD}	Supply voltage (AV_{DD}, etc.)		4.75	5	5.25	V
V_{SS}	Supply voltage (CV_{SS}, etc.)			0		V
V_{IH}	High-level input voltage	All other pins	2		V_{DD} + 0.3§	V
		CLKIN	2.6		V_{DD} + 0.3§	
V_{IL}	Low-level input voltage		– 0.3§		0.8	V
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		85	°C

‡ All nominal values are at V_{DD} = 5 V, T_A (ambient air temperature)= 25°C.
§ These values are derived from characterization and not tested.
NOTE 3: All input and output voltage levels are TTL-compatible.

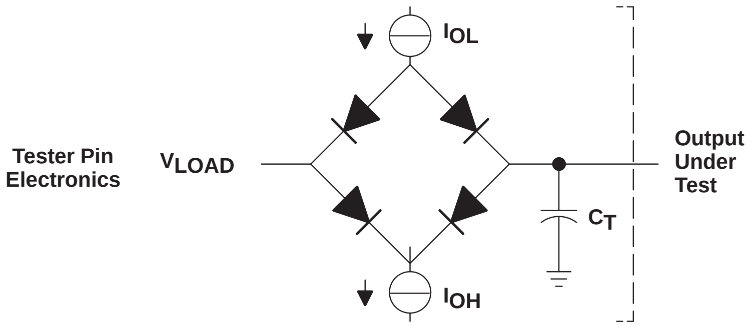
electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = MIN, I_{OH} = MAX		2.4	3		V
V_{OL}	Low-level output voltage		V_{DD} = MIN, I_{OL} = MAX			0.3	0.6§	V
I_Z	High-impedance current		V_{DD} = MAX		– 20		20	µA
I_I	Input current		$V_I = V_{SS}$ to V_{DD}		– 10		10	µA
I_{IP}	Input current		Inputs with internal pullups (see Note 4)		– 600		20	µA
I_{CC}	Supply current		T_A = 25°C, V_{DD} = MAX, $t_{c(CI)}$ = MIN, See Note 5	’320C30-27		130	600	mA
				’320C30-33		150	600	
				’320C30-40		175	600	
				’320C30-50		200	600	
C_i	Input capacitance	CLKIN					25	pF
		All other inputs					15	
C_o	Output capacitance						20¶	pF

† For conditions shown as MIN / MAX, use the appropriate value specified in recommended operating conditions.
‡ All typical values are at V_{DD} = 5 V, T_A (ambient air temperature)= 25°C.
§ These values are derived from characterization but not tested.
¶ These values are derived by design but not tested.

NOTES: 3. All input and output voltage levels are TTL-compatible.
4. Pins with internal pullup devices: $\overline{\text{INT0}}$–$\overline{\text{INT3}}$, MC / $\overline{\text{MP}}$, RSV0 – RSV10. Although RSV0 – RSV10 have internal pullup devices, external pullups should be used on each pin as identified in the pin functions tables.
5. Actual operating current is less than this maximum value. This value is obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 2.15 V
C_T = 80-pF typical load-circuit capacitance

Figure 4. Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows (see Figure 5):

- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

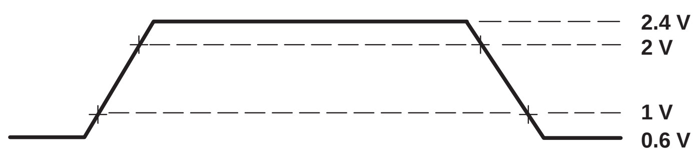


Figure 5. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows (see Figure 6):

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2 V and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2 V.

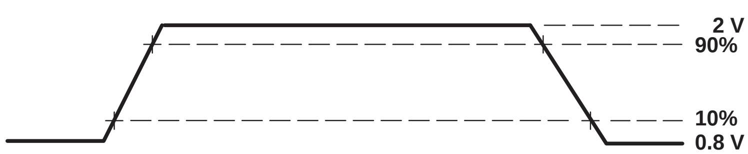


Figure 6. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	(L)A30 – (L)A0 or (L)Ax	IOS	$\overline{\text{IOSTRB}}$
ASYNCH	Asynchronous reset signals in the high-impedance state	(M)S	$\overline{\text{(M)STRB}}$, includes $\overline{\text{STRB}}$ and $\overline{\text{MSTRB}}$
CH	CLKX0 and CLKX1	RDY	$\overline{\text{RDY}}$
CI	CLKIN	RESET	$\overline{\text{RESET}}$
CLKR	CLKR0 and CLKR1	RW	R / $\overline{\text{W}}$
CONTROL	Control signals	S	$\overline{\text{(M)S}}$, which includes $\overline{\text{MSTRB}}$, $\overline{\text{STRB}}$; and IOS, $\overline{\text{IOSTRB}}$
D	D31 – D0 or Dx	SCK	CLKX/R, includes CLKX0, CLKX1, CLKR0, and CLKR1
DR	DR0 and DR1	TCLK	TCLK0 and TCLK1
DX	DX0 and DX1	XA	XA12 – XA0 or XAx
FS	FSX/R, includes FSX0, FSX1, FSR0, and FSR1	(X)A	Includes A23 – A0 and XA12 – XA0
FSR	FSR0 and RSR1	XD	XD31 –XD0 or XDx
FSX	FSX0 and FSX1	(X)D	Includes D31 – D0 and XD31 – XD0
GPIO	General-purpose input/output (peripheral pins include CLKX0/1, CLKR01, DX0/1, DR0/1, FSX0/1, FSR0/1, TCLK0/1)	XF	XFx, includes XF0 and XF1
H	H1 and H3	XF0	XF0
H1	H1	XF1	XF1
H3	H3	XFIO	XFx switching from input to output
HOLD	$\overline{\text{HOLD}}$	XRDY	$\overline{\text{XRDY}}$
HOLDA	$\overline{\text{HOLDA}}$	(X)RDY	$\overline{\text{(X)RDY}}$, includes $\overline{\text{RDY}}$ and $\overline{\text{XRDY}}$
IACK	$\overline{\text{IACK}}$	XRW	XR/$\overline{\text{W}}$
INT	$\overline{\text{INT3}}$ – $\overline{\text{INT0}}$	(X)RW	(X)R/$\overline{\text{W}}$, includes R/$\overline{\text{W}}$ and XR/$\overline{\text{W}}$

X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals. The numbers shown in Figure 7 and Figure 8 correspond with those in the NO. column of the table below. Refer to the RESET timing in Figure 19 for CLKIN to H1 and H3 delay specification.

timing parameters for X2/CLKIN, H1, H3 (see Figure 7 and Figure 8)

NO.			'C30-27		'C30-33		'C30-40		'C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		6†		5†		5†		5†	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low $t_{c(CI)}$ = min	14		10		9		7		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high $t_{c(CI)}$ = min	14		10		9		7		ns
4	$t_{r(CI)}$	Rise time, CLKIN		6†		5†		5†		5†	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	37	303	30	303	25	303	20	303	ns
6	$t_{f(H)}$	Fall time, H1 and H3		4		3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1 and H3 low	P–6‡		P–6‡		P–5‡		P–5‡		ns
8	$t_{w(HH)}$	Pulse duration, H1 and H3 high	P–7‡		P–7‡		P–6‡		P–6‡		ns
9	$t_{r(H)}$	Rise time, H1 and H3		5		4		3		3	ns
9.1	$t_{d(HL-HH)}$	Delay time, from H1 low to H3 high or from H3 low to H1 high	0	6	0	5	0	4	0	4	ns
10	$t_{c(H)}$	Cycle time, H1 and H3	74	606	60	606	50	606	40	606	ns

† Specified by design but not tested
‡ P = $t_{c(CI)}$

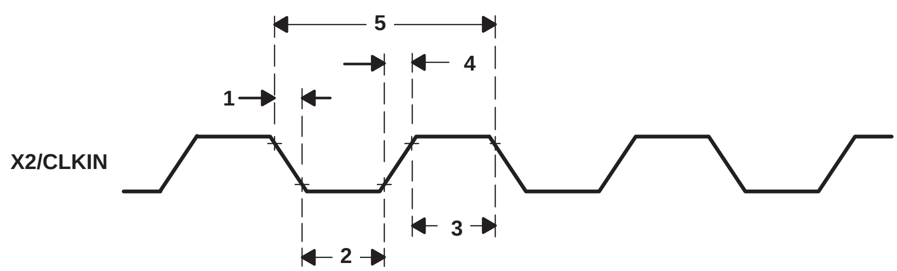


Figure 7. Timing for X2/CLKIN

X2/CLKIN, H1, and H3 timing (continued)

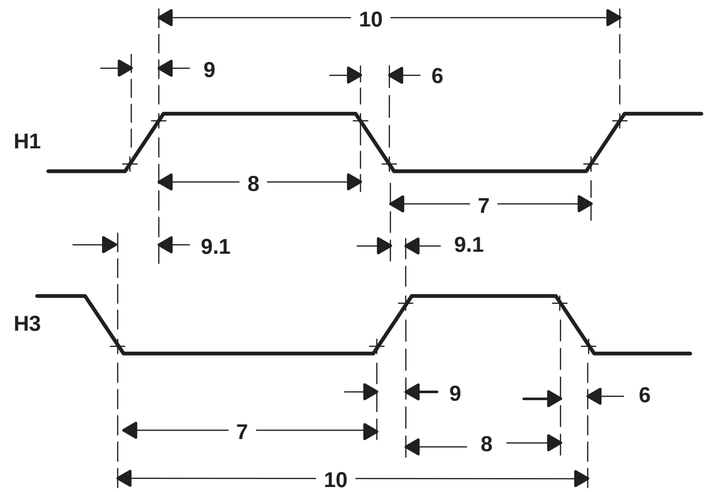


Figure 8. Timing for H1 and H3

memory read/write timing

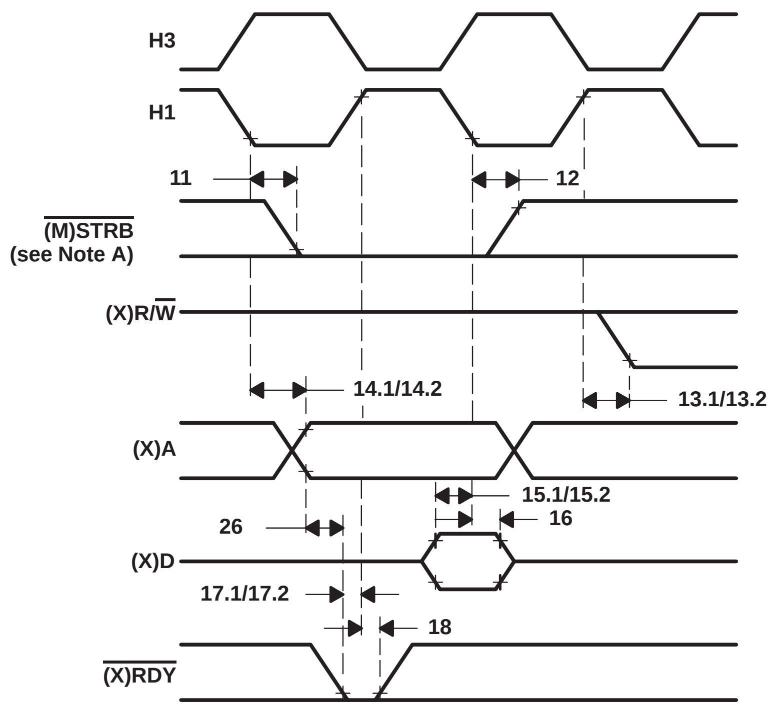
The following table defines memory read/write timing parameters for $\overline{\text{(M)STRB}}$. The numbers shown in Figure 9 and Figure 10 correspond with those in the NO. column of the table.

timing parameters for a memory [$\overline{\text{(M)STRB}}$ = 0] read/write (see Figure 9 and Figure 10)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
11	$t_{d[H1L-(M)SL]}$	Delay time, H1 low to $\overline{\text{(M)STRB}}$ low	0†	13	0†	10	0†	6‡	0†	4	ns
12	$t_{d[H1L-(M)SH]}$	Delay time, H1 low to $\overline{\text{(M)STRB}}$ high	0†	13	0†	10	0†	6	0†	4	ns
13.1	$t_{d(H1H-RWL)}$	Delay time, H1 high to R/$\overline{\text{W}}$ low	0†	13	0†	10	0†	9	0†	7	ns
13.2	$t_{d(H1H-XRWL)}$	Delay time, H1 high to XR/$\overline{\text{W}}$ low	0†	19	0†	15	0†	13	0†	11	ns
14.1	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0†	16	0†	14	0†	11	0†	9	ns
14.2	$t_{d(H1L-XA)}$	Delay time, H1 low to XA valid	0†	12	0†	10	0†	9	0†	8	ns
15.1	$t_{su(D-H1L)R}$	Setup time, D before H1 low (read)	18		16		14		10		ns
15.2	$t_{su(XD-H1L)R}$	Setup time, XD before H1 low (read)	21		18		16		14		ns
16	$t_{h[H1L-(X)D]R}$	Hold time, (X)D after H1 low (read)	0		0		0		0		ns
17.1	$t_{su(RDY-H1H)}$	Setup time, $\overline{\text{RDY}}$ before H1 high	10		8		8		6		ns
17.2	$t_{su(XRDY-H1H)}$	Setup time, $\overline{\text{XRDY}}$ before H1 high	11		9		9		8		ns
18	$t_{h[H1H-(X)RDY]}$	Hold time, $\overline{\text{(X)RDY}}$ after H1 high	0		0		0		0		ns
19	$t_{d[H1H-(X)RWH]W}$	Delay time, H1 high to (X)R/$\overline{\text{W}}$ high (write)		13		10		9		7	ns
20	$t_{v[H1L-(X)D]W}$	Valid time, (X)D after H1 low (write)		25		20		17		14	ns
21	$t_{h[H1H-(X)D]W}$	Hold time, (X)D after H1 high (write)	0†		0†		0†		0†		ns
22.1	$t_{d(H1H-A)W}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		23		18		15		12	ns
22.2	$t_{d(H1H-XA)W}$	Delay time, H1 high to XA valid on back-to-back write cycles (write)		32		25		21		18	ns
26	$t_{d[A-(X)RDY]}$	Delay time, $\overline{\text{(X)RDY}}$ from A valid		10§		8§		7§		6	ns

† Specified by design but not tested
‡ For ’C30 PPM, $t_{d[H1L-(M)SL]}$ (max)=7 ns
§ This value is characterized but not tested

memory read/write timing (continued)



NOTE A: (M)STRB remains low during back-to-back read operations.

Figure 9. Timing for Memory [(M)STRB = 0] Read

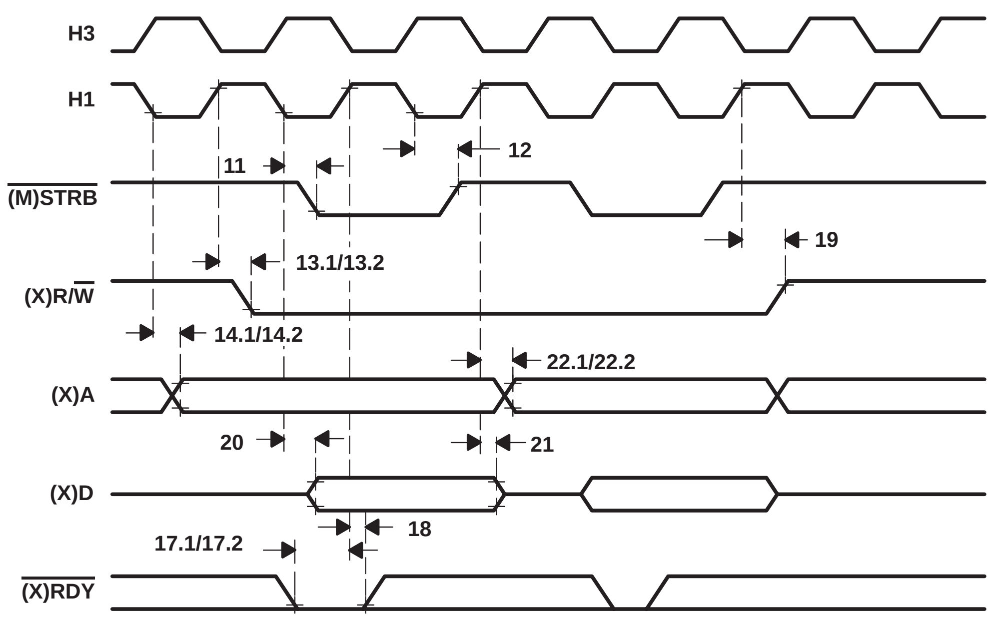


Figure 10. Timing for Memory [(M)STRB = 0] Write

memory read/write timing (continued)

The following table defines memory read timing parameters for $\overline{\text{IOSTRB}}$. The numbers shown in Figure 11 correspond with those in the NO. column of the table below.

timing parameters for a memory ($\overline{\text{IOSTRB}}$ = 0) read (see Figure 11)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
11.1	$t_{d(H1H-IOSL)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ low	0†	13	0†	10	0†	9	0†	8	ns
12.1	$t_{d(H1H-IOSH)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ high	0†	13	0†	10	0†	9	0†	8	ns
13.1	$t_{d(H1L-XRWH)}$	Delay time, H1 low to XR/$\overline{\text{W}}$ high	0†	13	0†	10	0†	9	0	8	ns
14.3	$t_{d(H1L-XA)}$	Delay time, H1 low to XA valid	0†	13	0†	10	0†	9	0†	8	ns
15.3	$t_{su(XD-H1H)R}$	Setup time, XD before H1 high (read)	19		15		13		11		ns
16.1	$t_{hH1H-XD)R}$	Hold time, XD after H1 high (read)	0		0		0		0		ns
17.3	$t_{su(XRDY-H1H)}$	Setup time, $\overline{\text{XRDY}}$ before H1 high	11		9		9		8		ns
18.1	$t_{h(H1H-XRDY)}$	Hold time, $\overline{\text{XRDY}}$ after H1 high	0		0		0		0		ns
23	$t_{d(H1L-XRWL)}$	Delay time, H1 low to XR/$\overline{\text{W}}$ low	0†	19	0†	15	0†	13	0†	11	ns

† This value is characterized but not tested

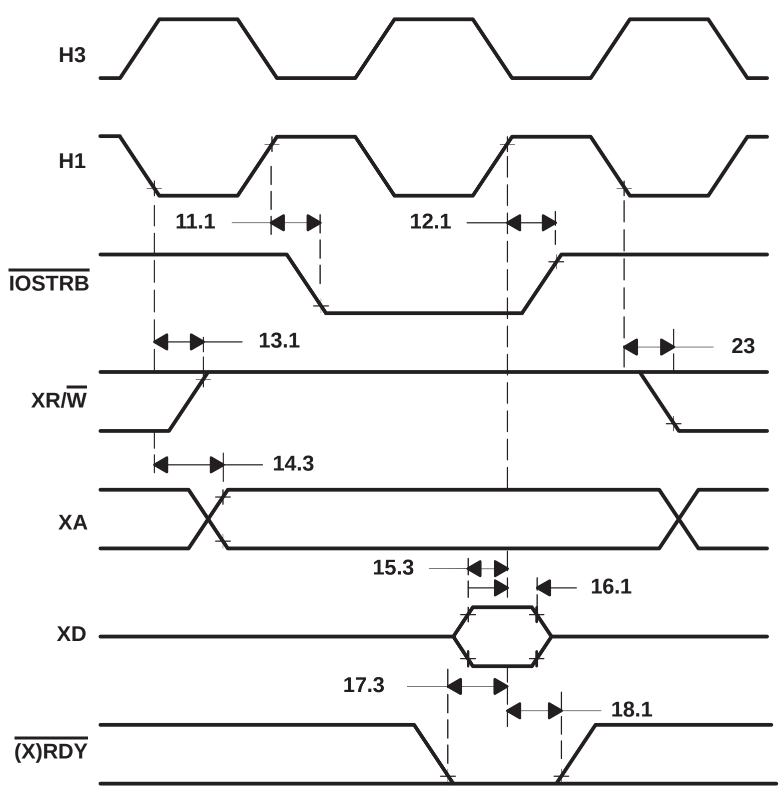


Figure 11. Timing for Memory ($\overline{\text{IOSTRB}}$ = 0) Read

memory read/write timing (continued)

The following table defines memory write timing parameters for $\overline{IOSTRB}$. The numbers shown in Figure 12 correspond with those in the NO. column of the table below.

timing parameters for a memory ($\overline{IOSTRB}$ = 0) write (see Figure 12)

NO.			'C30-27		'C30-33		'C30-40		'C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
11.1	$t_{d(H1H-IOSL)}$	Delay time, H1 high to $\overline{IOSTRB}$ low	0†	13	0†	10	0†	9	0†	8	ns
12.1	$t_{d(H1H-IOSH)}$	Delay time, H1 high to $\overline{IOSTRB}$ high	0†	13	0†	10	0†	9	0†	8	ns
13.1	$t_{d(H1L-XRWH)}$	Delay time, H1 low to XR/$\overline{W}$ high	0†	13	0†	10	0†	9	0	8	ns
14.3	$t_{d(H1L-XA)}$	Delay time, H1 low to XA valid	0†	13	0†	10	0†	9	0†	8	ns
17.3	$t_{su(XRDY-H1H)}$	Setup time, $\overline{XRDY}$ before H1 high	11		9		9		8		ns
18.1	$t_{h(H1H-XRDY)}$	Hold time, $\overline{XRDY}$ after H1 high	0		0		0		0		ns
23	$t_{d(H1L-XRWL)}$	Delay time, H1 low to XR/$\overline{W}$ low	0†	19	0†	15	0†	13	0†	11	ns
24	$t_{v(H1H-XD)W}$	Valid time, (X)D after H1 high (write)		38		30		25		20	ns
25	$t_{h(H1L-XD)W}$	Hold time, (X)D after H1 low (write)	0		0		0		0		ns

† This value is characterized but not tested

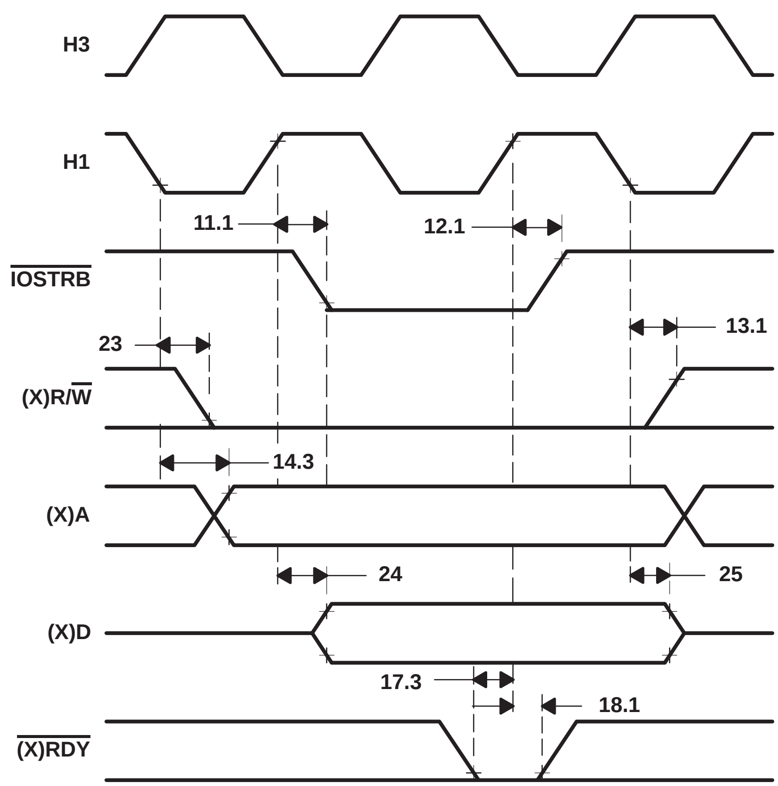


Figure 12. Timing for Memory ($\overline{IOSTRB}$ = 0) Write

XF0 and XF1 timing when executing LDFI or LDII

The following table defines the timing parameters for XF0 and XF1 during execution of LDFI or LDII. The numbers shown in Figure 13 correspond with those in the NO. column of the table below.

timing parameters for XF0 and XF1 when executing LDFI or LDII (see Figure 13)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		19		15		13		12	ns
2	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	13		10		9		9		ns
3	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		ns

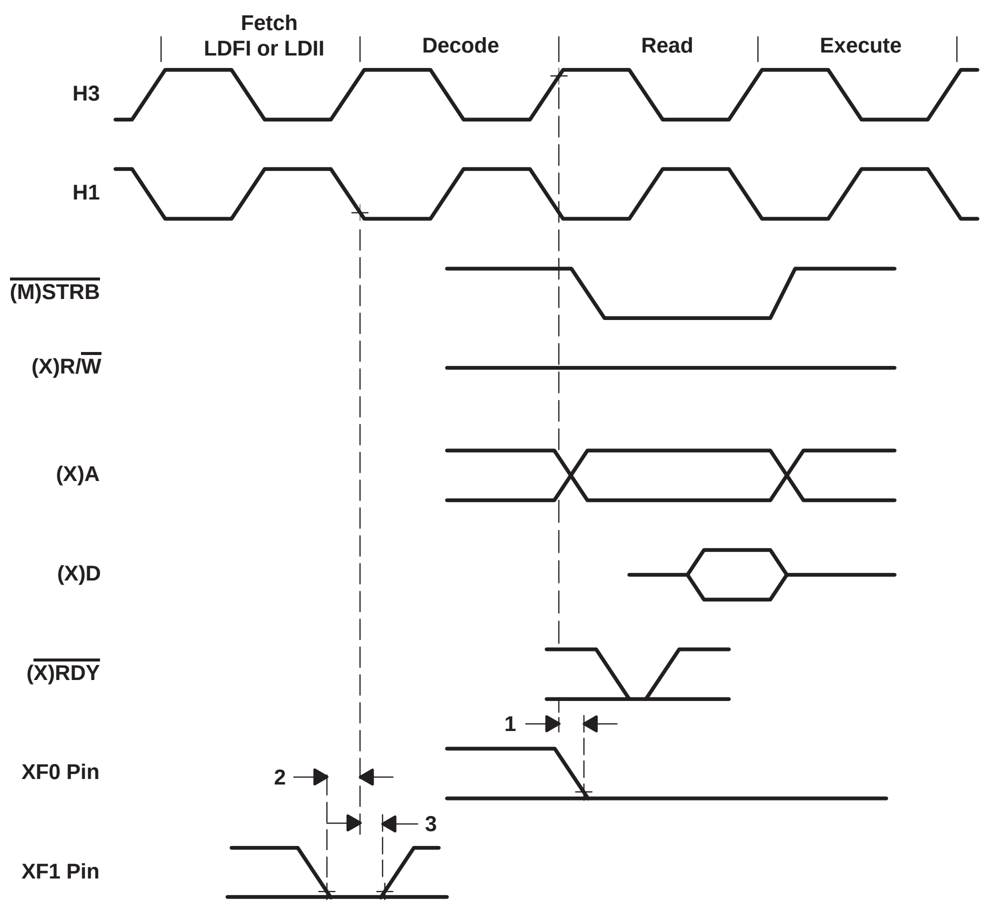


Figure 13. Timing for XF0 and XF1 When Executing LDFI or LDII

XF0 timing when executing STFI and STII

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII. The number shown in Figure 14 corresponds with the number in the NO. column of the table below.

timing parameters for XF0 when executing STFI or STII (see Figure 14)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		19		15		13		12	ns

XF0 is always set high at the beginning of the execute phase of the interlock store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

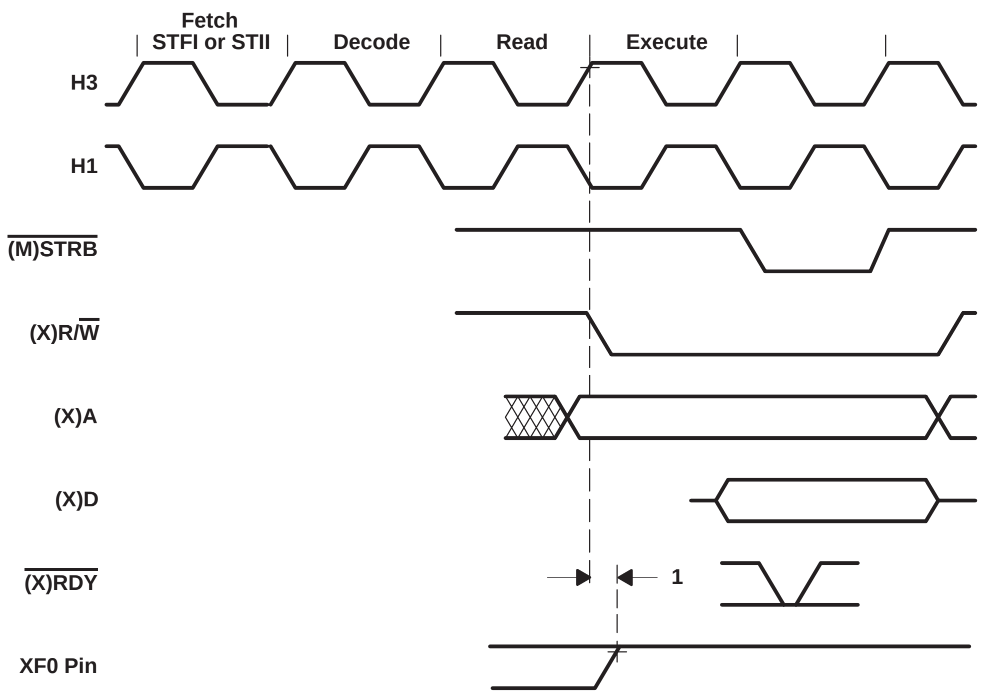


Figure 14. Timing for XF0 When Executing an STFI or STII

XF0 and XF1 timing when executing SIGI

The following table defines the timing parameters for the XF0 and XF1 pins during execution of SIGI. The numbers shown in Figure 15 correspond with those in the NO. column of the table below.

timing parameters for XF0 and XF1 when executing SIGI (see Figure 15)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		19		15		13		12	ns
2	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		19		15		13		12	ns
3	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	13		10		9		9		ns
4	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		ns

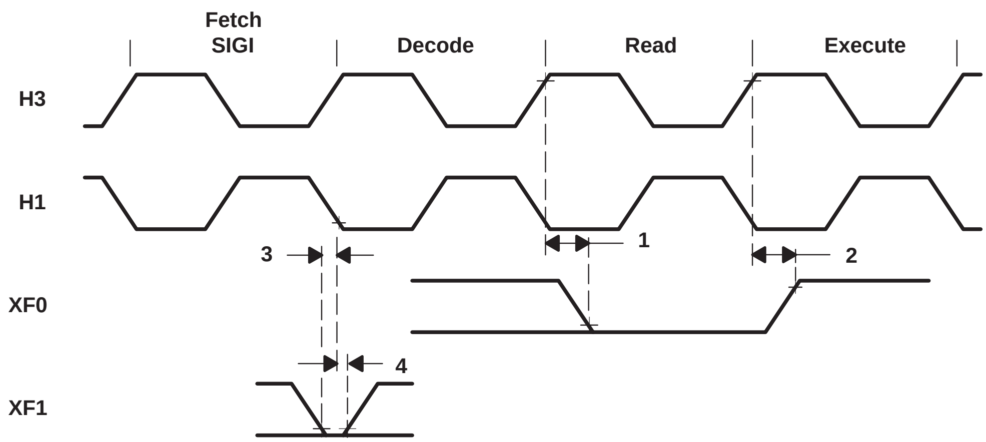


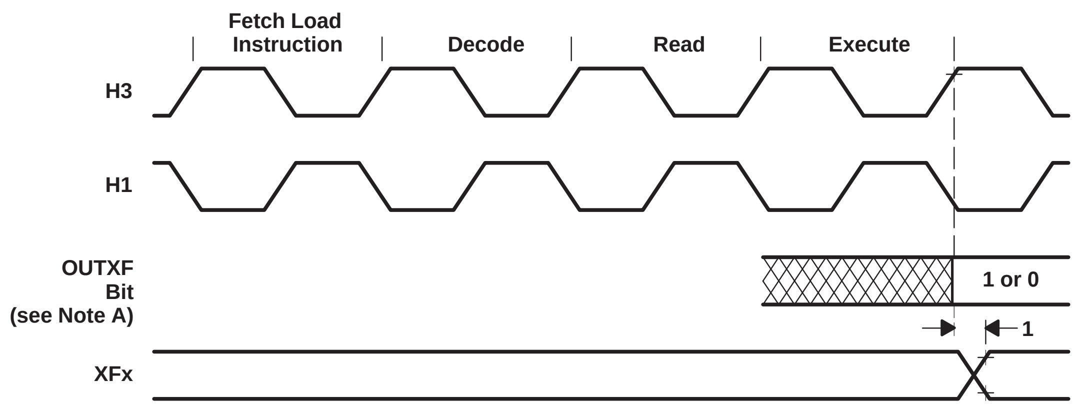
Figure 15. Timing for XF0 and XF1 When Executing SIGI

loading when XFx is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output. The number shown in Figure 16 corresponds with the number in the NO. column of the table below.

timing parameters for loading the XFx register when configured as an output pin (see Figure 16)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{v(H3H\text{-}XF)}$	Valid time, H3 high to XFx		19		15		13		12	ns



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 16. Timing for Loading XFx Register When Configured as an Output Pin

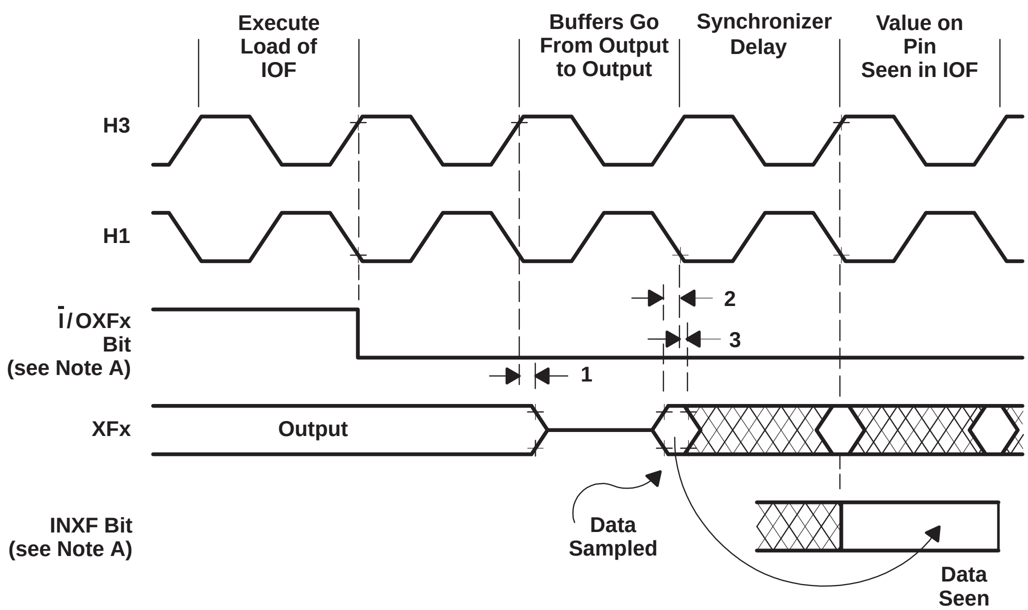
changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin. The numbers shown in Figure 17 correspond with those in the NO. column of the table below.

timing parameters of XFx changing from output to input mode (see Figure 17)

NO.			'C30-27		'C30-33		'C30-40		'C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{h(H3H-XF)}$	Hold time, XFx after H3 high		19‡		15‡		13†‡		12‡	ns
2	$t_{su(XF-H1L)}$	Setup time, XFx before H1 low	13		10		9		9		ns
3	$t_{h(H1L-XF)}$	Hold time, XFx after H1 low	0		0		0		0		ns

† For 'C30 PPM, $t_{n(H3H-XF01)}$ (max)=14 ns
‡ This value is characterized but not tested



NOTE A: I/OXFx represents bit 1 or 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

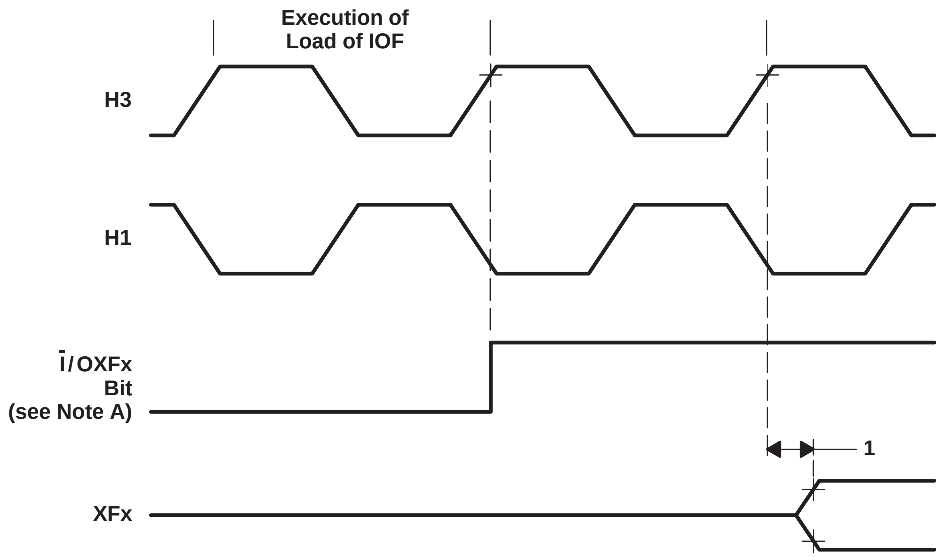
Figure 17. Timing for Change of XFx From Output to Input Mode

changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin. The number shown in Figure 18 corresponds with the number in the NO. column of the table below.

timing parameters of XFx changing from input to output mode (see Figure 18)

NO.			'C30-27		'C30-33		'C30-40		'C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XFx switching from input to output		25		20		17		17	ns



NOTE A: I/OXFx represents either bit 1 or 5 of the IOF register.

Figure 18. Timing for Change of XFx From Input to Output Mode

reset timing

$\overline{\text{RESET}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 19 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0/1, DX0/1, FSX0/1, CLKR0/1, DR0/1, FSR0/1, and TCLK0/1.

The following table defines the timing parameters for the $\overline{\text{RESET}}$ signal. The numbers shown in Figure 19 correspond with those in the NO. column of the following table.

Resetting the device initializes the primary- and expansion-bus control registers to seven software wait states and therefore results in slow external accesses until these registers are initialized.

Note also that $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted during reset.

timing parameters for $\overline{\text{RESET}}$ for the TMS320C30 (see Figure 19)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(RESET-CIL)}$	Setup time, $\overline{\text{RESET}}$ before CLKIN low	28	P†‡	10	P†‡	10	P†‡	10	P†‡	ns
2.1	$t_{d(CIH-H1H)}$	Delay time, CLKIN high to H1 high§¶	2	20	2	14	2	12	2	10	ns
2.2	$t_{d(CIH-H1L)}$	Delay time, CLKIN high to H1 low§¶	2	20	2	14	2	12	2	10	ns
3	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	13		10		9		7		ns
5.1	$t_{d(CIH-H3L)}$	Delay time, CLKIN high to H3 low§¶	2	20	2	14	2	12	2	10	ns
5.2	$t_{d(CIH-H3H)}$	Delay time, CLKIN high to H3 high§¶	2	20	2	14	2	12	2	10	ns
8	$t_{dis[H1H-(X)D]}$	Disable time, H1 high to (X)D (high impedance)		19†		15†		13†		12†	ns
9	$t_{dis[H3H-(X)A]}$	Disable time, H3 high to (X)A (high impedance)		13†		10†		9†		8†	ns
10	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		13†		10†		9†		8†	ns
12	$t_{d(H1H-RWH)}$	Delay time, H1 high to R/$\overline{\text{W}}$ high		13†		10†		9†		8†	ns
13	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		13†		10†		9†		8†	ns
14	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals (high impedance)		31†		25†		21†		17†	ns

† This value is characterized but not tested
‡ P = $t_{c(CI)}$
§ See Figure 20 for temperature dependence for the 33-MHz and the 40-MHz TMS320C30.
¶ See Figure 21 for temperature dependence for the 50-MHz TMS320C30.

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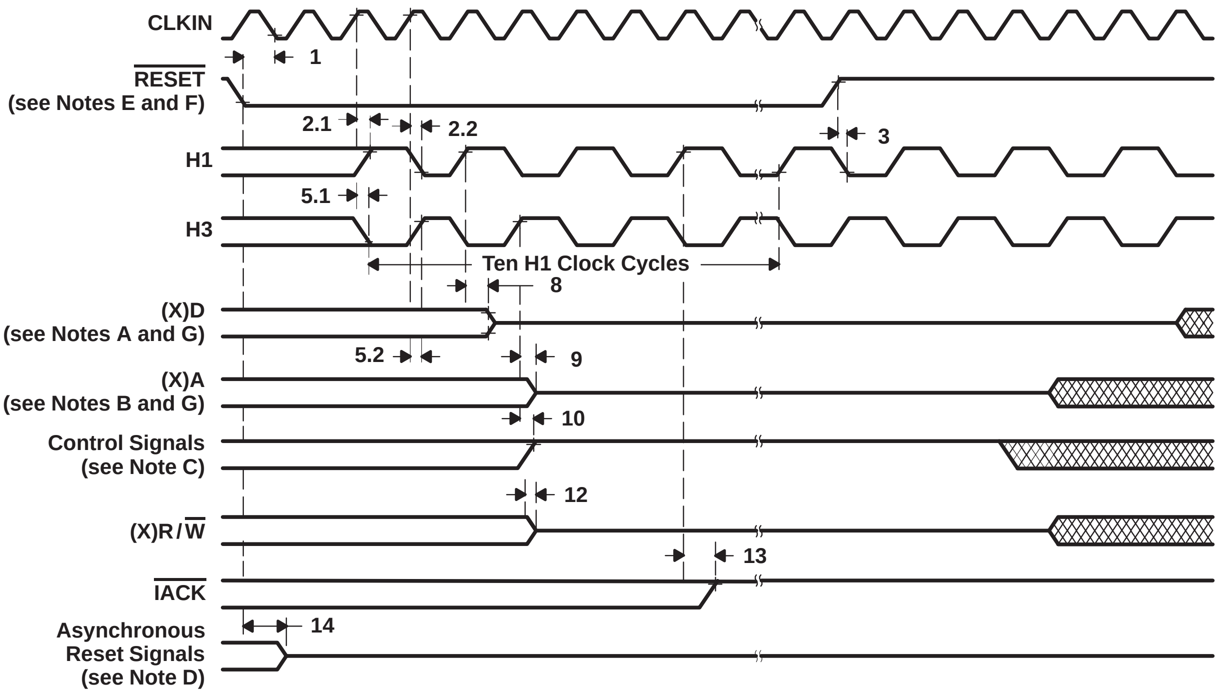
reset timing (continued)



NOTES: A. (X)D includes D31–D0 and XD31–XD0.
B. (X)A includes A23–A0 and XA12–XA0.
C. Interface signals include STRB, MSTRB, and IOSTRB.
D. Asynchronous reset signals include XF0/1, CLKX0/1, DX0/1, FSX0/1, CLKR0/1, DR0/1, FSR0/1, and TCLK0/1.
E. RESET is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
F. The R/W and XR/W outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18–22 kΩ, if undesirable spurious writes could be caused when these outputs go low.
G. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.

Figure 19. Timing for RESET

reset timing (continued)

Figure 20 and Figure 21 illustrate CLKIN-to-H1 and CLKIN-to-H3 timing as a function of case temperature.

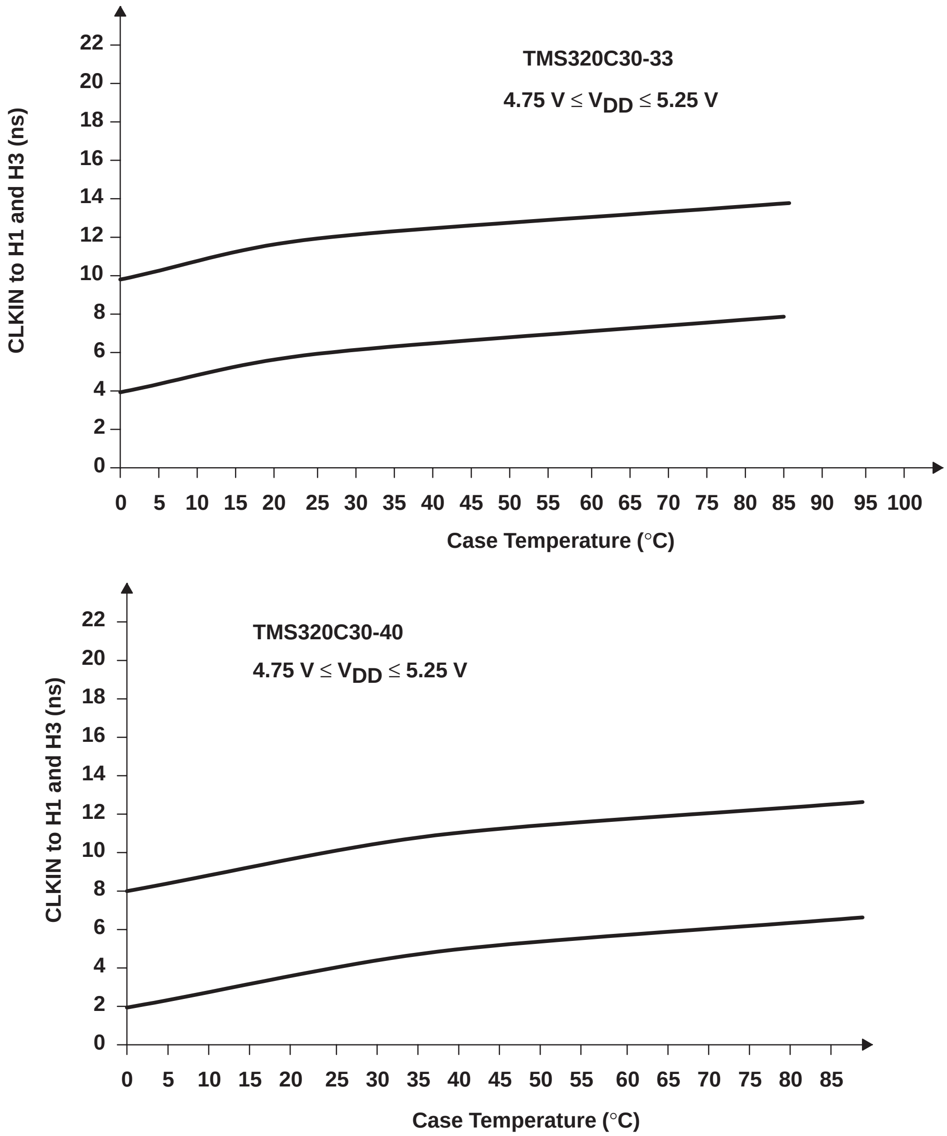


Figure 20. CLKIN to H1 and H3 as a Function of Temperature

reset timing (continued)

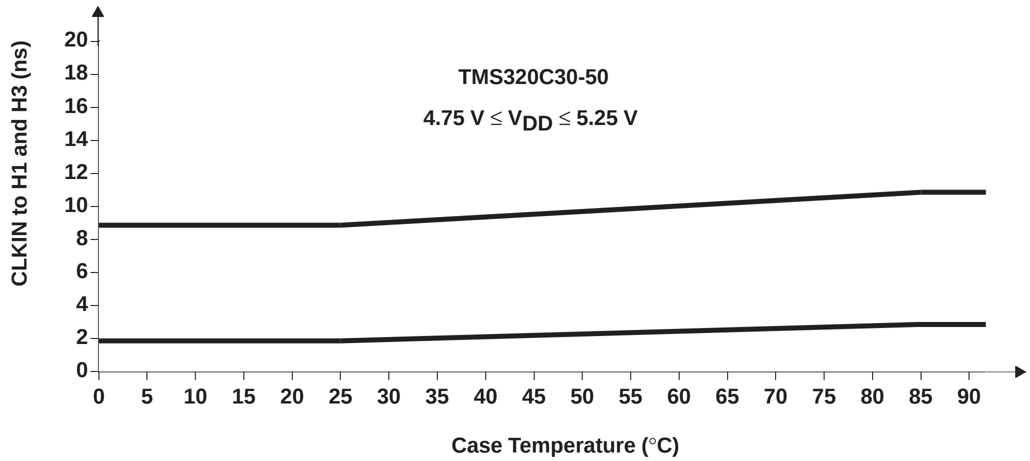


Figure 21. CLKIN to H1 and H3 as a Function of Temperature

interrupt response timing

The following table defines the timing parameters for the $\overline{\text{INT}}$ signals. The numbers shown in Figure 22 correspond with those in the NO. column of the table below.

timing parameters for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ (see Figure 22)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(INT-H1L)}$	Setup time, $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ before H1 low	19		15		13		10		ns
2	$t_{w(INT)}$	Pulse duration, interrupt to ensure only one interrupt	P	2P†‡	P	2P†‡	P	2P†‡	P	2P†‡	ns

† Characterized but not tested
‡ P = $t_{c(H)}$

The interrupt ($\overline{\text{INT}}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The TMS320C30 interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The TMS320C30 can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 22 occurs; otherwise, an additional delay of one clock cycle is possible.

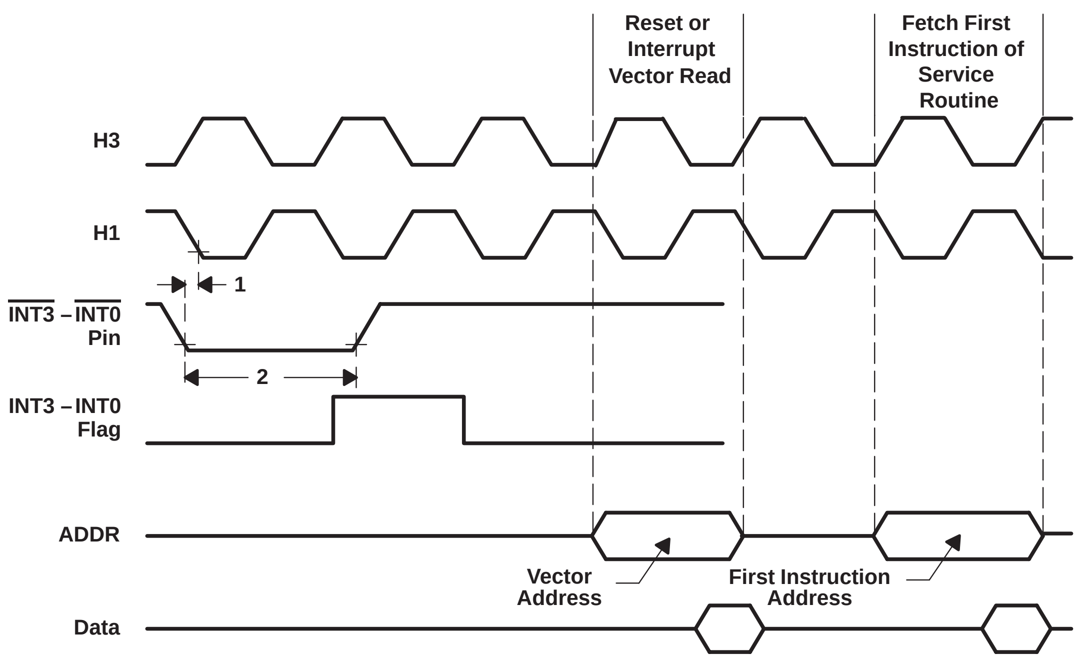


Figure 22. Timing for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ Response

interrupt-acknowledge timing

The IACK output goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction.

The following table defines the timing parameters for the IACK signal. The numbers shown in Figure 23 correspond with those in the NO. column of the table below.

timing parameters for IACK (see Note 6 and Figure 23)

NO.			’C30-27 MIN	’C30-27 MAX	’C30-33 MIN	’C30-33 MAX	’C30-40 MIN	’C30-40 MAX	’C30-50 MIN	’C30-50 MAX	UNIT
1	$t_{d(H1H-IACKL)}$	Delay time, H1 high to IACK low		13		10		9		7	ns
2	$t_{d(H1H-IACKH)}$	Delay time, H1 high to IACK high		13		10		9		7	ns

NOTE 6: IACK goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of the pipeline conflicts, IACK remains low for one cycle even if the decode phase of the IACK instruction is extended.

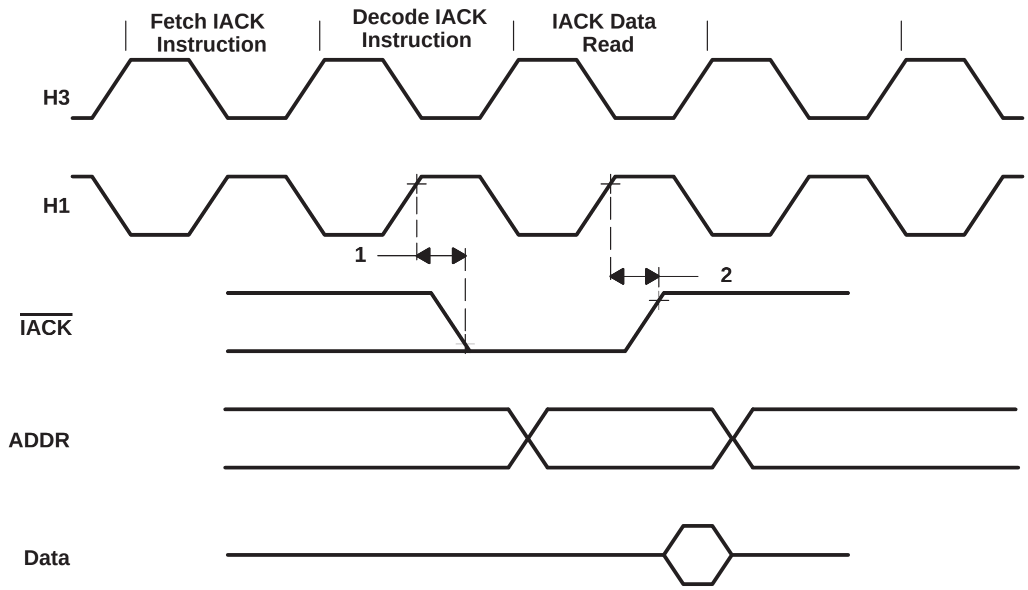


Figure 23. Timing for IACK

serial-port timing parameters (see Figure 24 and Figure 25)

NO.				'320C30-27 MIN	'320C30-27 MAX	UNIT
1	$t_{d(H1H\text{-}SCK)}$	Delay time, H1 high to internal CLKX/R			19	ns
2	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
3	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+12		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–15	[$t_{c(SCK)}$/2]+5	
4	$t_{r(SCK)}$	Rise time, CLKX/R			10	ns
5	$t_{f(SCK)}$	Fall time, CLKX/R			10	ns
6	$t_{d(CH\text{-}DX)}$	Delay time, CLKX to DX valid	CLKX ext		44	ns
			CLKX int		25	
7	$t_{su(DR\text{-}CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	13		ns
			CLKR int	31		
8	$t_{h(CLKRL\text{-}DR)}$	Hold time, DR from CLKR low	CLKR ext	13		ns
			CLKR int	0		
9	$t_{d(CH\text{-}FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		40	ns
			CLKX int		21	
10	$t_{su(FSR\text{-}CLKRL)}$	Setup time, FSR0 or FSR1 before CLKR low	CLKR ext	13		ns
			CLKR int	13		
11	$t_{h(SCKL\text{-}FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	13		ns
			CLKX/R int	0		
12	$t_{su(FSX\text{-}CH)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	–[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
13	$t_{d(CH\text{-}DX)V}$	Delay time, CLKX to first DX bit, FSX0 or FSX1 precedes CLKX high	CLKX ext		45†	ns
			CLKX int		26†	
14	$t_{d(FSX\text{-}DX)V}$	Delay time, FSX0 or FSX1 to first DX bit, CLKX precedes FSX0 or FSX1			45†	ns
15	$t_{d(CHH\text{-}DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			25†	ns

† This value is characterized but not tested

serial-port timing parameters (see Figure 24 and Figure 25) (continued)

NO.				’320C30-33 MIN	’320C30-33 MAX	UNIT
1	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			15	ns
2	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
3	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+12		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–15	[$t_{c(SCK)}$/2]+5	
4	$t_{r(SCK)}$	Rise time, CLKX/R			8	ns
5	$t_{f(SCK)}$	Fall time, CLKX/R			8	ns
6	$t_{d(CH-DX)}$	Delay time, CLKX to DX valid	CLKX ext		35	ns
			CLKX int		20	
7	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	10		ns
			CLKR int	25		
8	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	10		ns
			CLKR int	0		
9	$t_{d(CH-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		32	ns
			CLKX int		17	
10	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	10		ns
			CLKR int	10		
11	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	10		ns
			CLKX/R int	0		
12	$t_{su(FSX-CH)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
13	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		36†	ns
			CLKX int		21†	
14	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			36†	ns
15	$t_{d(CHH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			20†	ns

† This value is characterized but not tested

serial-port timing parameters (see Figure 24 and Figure 25) (continued)

NO.				’320C30-40 MIN	’320C30-40 MAX	UNIT
1	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			13	ns
2	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
3	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	[$t_{c(SCK)}$/2]–5	[$t_{c(SCK)}$/2]+5	
4	$t_{r(SCK)}$	Rise time, CLKX/R			7	ns
5	$t_{f(SCK)}$	Fall time, CLKX/R			7	ns
6	$t_{d(CH-DX)}$	Delay time, CLKX to DX valid	CLKX ext		30	ns
			CLKX int		17	
7	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	21		
8	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	9		ns
			CLKR int	0		
9	$t_{d(CH-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		27	ns
			CLKX int		15	
10	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	9		ns
			CLKR int	9		
11	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	9		ns
			CLKX/R int	0		
12	$t_{su(FSX-CH)}$	Setup time, external FSX before CLKX	CLKX ext	–[$t_{c(H)}$–8]†	[$t_{c(SCK)}$/2]–10†	ns
			CLKX int	[$t_{c(H)}$–21]†	$t_{c(SCK)}$/2†	
13	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext CLKX int		30† 18†	ns
14	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			30†	ns
15	$t_{d(CHH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			17†	ns

† This value is characterized but not tested

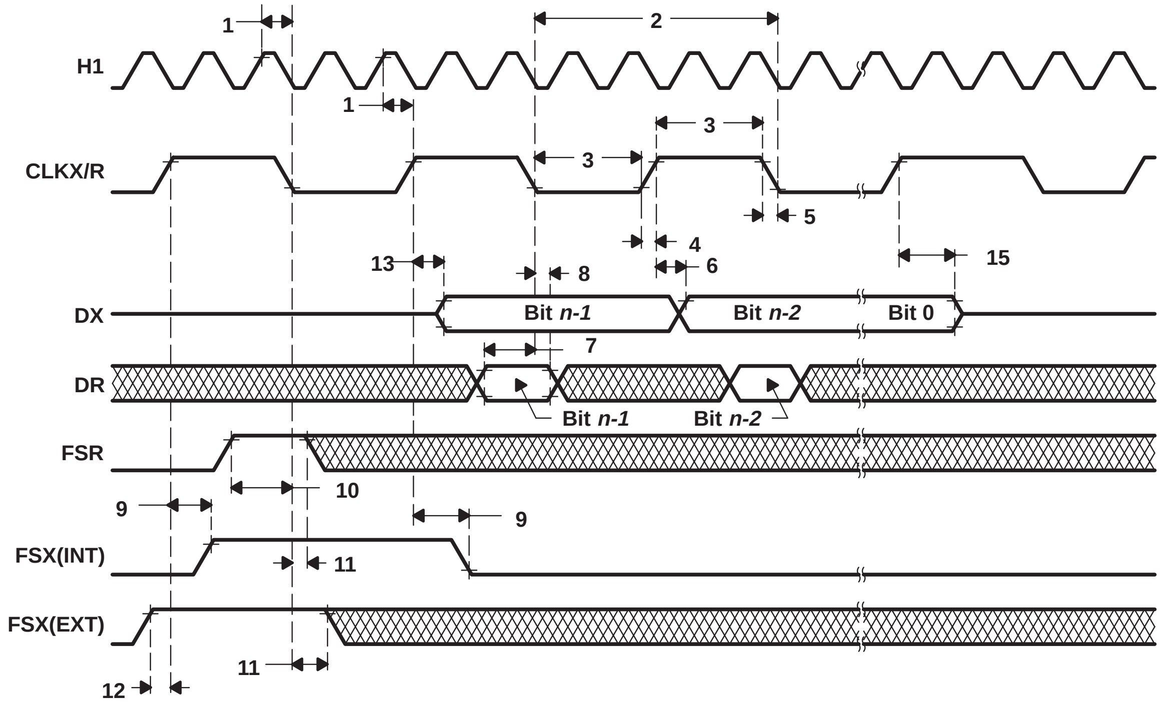
serial-port timing parameters (see Figure 24 and Figure 25) (continued)

NO.				’320C30-50 MIN	’320C30-50 MAX	UNIT
1	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			10	ns
2	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext CLKX/R int	$t_{c(H)} \times 2.6$ $t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$	ns
3	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}+10$		ns
			CLKX/R int	$[t_{c(SCK)}/2]–5$	$[t_{c(SCK)}/2]+5$	
4	$t_{r(SCK)}$	Rise time, CLKX/R			6	ns
5	$t_{f(SCK)}$	Fall time, CLKX/R			6	ns
6	$t_{d(CH-DX)}$	Delay time, CLKX to DX valid	CLKX ext		24	ns
			CLKX int		16	
7	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	17		
8	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	7		ns
			CLKR int	0		
9	$t_{d(CH-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		22	ns
			CLKX int		15	
10	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	7		ns
			CLKR int	7		
11	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	7		ns
			CLKX/R int	0		
12	$t_{su(FSX-CH)}$	Setup time, external FSX before CLKX	CLKX ext	$–[t_{c(H)}–8]^{\dagger}$	$[t_{c(SCK)}/2]–10^{\dagger}$	ns
			CLKX int	$[t_{c(H)}–21]^{\dagger}$	$t_{c(SCK)}/2^{\dagger}$	
13	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		$24^{\dagger}$	ns
			CLKX int		$14^{\dagger}$	
14	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			$24^{\dagger}$	ns
15	$t_{d(CHH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			$14^{\dagger}$	ns

† This value is characterized but not tested

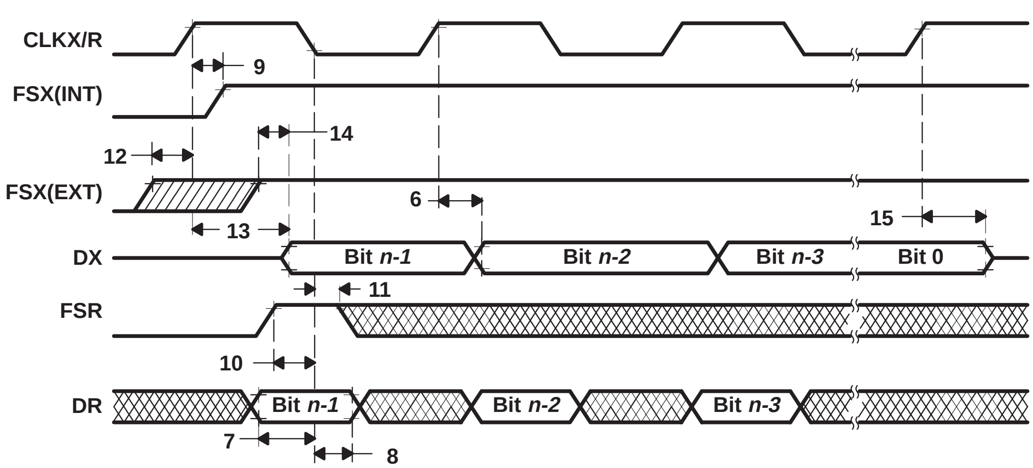
data-rate timing modes

Unless otherwise indicated, the data-rate timings shown in Figure 24 and Figure 25 are valid for all serial-port modes, including handshake. See serial-port timing parameter tables.



NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial port word, where *n* = 8, 16, 24, or 32 bits, respectively.

Figure 24. Timing for Fixed Data-Rate Mode



NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where *n* = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 25. Timing for Variable Data-Rate Mode

$\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 26 occurs; otherwise, an additional delay of one clock cycle is possible.

The “timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$” table defines the timing parameters for the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. The numbers shown in Figure 26 correspond with those in the NO. column of the table.

The NOHOLD bit of the primary bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue until a second write is encountered.

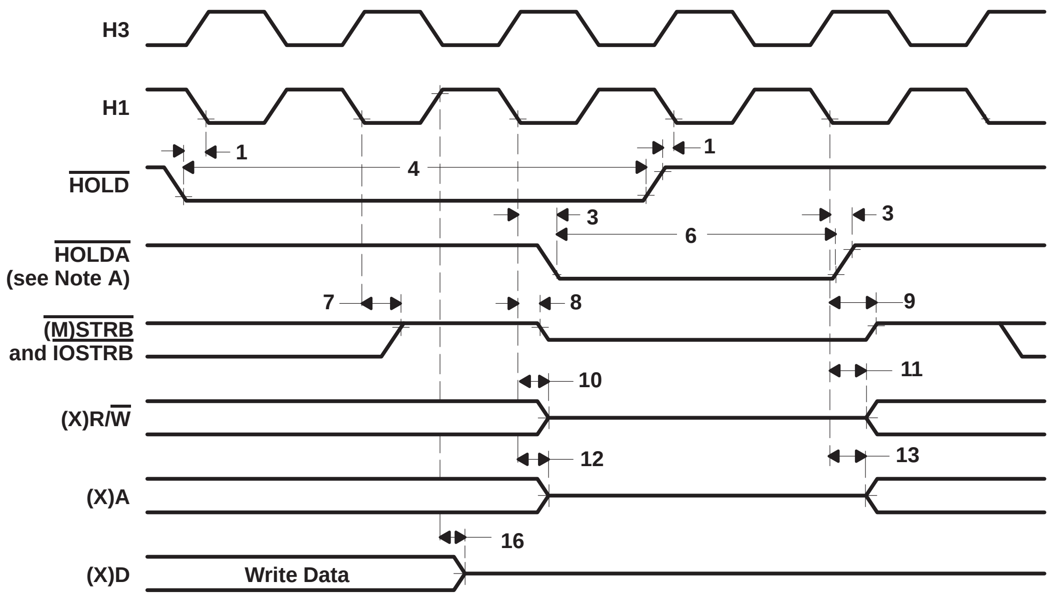
HOLD timing (continued)

timing parameters for HOLD/HOLDA (see Figure 26)

NO.			'C30-27 MIN	'C30-27 MAX	'C30-33 MIN	'C30-33 MAX	'C30-40 MIN	'C30-40 MAX	'C30-50 MIN	'C30-50 MAX	UNIT
1	$t_{su(HOLD-H1L)}$	Setup time, HOLD before H1 low	19		15		13		10		ns
3	$t_{v(H1L-HOLDA)}$	Valid time, HOLDA after H1 low	0†	14	0†	10	0†	9	0†	7	ns
4	$t_{w(HOLD‡)}$	Pulse duration, HOLD low	$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		ns
6	$t_{w(HOLDA)}$	Pulse duration, HOLDA low	$t_{c(H)}$–5†		$t_{c(H)}$–5†		$t_{c(H)}$–5†		$t_{c(H)}$–5†		ns
7	$t_{d(H1L-SH)HOLD}$	Delay time, H1 low to (M)S and IOS high for a HOLD	0§	13	0§	10	0§	9	0§	7	ns
8	$t_{dis(H1L-S)Z}$	Disable time, H1 low to (M)S and IOS in the high-impedance state	0§	13†	0§	10†	0§	9†	0§	8†	ns
9	$t_{en(H1L-S)}$	Enable time, H1 low to (M)S and IOS (active)	0§	13	0§	10	0§	9	0§	7	ns
10	$t_{dis[H1L-(X)RW]Z}$	Disable time, H1 low to (X)R/W in the high-impedance state	0†	13†	0†	10†	0†	9†	0†	8†	ns
11	$t_{en[H1L-(X)RW]}$	Enable time, H1 low to (X)R/W (active)	0†	13	0†	10	0†	9	0†	7	ns
12	$t_{dis[H1L-(X)A]}$	Disable time, H1 low to (X)A in the high-impedance state	0§	13†	0§	10†	0§	10†	0§	8†	ns
13	$t_{en[H1L-(X)A]}$	Enable time, H1 low to (X)A (valid)	0§	19	0§	15	0§	13	0§	12	ns
16	$t_{dis[H1H-(X)D]Z}$	Disable time, H1 high to (X)D in the high-impedance state	0§	13†	0§	10†	0§	9†	0§	8†	ns

† This value is characterized but not tested
‡ HOLD is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
§ Not tested

HOLD timing (continued)



NOTE A: HOLDA goes low in response to HOLD going low and continues to remain low until one H1 cycle after HOLD goes back high.

Figure 26. Timing for HOLD/HOLDA

general-purpose I/O timing

Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The contents of the internal-control registers associated with each peripheral define the modes for these pins.

peripheral pin I/O timing

The following table defines peripheral pin general-purpose I/O timing parameters. The numbers shown in Figure 27 correspond with those in the NO. column of the table below.

timing parameters for peripheral pin general-purpose I/O (see Note 7 and Figure 27)

NO.			'C30-27		'C30-33		'C30-40		'C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{su(GPIO-H1L)}$	Setup time, general-purpose input before H1 low	15		12		10		9		ns
2	$t_{h(H1L-GPIO)}$	Hold time, general-purpose input after H1 low	0		0		0		0		ns
3	$t_{d(H1H-GPIO)}$	Delay time, general-purpose output after H1 high		19		15		13		10	ns

NOTE 7: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

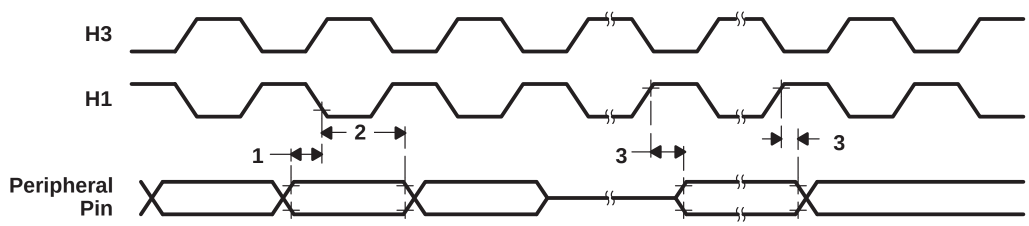


Figure 27. Timing for Peripheral Pin General-Purpose I/O

changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and the reverse. The numbers shown in Figure 28 and Figure 29 correspond to those shown in the NO. column of the following tables.

timing parameters for peripheral pin changing from general-purpose output to input mode (see Note 7 and Figure 28)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{h(H1H-GPIO)}$	Hold time, peripheral pin after H1 high		19		15		13		10	ns
2	$t_{su(GPIO-H1L)}$	Setup time, peripheral pin before H1 low	13		10		9		9		ns
3	$t_{h(H1L-GPIO)}$	Hold time, peripheral pin after H1 low	0		0		0		0		ns

NOTE 7: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

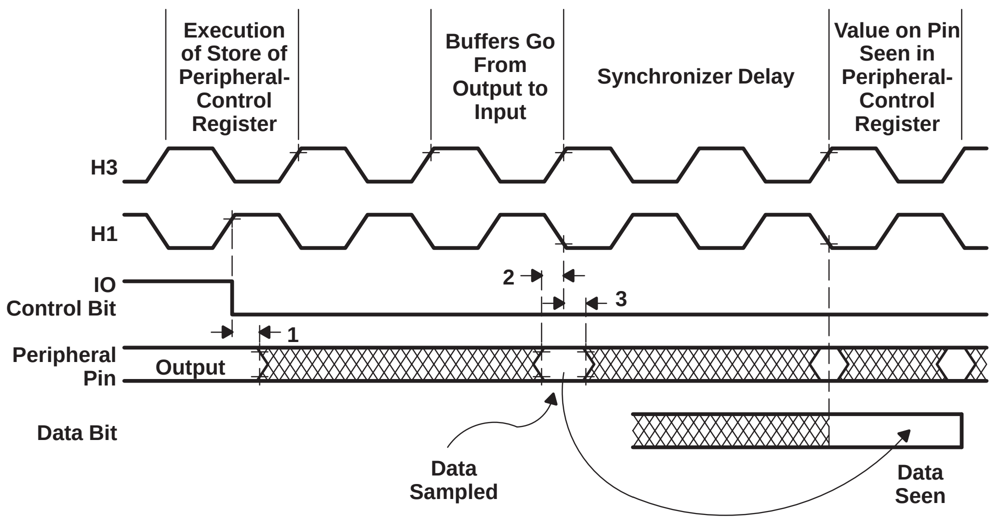


Figure 28. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

timing parameters for peripheral pin changing from general-purpose input to output mode (see Note 7 and Figure 29)

NO.			’C30-27		’C30-33		’C30-40		’C30-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{d(H1H-GPIO)}$	Delay time, H1 high to peripheral pin switching from input to output		19		15		13		10	ns

NOTE 7: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.

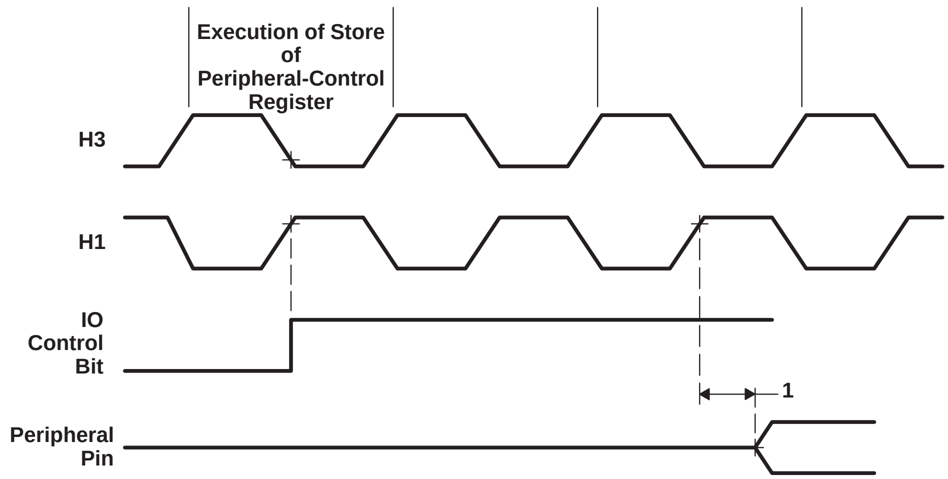


Figure 29. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

timer pin (TCLK0 and TCLK1) timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers.

The following tables define the timing parameters for the timer pin. The numbers shown in Figure 30 correspond with those in the NO. column of the tables below.

timing parameters for timer pin (TCLK0 and TCLK1) (see Figure 30)†

NO.				'C30-27†		'C30-33†		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{su(TCLK-H1L)}$	Setup time, TCLK ext before H1 low	TCLK ext	15		12		ns
2	$t_{h(H1L-TCLK)}$	Hold time, TCLK ext after H1 low	TCLK ext	0		0		ns
3	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK int valid	TCLK int		13		10	ns
4	$t_{c(TCLK)}$	Cycle time, TCLK	TCLK ext	$t_{c(H)}\times 2.6$		$t_{c(H)}\times 2.6$		ns
			TCLK int	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	
5	$t_{w(TCLK)}$	Pulse duration, TCLK high/low	TCLK ext	$t_{c(H)}+12$		$t_{c(H)}+12$		ns
			TCLK int	$[t_{c(TCLK)}/2]-15$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-15$	$[t_{c(TCLK)}/2]+5$	

NO.				'C30-40†		'C30-50†		UNIT
				MIN	MAX	MIN	MAX	
1	$t_{su(TCLK-H1L)}$	Setup time, TCLK ext before H1 low	TCLK ext	10		8		ns
2	$t_{h(H1L-TCLK)}$	Hold time, TCLK ext after H1 low	TCLK ext	0		0		ns
3	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK int valid	TCLK int		9		9	ns
4	$t_{c(TCLK)}$	Cycle time, TCLK	TCLK ext	$t_{c(H)}\times 2.6$		$t_{c(H)}\times 2.6$		ns
			TCLK int	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$‡	
5	$t_{w(TCLK)}$	Pulse duration, TCLK high/low	TCLK ext	$t_{c(H)}+10$		$t_{c(H)}+10$		ns
			TCLK int	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

† Timing parameters 1 and 2 are applicable for a synchronous input clock. Timing parameters 4 and 5 are applicable for an asynchronous input clock.
‡ Assured by design but not tested

timer pin (TCLK0 and TCLK1) timing (continued)

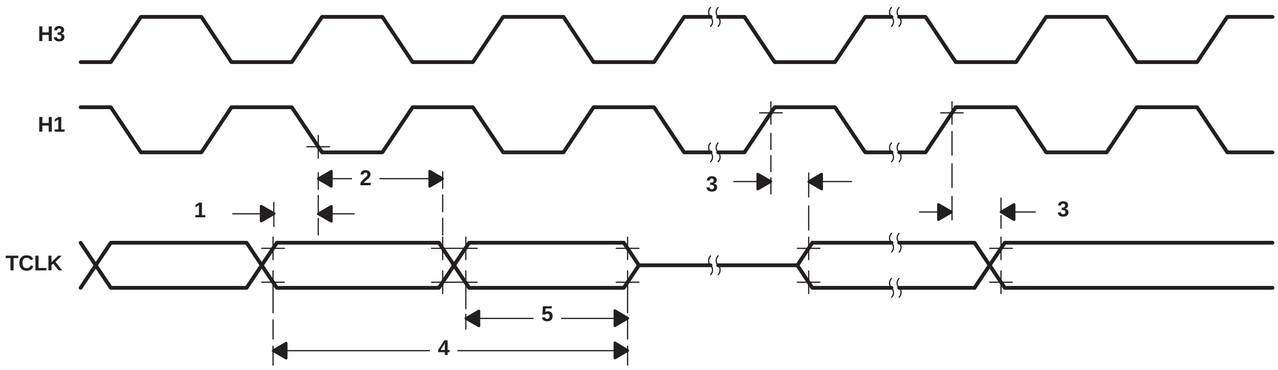


Figure 30. Timing for Timer Pin

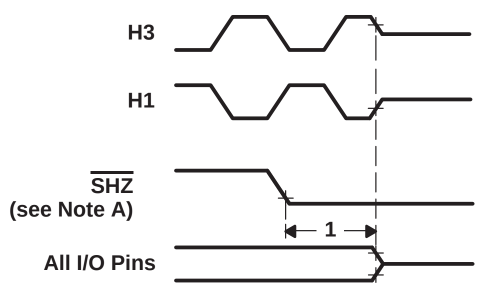
$\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin. The number shown in Figure 31 corresponds with that in the NO. column of the table below.

timing parameters for $\overline{\text{SHZ}}$ pin (see Figure 31)

NO.			'C30 MIN	'C30 MAX	UNIT
1	$t_{dis(SHZ)}$	Disable time, $\overline{\text{SHZ}}$ low to all outputs, I/O pins disabled (high impedance)	0†	2P†‡	ns

† Characterized but not tested
‡ $P = t_{c(CI)}$

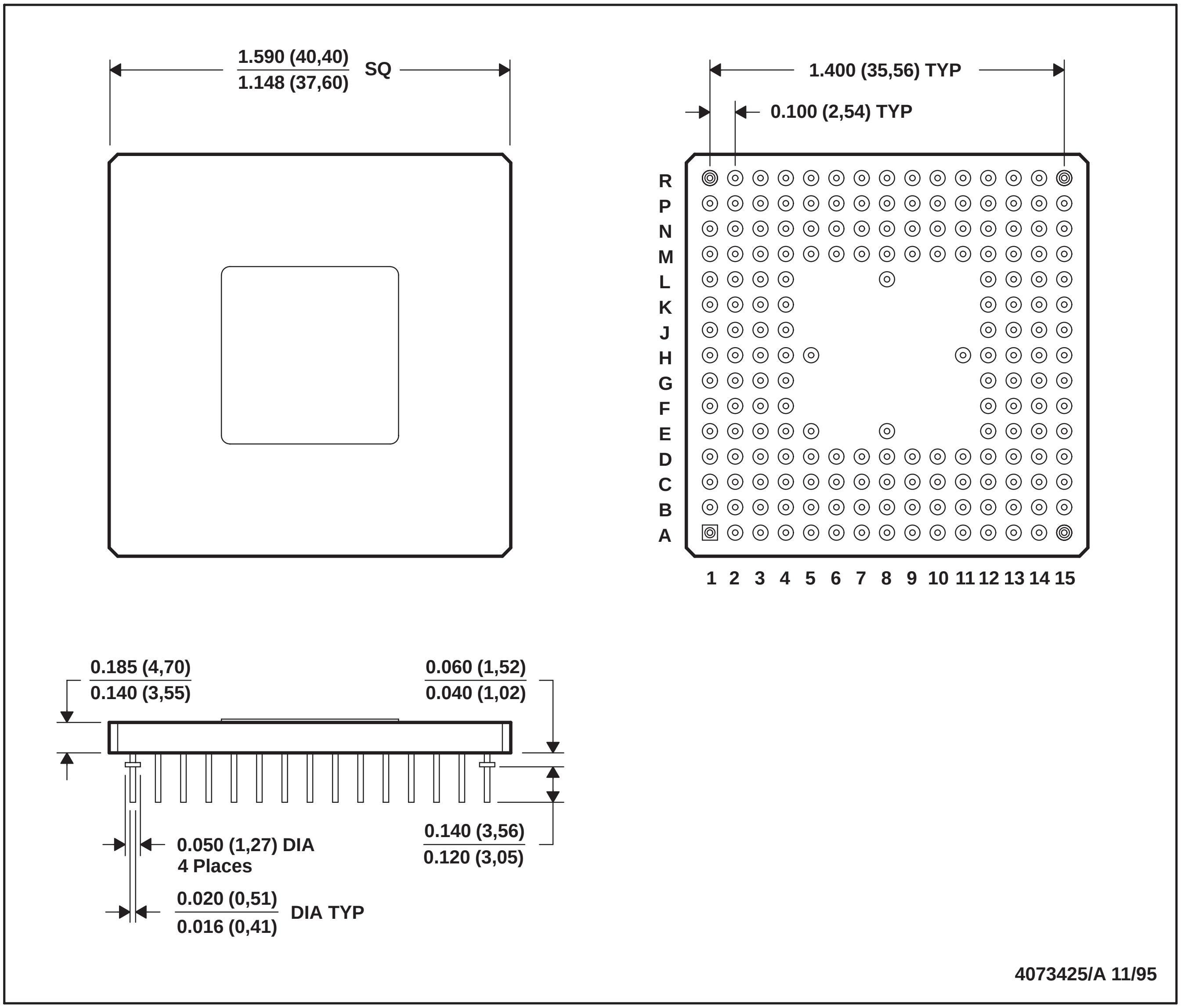


NOTE A: Enabling $\overline{\text{SHZ}}$ destroys TMS320C30 register and memory contents. Assert $\overline{\text{SHZ}}$ = 1 and reset the TMS320C30 to restore it to a known condition.

Figure 31. Timing for $\overline{\text{SHZ}}$

MECHANICAL DATA

GE (S-CPGA-P181) CERAMIC PIN GRID ARRAY PACKAGE



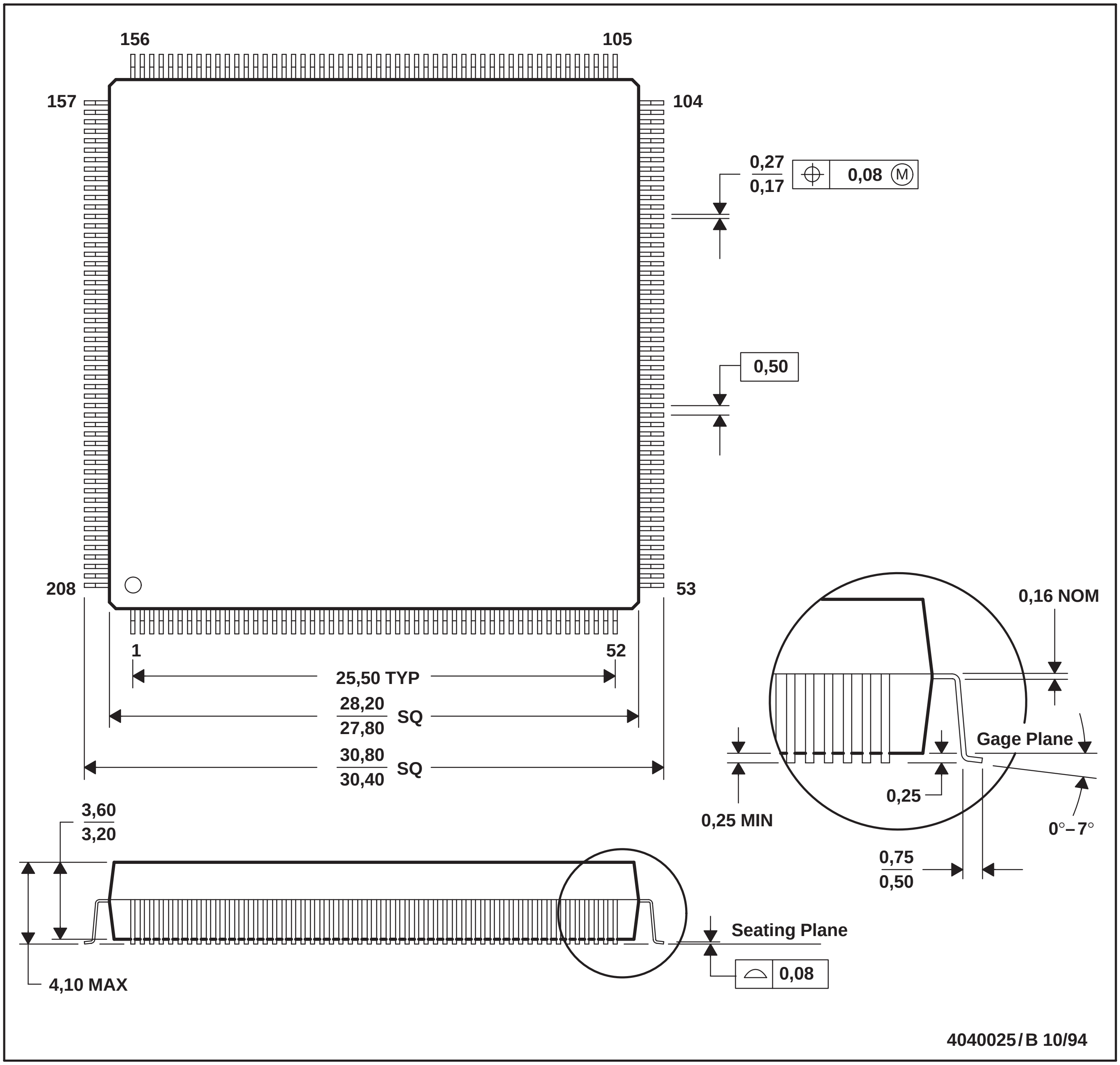
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Table 1. Thermal Resistance Characteristics for TMS320C30 GEL (PGA Package)

PARAMETER		MAX	UNIT
$R_{\Theta JA}$	Junction-to-free air	21.8	°C/W
$R_{\Theta JC}$	Junction-to-case	2.0	°C/W

MECHANICAL DATA

PPM (S-PQFP-G208) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-143

Table 2. Thermal Resistance Characteristics for TMS320C30 PPM (PQFP Package)

PARAMETER		MAX	UNIT
$R_{\Theta JA}$	Junction-to-free air	35.2	°C/W
$R_{\Theta JC}$	Junction-to-case	8.5	°C/W

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMS320C30GEL	NRND	CPGA	GE	181	21	TBD	AU	N / A for Pkg Type
TMS320C30GEL27	OBSOLETE	CPGA	GB	181		TBD	Call TI	Call TI
TMS320C30GEL40	NRND	CPGA	GE	181	21	TBD	AU	N / A for Pkg Type
TMS320C30GEL50	NRND	CPGA	GE	181	21	TBD	AU	N / A for Pkg Type
TMS320C30PPM40	OBSOLETE	QFP	PP	208		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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