SENSYLINK Microelectronics

(CA9306)
Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

The CA9306 device is a dual bidirectional I²C and SMBus voltage-level translator with an enable input, and is operational from 1.2V to 3.3V V_{REF1} and 1.8V to 5.5V V_{REF2}.
It is ideally used in Servers, Routers, PC, Industrial Automation and two-signal interfaces (I²C, SMBus, PMBus, MDIO, UART, low-speed SDIO, GPIO).

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Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

1. Description

The CA9306 device is a dual bidirectional I^2C and SMBus voltage-level translator with an enable input, and is operational from 1.2V to 3.3V V_{REF1} and 1.8V to 5.5V V_{REF2}.

The CA9306 device allows bidirectional voltage translations between 1.2V and 5V without a direction pin. The low ON-state resistance (RON) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is OFF, and a high-impedance state exists between ports.

The CA9306 device can be used to isolate a 400kHz bus from a 100kHz bus by controlling the EN pin to disconnect the slower bus during fast-mode communication in addition to voltage translation.

Available Package: MSOP-8, DFN3x4-8, DFN2x3-8 package.

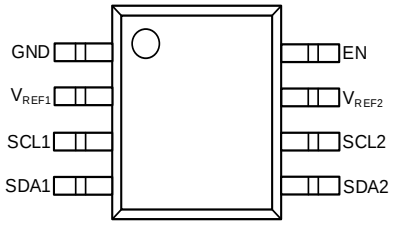
2. Features

- 2-Bit bidirectional translator for SDA and SCL in mixed-mode I^2C applications
- I^2C and SMBus compatible
- Less than 1.5ns maximum propagation delay to accommodate standard-mode and fast-mode I^2C devices and multiple masters
- Allows voltage-level translation between
  – 1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  – 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  – 2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  – 3.3V V_{REF1} and 5V V_{REF2}
- Provides bidirectional voltage translation with no direction pin
- Low 3.5Ω ON-state resistance between input and output ports provides less signal distortion
- 5V tolerant I^2C I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = Low
- Lockup-free operation for isolation when EN = Low
- Flow-through pin out for ease of printed-circuit-board trace routing

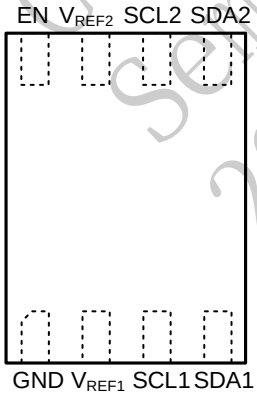
3. Applications

- I^2C, SMBus, PMBus, MDIO, UART, low-speed SDIO, GPIO, and other two-signal interfaces
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Industrial Automation Applications

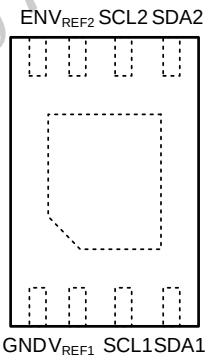
4. PIN Configurations



MSOP-8(Package Code MM)



DFN3x4-8(Package Code DN)



DFN2x3-8 (Package Code DNA)

5. Typical Application

The typical value of R_{PU} is 1kΩ

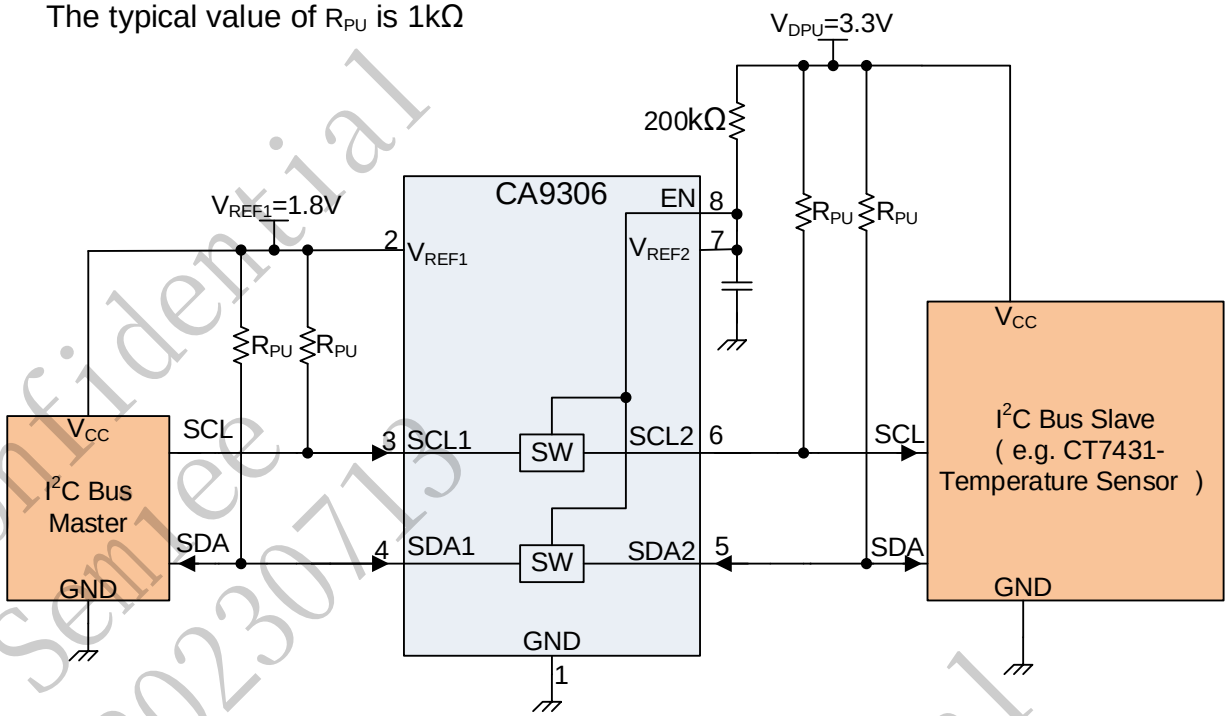


Figure 1 Typical Application Circuit (Switch Always Enable)

The typical value of R_{PU} is 1kΩ

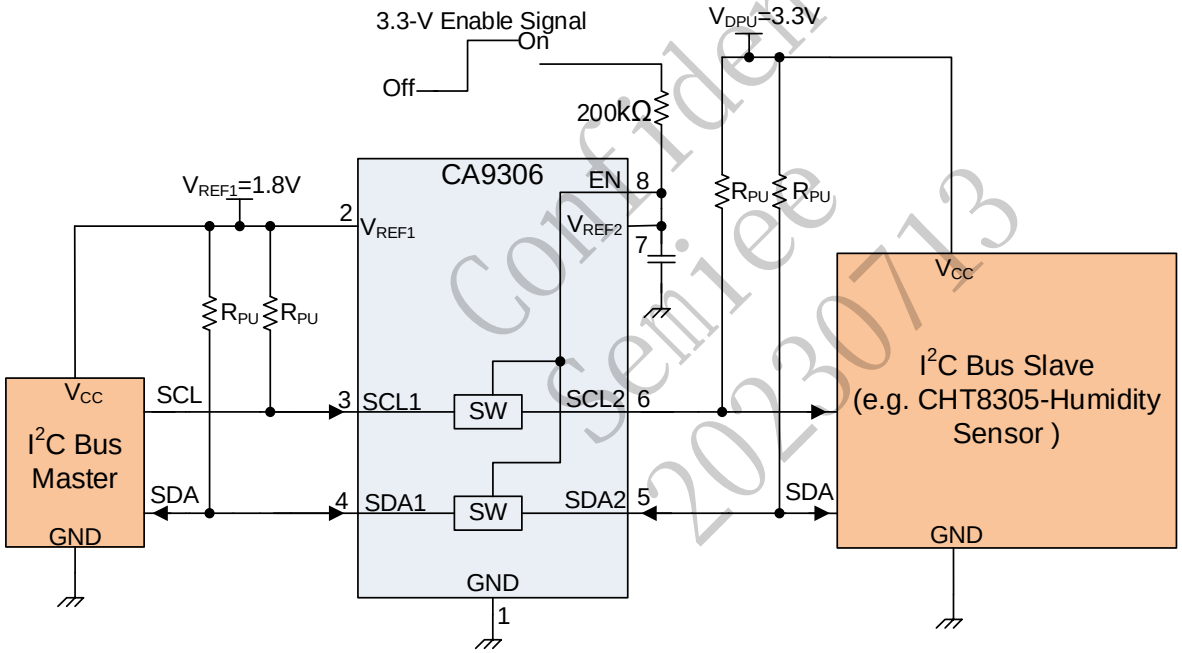


Figure 2 Typical Application Circuit (Switch Enable Control)

6. Pin Description

PIN Name	PIN No.	Description
GND	1	Supply ground
V_{REF1}	2	Low-voltage-side reference supply voltage for SCL1 and SDA1
SCL1	3	Serial clock, low-voltage side
SDA1	4	Serial data, low-voltage side
SDA2	5	Serial data, high-voltage side
SCL2	6	Serial clock, high-voltage side
V_{REF2}	7	High-voltage-side reference supply voltage for SCL2 and SDA2
EN	8	Switch enable input

7. Function Block

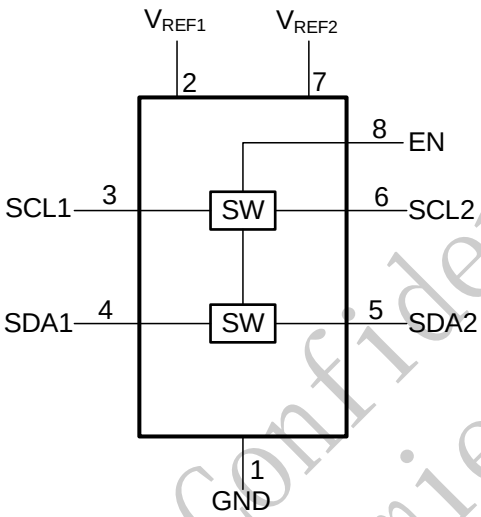
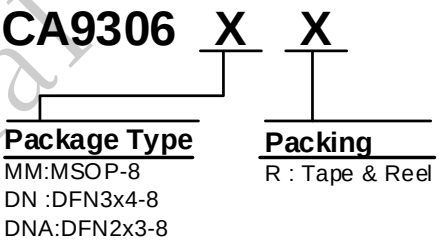


Figure 3 CA9306 Function Block

8. Ordering Information



Order PN	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
CA9306MMR	Halogen free	MSOP-8	9306 YWWAXX	Tape & Reel	3,000	-40°C~+85°C
CA9306DNR	Halogen free	DFN3x4-8	9306 YWWAXX	Tape & Reel	5,000	-40°C~+85°C
CA9306DNAR	Halogen free	DFN2x3-8	HF YWXA	Tape & Reel	3,000	-40°C~+85°C

Notes:
1. Sensylink can meet RoHS2.0/REACH requirement. Most package types Sensylink offers only states halogen free, instead of lead free.
2. Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

9. Specification

9.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
DC Reference Voltage Range	V_{REF1}	-0.5 to 7	V
DC Reference Bias Voltage Range	V_{REF2}	-0.5 to 7	V
Input Voltage Range	V_I	-0.5 to 7	V
Input/Output Voltage Range[2]	$V_{I/O}$	-0.5 to 7	V
Continuous Channel Current		128	mA
Input Clamp Current	I_{IK}	-50	mA
Maximum Junction Temperature	T_{jmax}	125	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
ESD HBM	ESD_{HBM}	±4000	V
ESD CDM	ESD_{CDM}	±1000	V

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

9.2 Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Input/output Voltage	$V_{I/O}$	0 to 5.5	V
Reference Voltage	V_{REF1}	0 to 5.5	V
Reference Voltage	V_{REF2}	0 to 5.5	V
Enable input Voltage	EN	0 to 5.5	V
Pass Switch Current	I_{PASS}	64	mA
Operating Ambient Temperature	T_A	-40 to 85	°C

9.3 Electrical Characteristics

Over recommended operating ambient temperature range (unless otherwise noted). All limits are 100% tested at T_A=25℃.

Parameter	Symbol	TEST CONDITIONS	MIN	Typ.	MAX	UNIT
Input Clamp Voltage	V_{IK}	I_I = –18 mA, EN = 0 V			-1.2	V
Input Leakage Current	I_{IH}	V_I = 5 V, EN = 0 V			5	uA
Input Capacitance	$C_{i(EN)}$	V_I = 3 V or 0		12		pF
Off Capacitance	$C_{io(off)}$	V_O = 3 V or 0, EN = 0 V		2.5	6	pF
On Capacitance	$C_{io(on)}$	V_O = 3 V or 0, EN = 3 V		2.5	12.5	pF
On-state Resistance	R_{ON}	V_I = 0, I_O = 64 mA, EN = 4.5 V		3.5	5.5	Ω
		V_I = 0, I_O = 64 mA, EN = 3 V		4.7	7	Ω
		V_I = 0, I_O = 64 mA, EN = 2.3 V		7	9.5	Ω
		V_I = 0, I_O = 15 mA, EN = 1.5 V		10	32	Ω
		V_I = 2.4 V, I_O = 15 mA, EN = 3 V	20	80	140	Ω
		V_I = 1.7 V, I_O = 15 mA, EN = 2.3 V	20	70	140	Ω

9.4 Interface Timing Requirements

9.4.1 Switching Characteristics AC Performance (Translating Down) (EN = 3.3V)[1]

Over recommended operating ambient temperature range, EN = 3.3V, V_{IH} = 3.3V, V_{IL} = 0, V_M = 1.15V (unless otherwise noted) (see Figure 15).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

Note:
1. Translating down: the high-voltage side driving toward the low-voltage side.

9.4.2 Switching Characteristics AC Performance (Translating Down) (EN = 2.5V)[1]

Over recommended operating ambient temperature range, EN = 2.5V, V_{IH} = 3.3V, V_{IL} = 0, V_M = 0.75V (unless otherwise noted) (see Figure 15)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

Note:
1. Translating down: the high-voltage side driving toward the low-voltage side.

9.4.3 Switching Characteristics AC Performance (Translating Up) (EN = 3.3V)[1]

Over recommended operating ambient temperature range, EN = 3.3V, V_{IH} = 2.3V, V_{IL} = 0, V_T = 3.3V, V_M = 1.15 V, R_L = 300 Ω (unless otherwise noted) (see Figure 15).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

Note:
1. Translating up: the low-voltage side driving toward the high-voltage side.

9.4.4 Switching Characteristics AC Performance (Translating Up) (EN = 2.5V)[1]

Over recommended operating ambient temperature range, EN = 2.5V, V_{IH} = 2.3V, V_{IL} = 0, V_T = 3.3V, V_M = 0.75 V, R_L = 300 Ω (unless otherwise noted) (see Figure 15).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

Note:
1. Translating up: the low-voltage side driving toward the high-voltage side.

9.5 Typical Characteristics

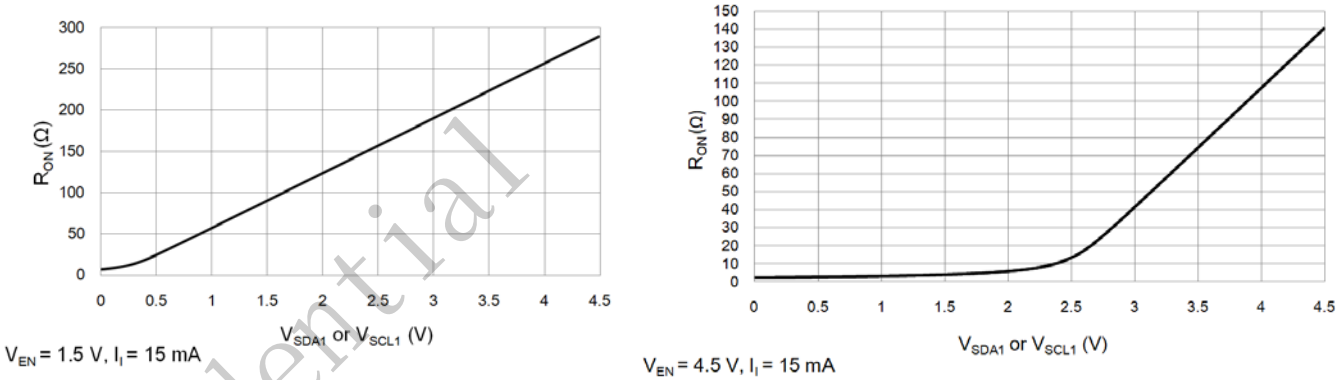


Figure 4 Typical Characteristics

10. Detailed Descriptions

10.1 Overview

The CA9306 device is a dual bidirectional I^2C and SMBus voltage-level translator with an enable (EN) input and operates without a direction pin. The V_{REF1} voltage supply ranges from 1.2V to 3.3V and the V_{REF2} voltage supply ranges from 1.8V to 5.5V.

The CA9306 device can also be used to run two buses. One bus is at 400kHz operating frequency and the other is at 100kHz. If the two buses are operating at different frequencies, the 100kHz bus must be disconnected by using the EN pin when the 400kHz operation of the main bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400kHz because the level shifter add the delays.

In I^2C applications, the bus capacitance limit of 400pF restricts the bus length and number of devices. The capacitive load on both sides of the CA9306 device must be taken into consideration when approximating the total load of the system, in order to ensure the sum of both sides is under 400pF.

Both the SDA and SCL channels have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because of the symmetrical fabrication of the switch. The translator provides excellent ESD protection to lower-voltage devices and protects less-ESD-resistant devices simultaneously.

10.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as V_{th}, which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2}. The value of V_{th} is approximately 0.6V at room temperature.

10.1.2 Correct Device Set Up

Figure 5 shows a normal set up. The enable (EN) pin and V_{REF2} are shorted together and tied to a 200kΩ resistor and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is required to help pass lows from one side to another side more effectively while still separating the different pull up voltages on both sides.

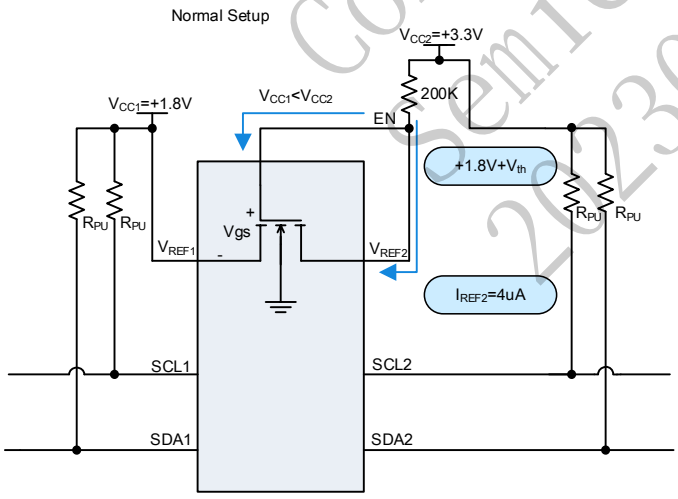


Figure 5 Normal Setup

An external resistor is required to be tied between V_{REF2} and V_{CC2}. Without the resistor, there is no external resistance from the V_{CC2} to V_{CC1} to limit the current such as in Figure 6. This effectively looks like a low impedance path for current to travel through and may break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 9.1. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2}.

Figure 6 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th}, the impedance between V_{CC1} and V_{CC2} is high, which does not cause damage to the device, but result in a low drain to source current. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th}. During this event, the NFET turns on and begin to conduct current, which is determined by the gate to source voltage and drain to source voltage.

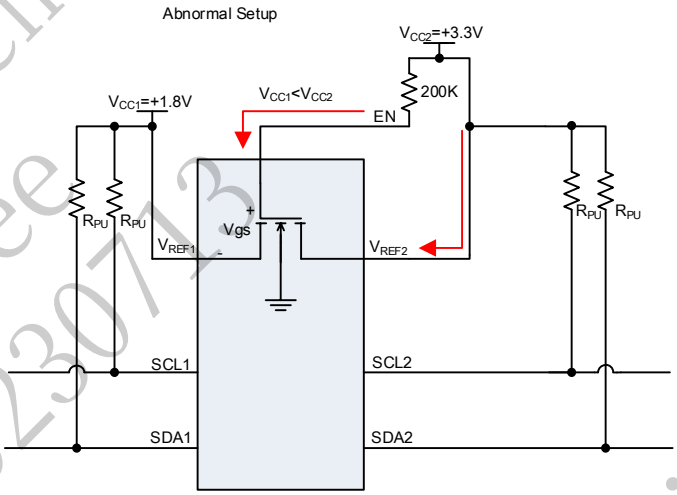


Figure 6 Abnormal Setup

10.1.3 Disconnecting a Slave from the Main I²C Bus Using the EN Pin

The CA9306 device can be used as a switch to disconnect one side of the device from the main I²C bus, which is advantageous in multiple situations. An example of this situation is if there are devices on the I²C bus which only supports fast mode (400kHz) while other devices on the bus support fast mode plus (1MHz). The example of this is presented in Figure 7.

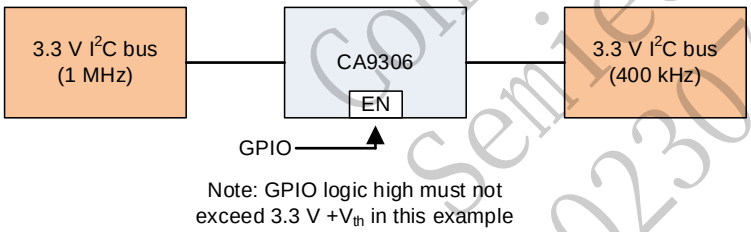


Figure 7 Example of an I²C bus with multiple supported Frequencies

In this situation, if the master is on the 1MHz side, then communicating at 1MHz should not be attempted if CA9306 were enabled. The CA9306 device needs to be disabled to avoid possibly glitching state machines in devices which were designed to operate correctly at 400kHz or slower. When CA9306 is disabled, the master can communicate with the 1MHz devices without disturbing the 400kHz bus. When the CA9306 is enabled, communication across both sides at 400kHz is acceptable.

10.1.4 Supporting Remote Board Insertion to Backplane with CA9306

Another situation where CA9306 is advantageous when using its enable feature is when a remote board with I²C lines is required to be attached to a main board (backplane) with an I²C bus such as in Figure 8. If the connection between remote board to a backplane is not done properly, it could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line, which could glitch an I²C device state machine causing the I²C bus to get stuck.

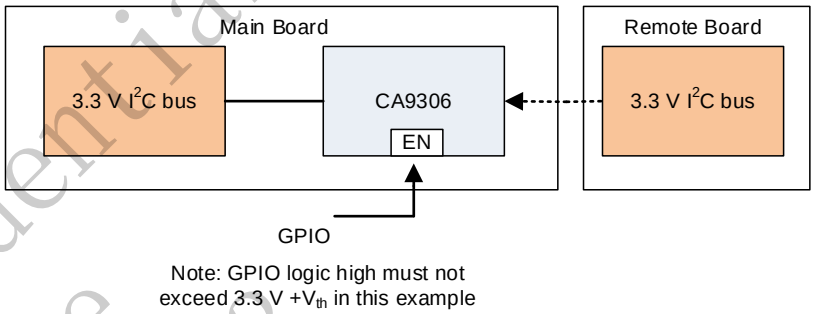


Figure 8 An Example of Connecting A Remote Board to A Main Board (Backplane)

CA9306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

10.1.5 Switch Configuration

CA9306 has the capability of being used with its V_{REF1} voltage equal to V_{REF2}. This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is displayed in Figure 9 and the translation mode is displayed in Figure 10.

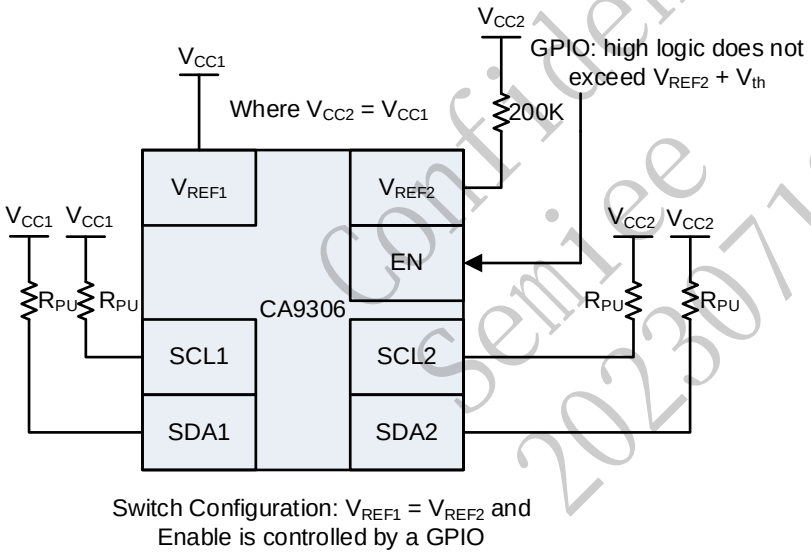


Figure 9 Switch Configuration

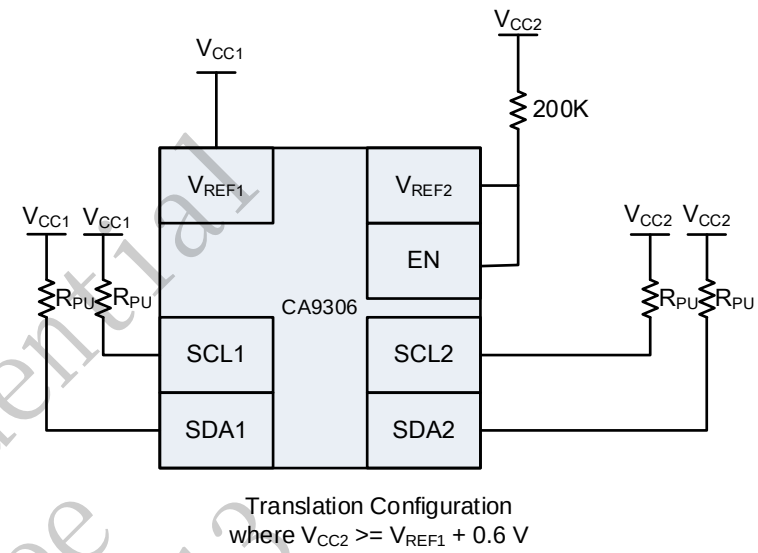


Figure 10 Translation Configuration

When CA9306 is in the switch configuration (V_{REF1} = V_{REF2}), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull-up resistance and capacitance on both sides of the bus are equal, then in switch mode, the CA9306 has the same propagation delay from side 1 to 2 and side 2 to 1. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8V is longer than at 5V in the switching configuration. When CA9306 is in translation mode, side 1propagate lows to side 2 faster than side 2 can propagate lows to side 1. This time difference becomes larger as the difference between V_{CC2} and V_{CC1} becomes larger.

10.1.6 Master on Side 1 or Side 2 of Device

I²C and SMBus are bidirectional protocol means that devices on the bus can both transmit and receive data. CA9306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the master to be able to be placed on either side of the device. Figure 11 represents the master on side two as opposed to the diagram in Figure 1.

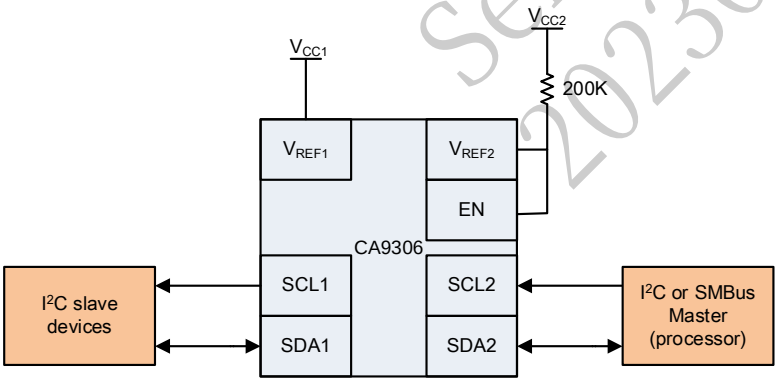


Figure 11 Master on Side 2 of CA9306

10.1.7 LDO and CA9306 Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some situations the LDO may lose its regulation because of the bias current from V_{REF2} to V_{REF1}. If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic), which results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when Vgs of the pass FET is equal to Vth, which means V_{REF1} node voltage is V_{CC2} - V_{th}. Note that any slaves/masters running off of the LDO now see the V_{CC2} - V_{th} voltage, which may result in damage to those slaves/masters if they are not rated to handle the increased voltage.

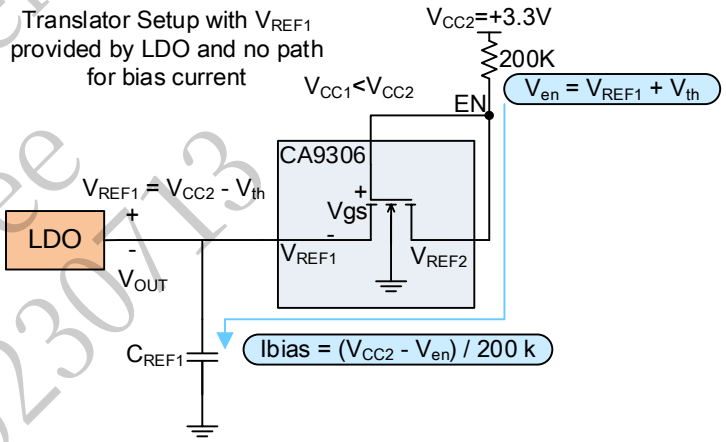


Figure 12 Example of No Leakage Current Path When Using LDO

To ensure LDO does not lose regulation caused by the bias current of CA9306, a weak pull-down resistor can be placed on VREF1 to ground, providing a path for the bias current to travel. The recommended pull-down resistor is calculated by Equation 4. (0.75 gives about 25% margin for error incase bias current increases during operation)

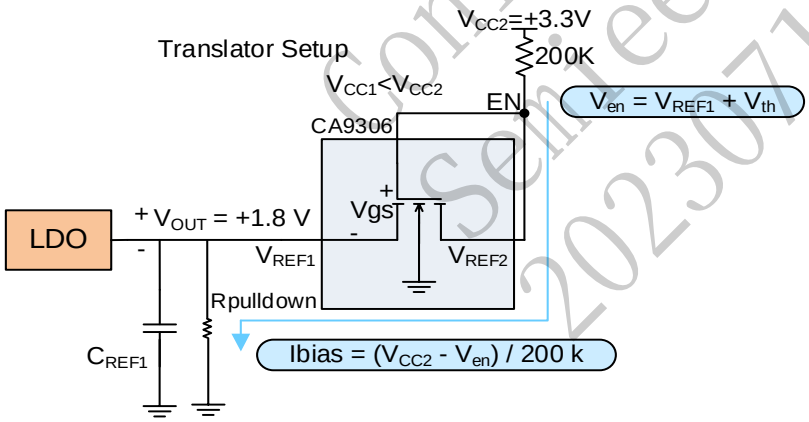


Figure 13 Example with Leakage Current Path When Using LDO

$V_{en} = V_{REF1} + V_{th}$ (1)

where

• V_{th} is approximately 0.6V

$I_{bias} = (V_{CC2} - V_{en})/200k$ (2)

$R_{pulldown} = V_{OUT}/I_{bias}$ (3)

Recommended $R_{pulldown} = R_{pulldown} \times 0.75$ (4)

10.1.8 Current Limiting Resistance on V_{REF2}

The resistor is used to limit the current between V_{REF2} and V_{REF1} (denoted as R_{CC}) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value. However, the bias current proportionally increases as the resistor decreases.

$I_{bias} = (V_{CC2} - V_{en})/R_{CC}$: $V_{en} = V_{REF1} + V_{th}$ (5)

where

• V_{th} is approximately 0.6V

Keep in mind R_{CC} should not be sized low enough that I_{CC} exceeds the absolute maximum continuous channel current specified in section 9.1 which is described in Equation 6.

$R_{CC}(min) \geq (V_{CC2} - V_{en})/0.128$: $V_{en} = V_{REF1} + V_{th}$ (6)

Where

•V_{th} is approximately 0.6V

10.2 Feature Description

10.2.1 Enable (EN) Pin

The CA9306 device is a double-pole, single-throw switch in which the voltage on the EN pin controls the gate of the transistors. The CA9306 device is always enabled when power is applied to V_{REF2} as shown in Figure 1. And the device is enabled when a control signal from a processor is in a logic-high state as shown in Figure 2.

10.2.2 Voltage Translation

The beginning feature of the CA9306 device is translating voltage from an I²C bus referenced to V_{REF1} up to an I²C bus referenced to V_{DPU}, to which V_{REF2} is connected through a 200kΩ pull-up resistor. Translation on a standard, open-drain I²C bus is achieved by simply connecting pull-up resistors from SCL1 and SDA1 to V_{REF1} and from SCL2 and SDA2 to V_{DPU}. Information on sizing the pull-up resistors can be found in the Sizing Pull-up Resistors section.

10.3 Device Functional Modes

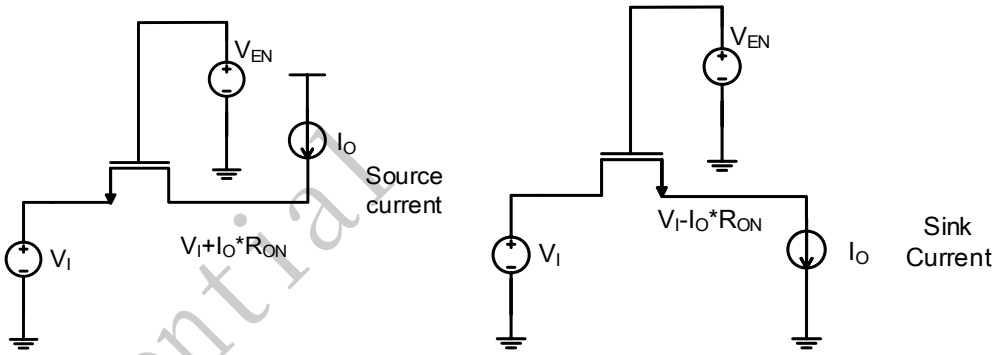
H = HIGH level; L = LOW level.

INPUT EN[1]	TRANSLATOR FUNCTION
H	SCL1 = SCL2; SDA1 = SDA2
L	Disconnect

Note:

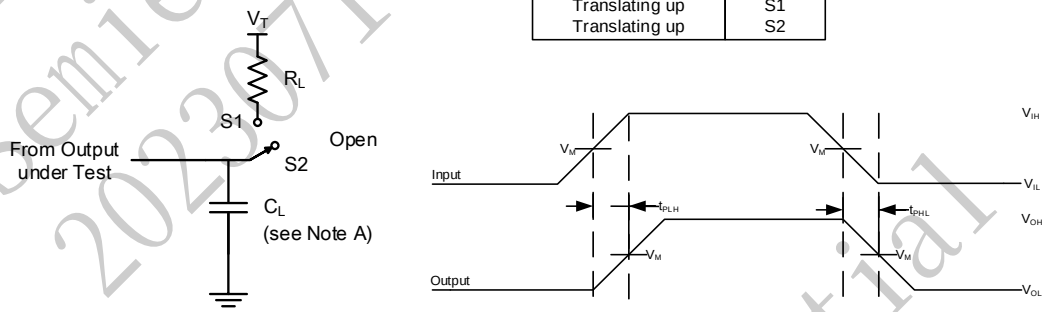
1. EN is controlled by the Vbias($_{REF2}$) logic levels and should be at least 1 V higher than V_{REF1} for best translator operation.

10.4 Parameter Measurement Information



a) Current Source Configuration b) Current Sink Configuration

Figure 14 Current Source and Current Sink Configurations for RON Measurements



USAGE	SWITCH
Translating up	S1
Translating up	S2

Notes:
A. CL includes probe and jig capacitance
B. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω , tr ≤ 2ns, tf ≤ 2ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 15 Load Circuit for Outputs

10.5 Application and Implementation

10.5.1 General Applications of I²C

As with the standard I²C system, pull-up resistors are required to provide the logic-high levels on the translator bus. Although the size of these pull-up resistors depends on the system, each side of the repeater must have a pull-up resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I²C devices only specify 3mA in a universal I²C system in which standard-mode devices and multiple masters are possible. High termination currents can be used under certain conditions. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. And when the SDA1 port is high, the SDA2 port is pulled to the pull-up supply voltage of the drain (V_{DPU}) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2.

10.5.2 Design Requirements

Parameter	Symbol	MIN	TYP[1]	MAX	UNIT
Reference Voltage	V_{REF2}	V_{REF1} + 0.6	2.1	5	V
Enable Input Voltage	EN	V_{REF1} + 0.6	2.1	5	V
Reference Voltage	V_{REF1}	1.2	1.5	4.4	V
Pass Switch Current	I_{PASS}		6		mA
Reference-transistor Current	I_{REF}		5		uA

Note:
1. All typical values are at T_A = 25°C.

10.6 Detailed Design Procedure

10.6.1 Bidirectional Voltage Translation

To ensure the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the enable (EN) input must be connected to V_{REF2} and both pins are pulled to high-side V_{DPU} through a pull-up resistor (typically 200 kΩ), which allows V_{REF2} to regulate the enable (EN) input. A 100pF filter capacitor connected to V_{REF2} is recommended. The I²C bus master output can be push-pull or open-drain (pull-up resistors may be required) and the I²C bus device output can be open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to avoid high-to-low contentions in either direction. If both outputs are open-drain, then no direction control is required.

10.6.2 Sizing Pull-up Resistors

To get an estimate for the range of values that can be used for the pull-up resistor. Figure 16 show the maximum pull-up resistance allowable by the I²C specification for standard-mode (100kHz) and fast-mode (400kHz) operation.

10.6.3 Application Curve

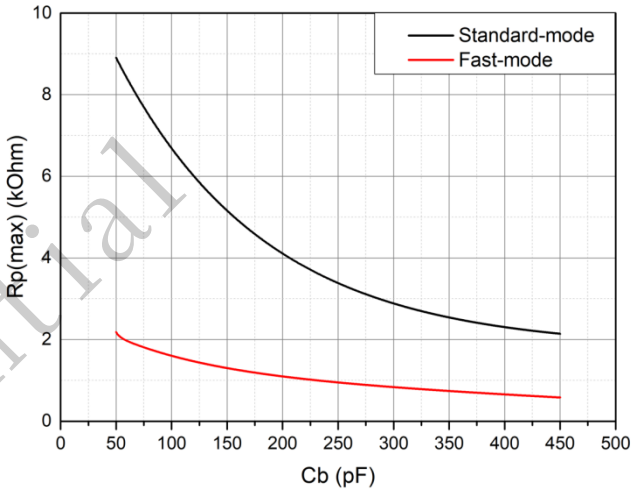


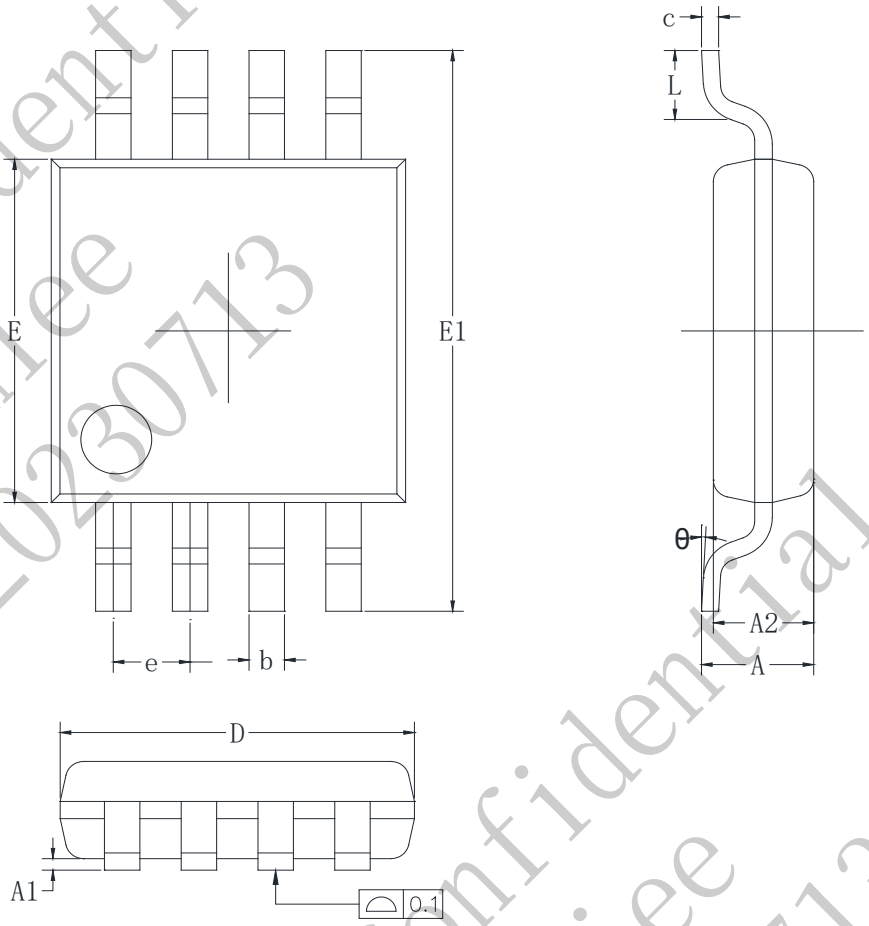
Figure 16 Maximum Pull-up Resistance (Rp(max)) vs Bus Capacitance (Cb)

11. Package Outline Dimensions and Recommend Land Pattern Layout

11.1 MSOP-8

Package Outline Dimensions

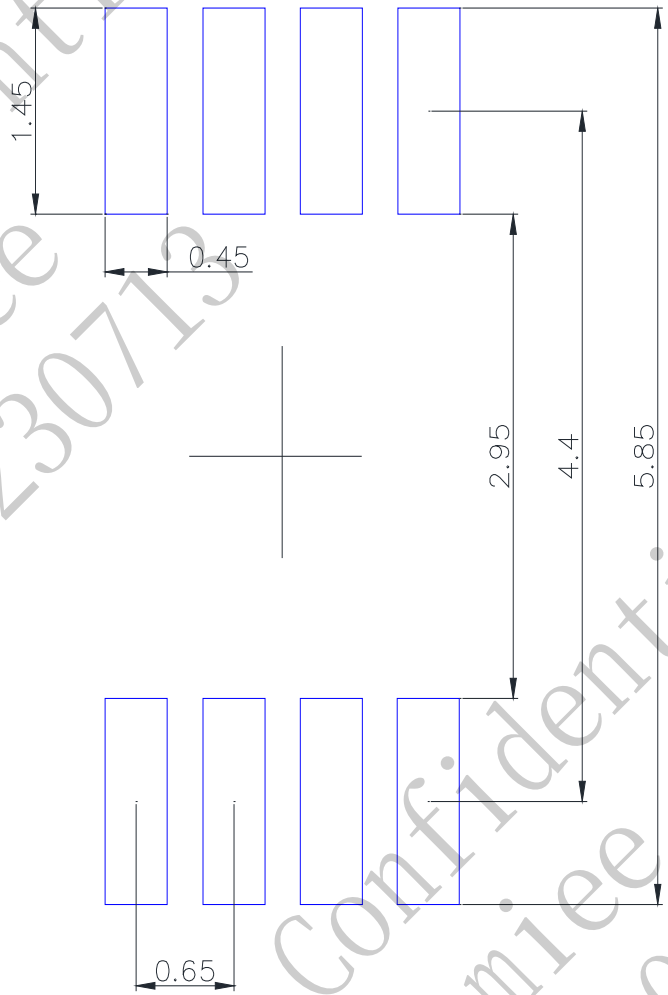
MSOP-8 Unit (mm)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.250	0.004	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650（BSC）		0.026（BSC）	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Recommended Land Pattern Layout

MSOP-8 Unit (mm)



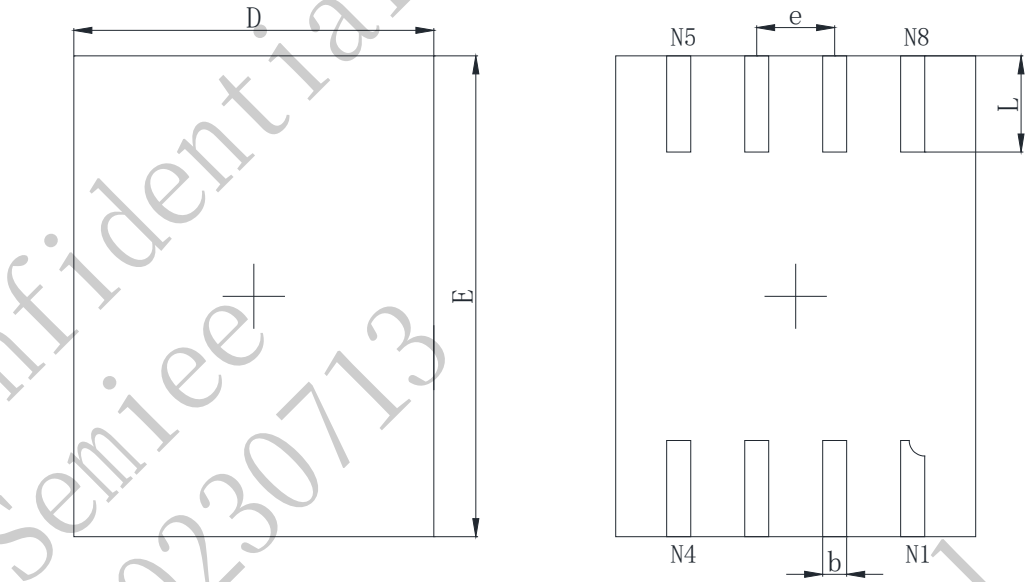
Notes:

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. Change without notice

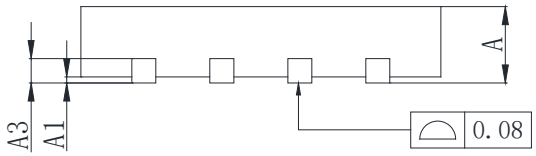
11.2 DFN3x4-8

Package Outline Dimensions

DFN3x4-8 Unit (mm)



Top View **Bottom View**



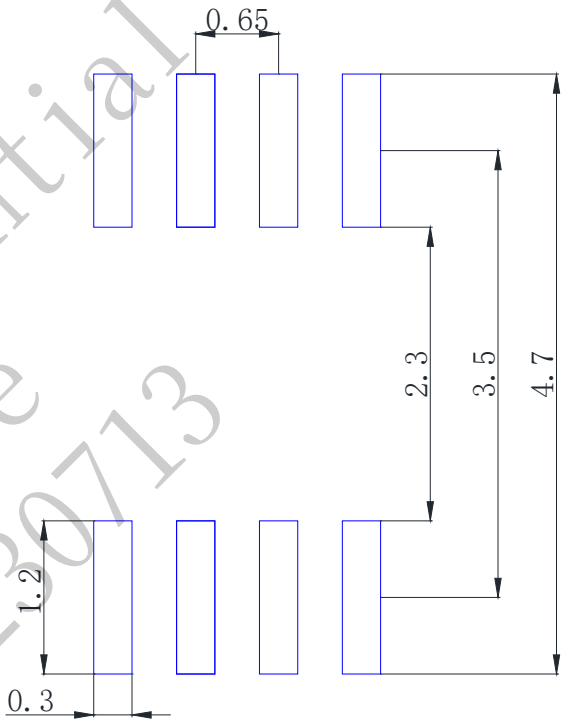
Side View

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF	
D	2.900	3.100	0.114	0.122
E	3.900	4.100	0.154	0.161
b	0.150	0.250	0.006	0.010
e	0.650TYP.		0.025TYP	
L	0.700	0.900	0.028	0.035

Note： pin 1 shape on backside is not limited to bevel, it can be a notch or arch.

Recommended Land Pattern Layout

DFN3x4-8 Unit (mm)



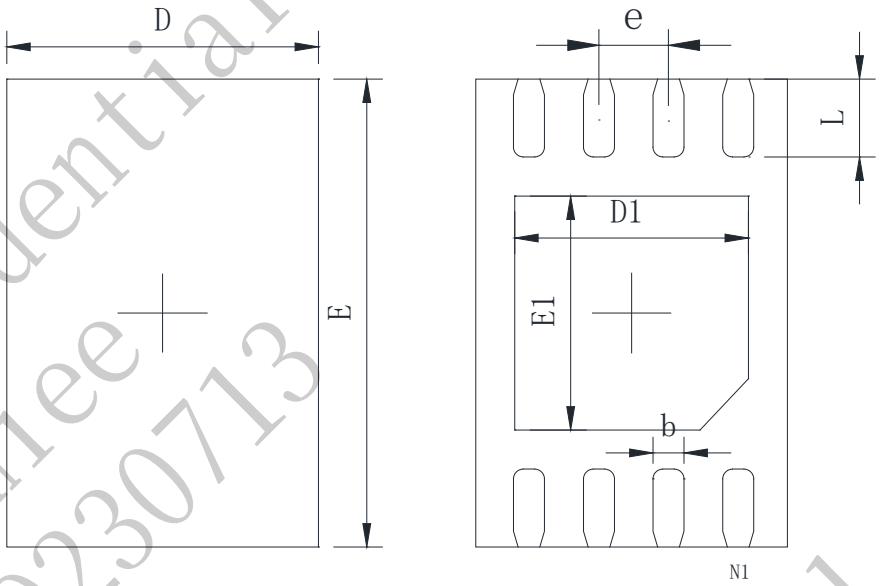
Notes:

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. Change without notice

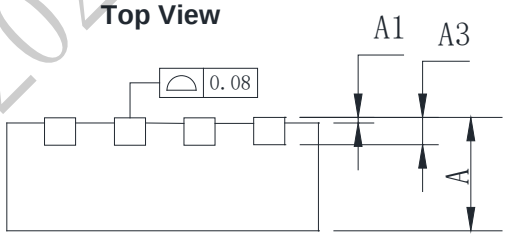
11.3 DFN2x3-8

Package Outline Dimensions

DFN2x3-8 Unit (mm)



Top View **Bottom View**



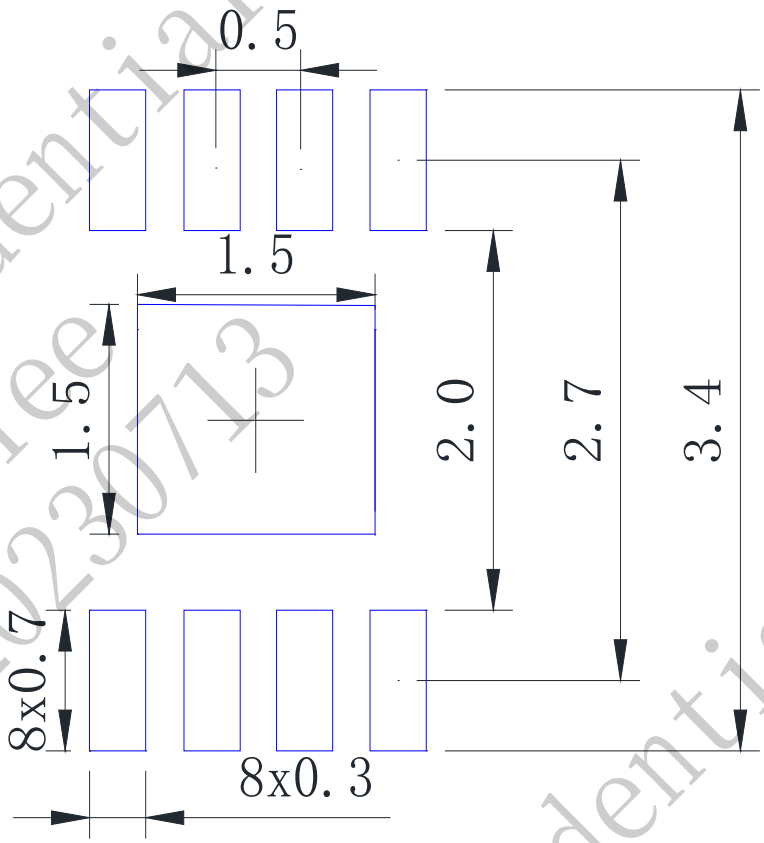
Side View

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF	
D	1.900	2.100	0.075	0.083
E	2.900	3.100	0.114	0.122
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP	
L	0.200	0.500	0.008	0.020

Note： pin 1 shape on backside is not limited to bevel, it can be a notch or arch.

Recommended Land Pattern Layout

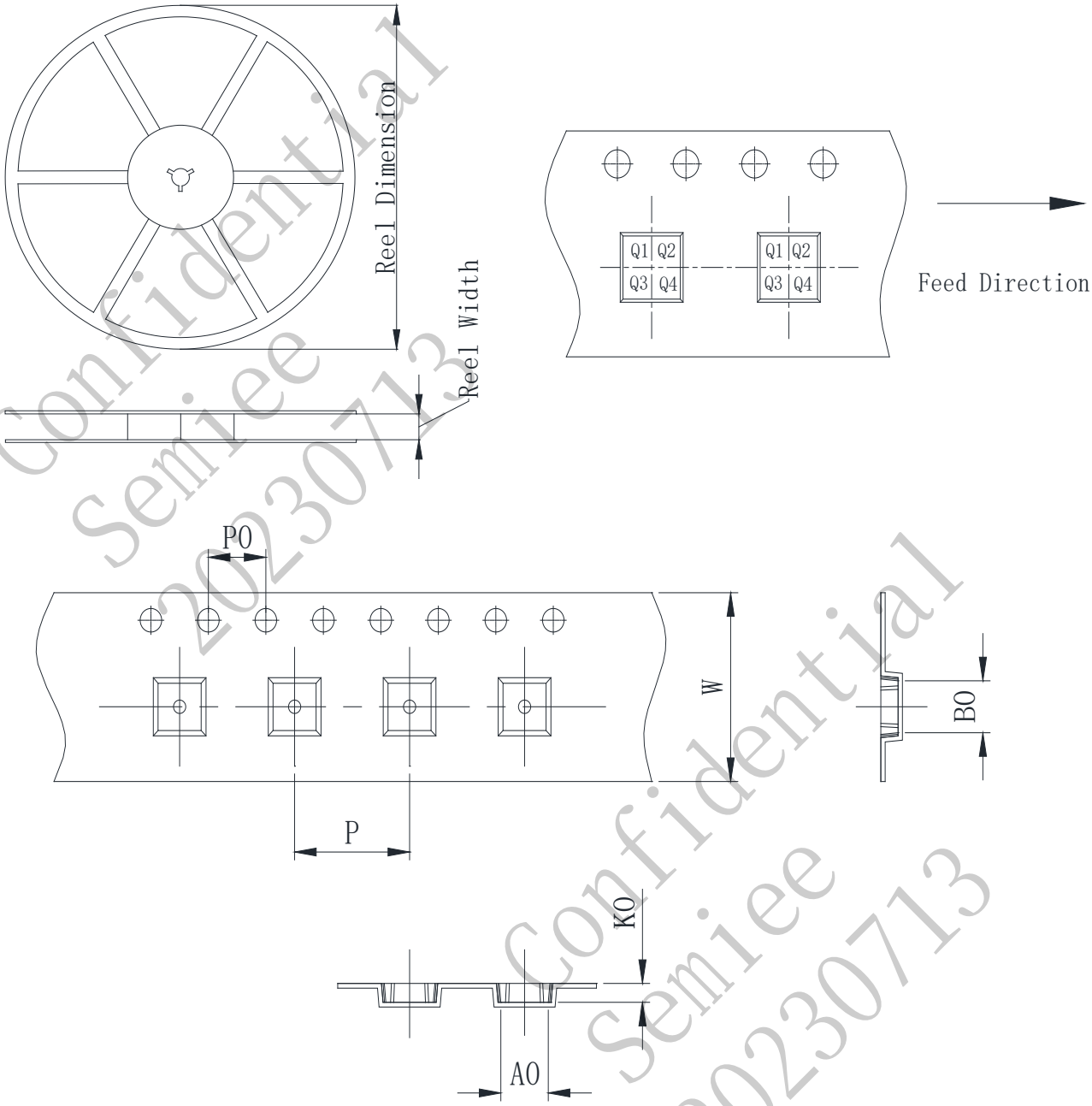
DFN2x3-8 Unit (mm)



Notes：

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. If the thermal pad is not necessary, designer can leave the land pattern area blank
4. Change without notice

12. Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
MSOP-8	13'	330	12.8	5.2	3.3	1.5	8.0	4.0	12.0	Q1
DFN3x4-8	13'	330	12.4	3.3	4.3	1.0	8.0	4.0	12.0	Q2
DFN2x3-8	7'	180	9.5	3.3	2.3	1.1	4.0	4.0	8.0	Q1

13. Revision History

Version	Date	Change Content
Ver1.0	2022/09	Advanced Version

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