DATA SHEET

74ALS109A

Dual J-$\overline{K}$ positive edge-triggered flip-flop with set and reset

Product specification

1991 Feb 08

IC05 Data Handbook

Philips
Semiconductors

PHILIPS

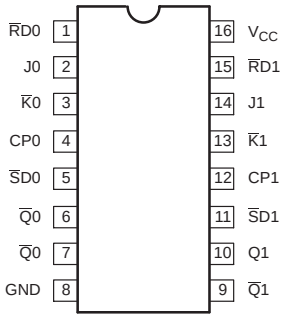
Dual J-$\overline{K}$ positive edge triggered flip-flop with set and reset

74ALS109A

DESCRIPTION

The 74ALS109A is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{S}$D) and reset ($\overline{R}$D) are asynchronous active-Low inputs and operate independently of the clock (CP) input. The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

PIN CONFIGURATION



SF00135

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS109A	150MHz	3.0mA

ORDERING INFORMATION

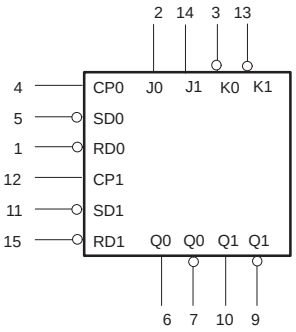
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74ALS109AN	SOT38-4
16-pin plastic SO	74ALS109AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/2.0	20µA/0.2mA
$\overline{K}$0, $\overline{K}$1	$\overline{K}$ inputs	1.0/2.0	20µA/0.2mA
CP0, CP1	Clock inputs (active rising edge)	1.0/2.0	20µA/0.2mA
$\overline{S}$D0, $\overline{S}$D1	Set inputs (active-Low)	1.0/4.0	20µA/0.4mA
$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active-Low)	1.0/4.0	20µA/0.4mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

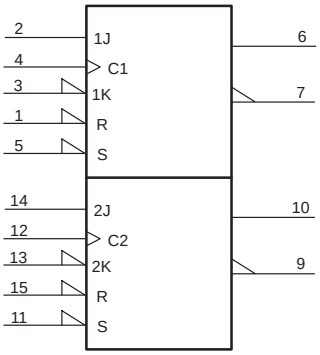
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

SF00136

IEC/IEEE SYMBOL

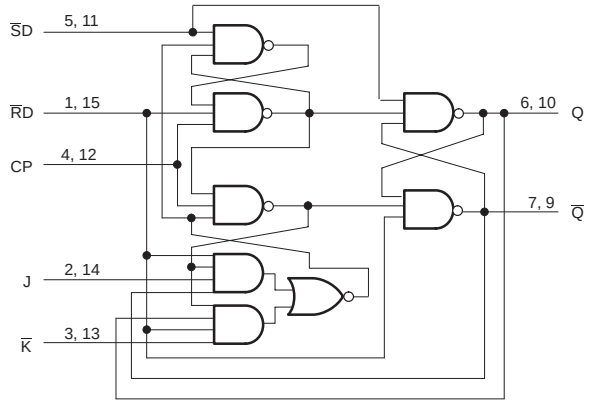


SF00137

Dual J-$\overline{K}$ positive edge triggered flip-flop with set and reset

74ALS109A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H*	H*	Undetermined*
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load “0”
H	H	↑	h	h	H	L	Load “1”
H	H	↑	l	h	q	$\overline{q}$	Hold “no change”
H	H	L	l	h	q	$\overline{q}$	Hold “no change”

H = High voltage level
h = High state must be present one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time prior to Low-to-High clock transition
q = Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don’t care
↑ = Low-to-High clock transition
* = The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the set and reset are near V_{IN} maximum. Furthermore, this configuration is nonstable; that is, it will not remain when either set or reset returns to its inactive (High) level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –0.4mA	V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.5	V
I_I	Input current at maximum input voltage	Jn, $\overline{K}$n, CPn	V_{CC} = MAX, V_I = 7.0V				0.1	mA
		$\overline{S}$Dn, $\overline{R}$Dn					0.2	mA
I_{IH}	High–level input current	Jn, $\overline{K}$n, CPn	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{S}$Dn, $\overline{R}$Dn					40	µA
I_{IL}	Low–level input current	Jn, $\overline{K}$n, CPn	V_{CC} = MAX, V_I = 0.4V				–0.2	mA
		$\overline{S}$Dn, $\overline{R}$Dn					–0.4	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		–30		–112	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			3.0	4.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

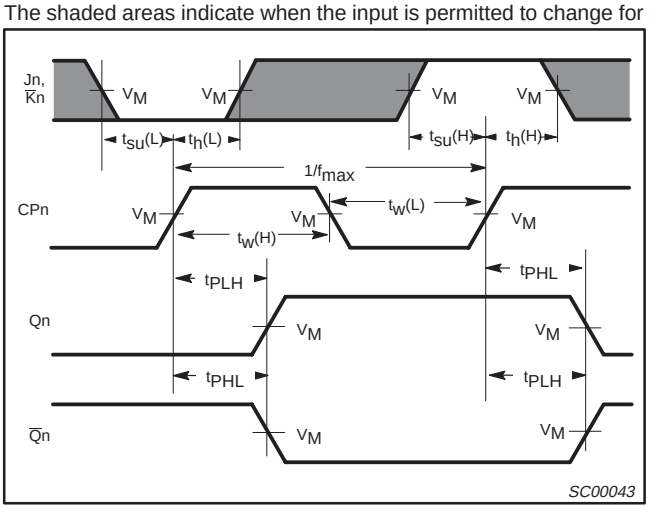
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.0 3.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn or $\overline{R}$D to Qn or $\overline{Q}$n	Waveform 2, 3	1.0 3.0	8.0 10.0	ns

AC SETUP REQUIREMENTS

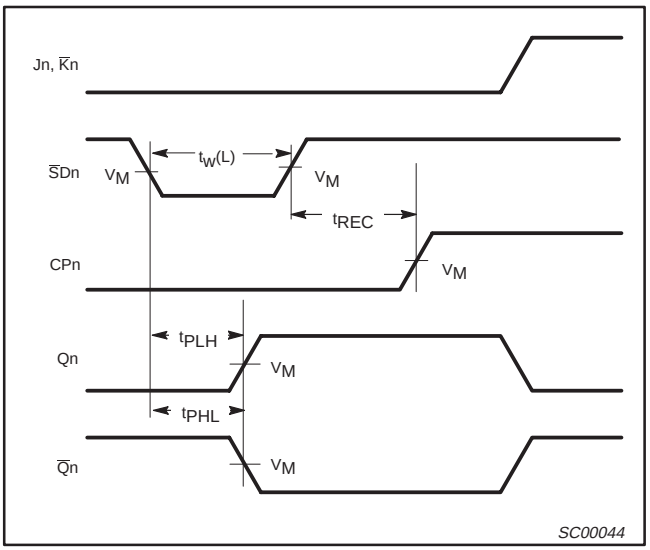
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, High or Low Jn, $\overline{K}$n to CPn	Waveform 1	6.0 6.0		ns
t_h (H) t_h (L)	Hold time, High or Low Jn, $\overline{K}$n to CPn	Waveform 1	0.0 0.0		ns
t_w (H) t_w (L)	CPn Pulse width High or Low	Waveform 1	6.0 6.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn Pulse width Low	Waveform 2, 3	6.0		ns
t_{rec}	Recovery time, $\overline{S}$Dn or $\overline{R}$Dn to CPn	Waveform 2, 3	6.0		ns

AC WAVEFORMS

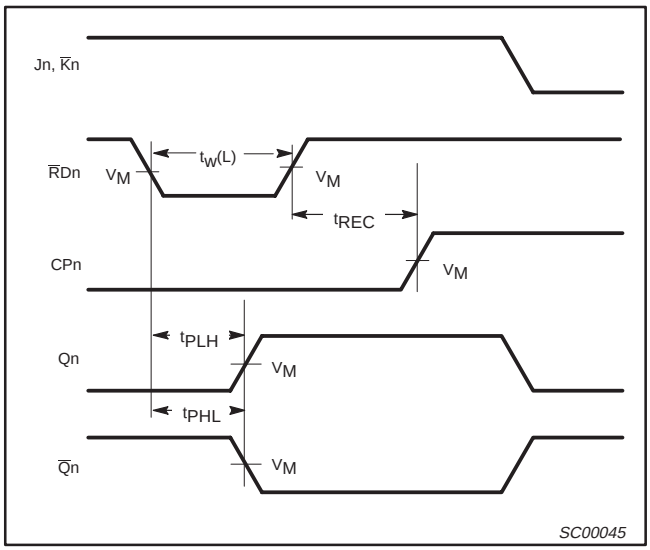
For all waveforms, V_M = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, Clock Width, and Maximum Clock Frequency

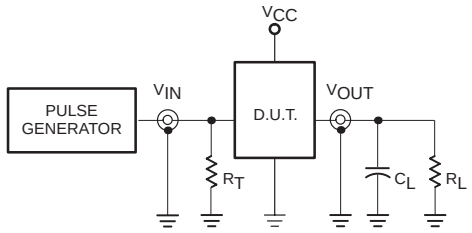


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width and Recovery Time for Set to Clock

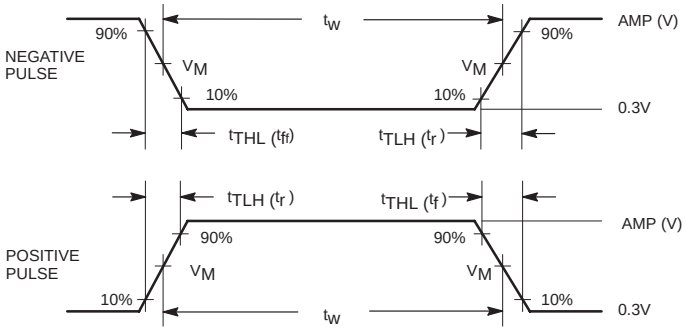


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width and Recovery Time for Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

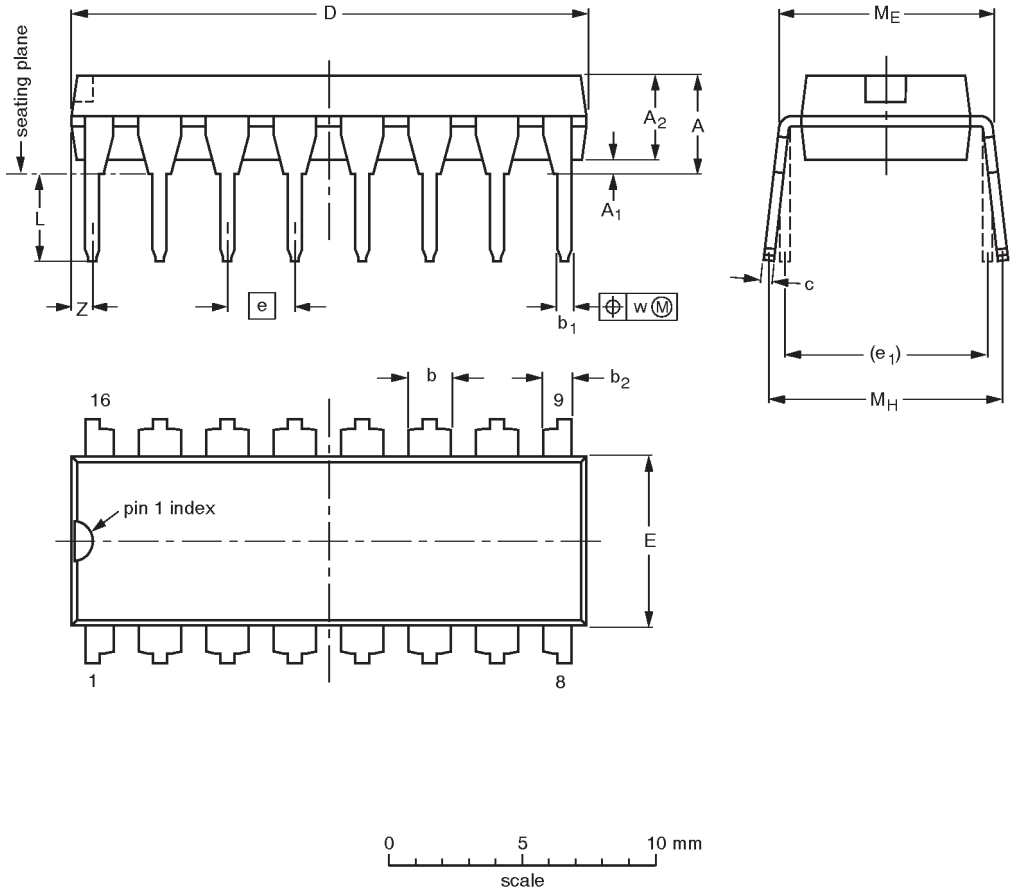
R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SC00005

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

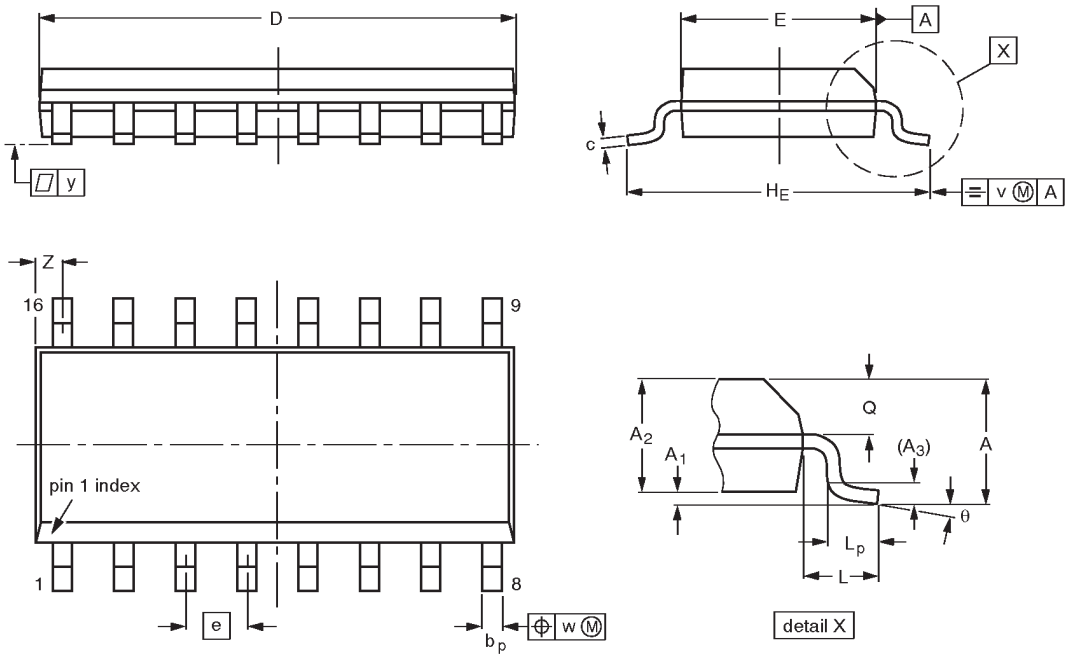
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

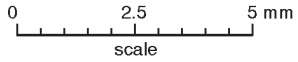
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

Dual J-$\overline{K}$ positive edge-triggered flip-flop with set and reset

74ALS109A

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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