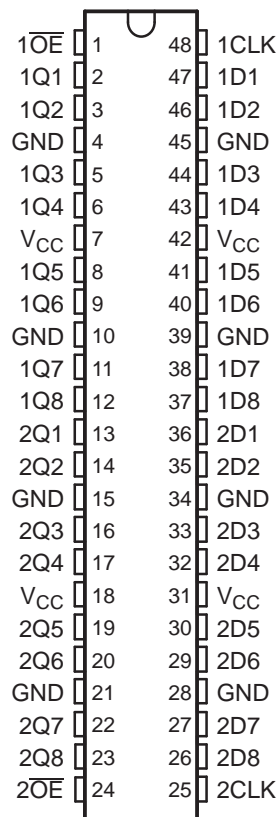


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH162374... WD PACKAGE  
SN74LVTH162374... DGG OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Reel of 1000	74LVTH162374GRDR	LL2374
	FBGA – ZRD (Pb-free)		74LVTH162374ZRDR	
	SSOP – DL	Tube of 25	SN74LVTH162374DL	LVTH162374
			SN74LVTH162374DLG4	
		Reel of 1000	74LVTH16374DLRG4 SN74LVTH16374DLR	
	TSSOP – DGG	Reel of 2000	SN74LVTH162374DGGR 74LVTH162374DGGRG4	LVTH162374
VFBGA – GQL	Reel of 1000	SN74LVTH162374GQLR	LL2374	
		74LVTH162374ZQLR		
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH162374WD	SNJ54LVTH162374WD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN54LVTH162374, SN74LVTH162374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS262M—JULY 1993—REVISED NOVEMBER 2006

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### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The LVTH162374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

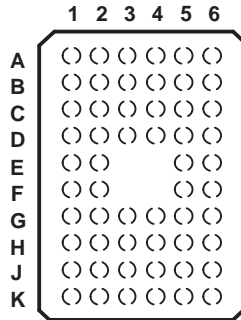
The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

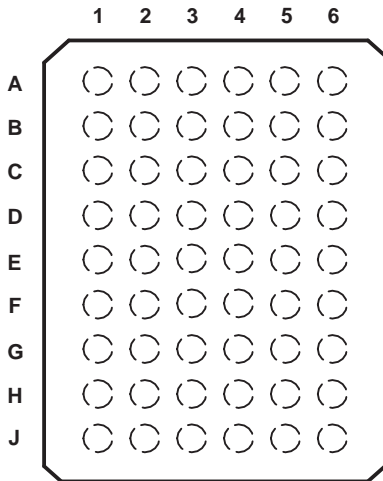


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	1 $\overline{OE}$	NC	NC	NC	NC	1CLK
<b>B</b>	1Q2	1Q1	GND	GND	1D1	1D2
<b>C</b>	1Q4	1Q3	V <sub>CC</sub>	V <sub>CC</sub>	1D3	1D4
<b>D</b>	1Q6	1Q5	GND	GND	1D5	1D6
<b>E</b>	1Q8	1Q7			1D7	1D8
<b>F</b>	2Q1	2Q2			2D2	2D1
<b>G</b>	2Q3	2Q4	GND	GND	2D4	2D3
<b>H</b>	2Q5	2Q6	V <sub>CC</sub>	V <sub>CC</sub>	2D6	2D5
<b>J</b>	2Q7	2Q8	GND	GND	2D8	2D7
<b>K</b>	2 $\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

	1	2	3	4	5	6
<b>A</b>	1Q1	NC	1 $\overline{OE}$	1CLK	NC	1D1
<b>B</b>	1Q3	1Q2	NC	NC	1D2	1D3
<b>C</b>	1Q5	1Q4	V <sub>CC</sub>	V <sub>CC</sub>	1D4	1D5
<b>D</b>	1Q7	1Q6	GND	GND	1D6	1D7
<b>E</b>	2Q1	1Q8	GND	GND	1D8	2D1
<b>F</b>	2Q3	2Q2	GND	GND	2D2	2D3
<b>G</b>	2Q5	2Q4	V <sub>CC</sub>	V <sub>CC</sub>	2D4	2D5
<b>H</b>	2Q7	2Q6	NC	NC	2D6	2D7
<b>J</b>	2Q8	NC	2 $\overline{OE}$	2CLK	NC	2D8

(1) NC – No internal connection

**FUNCTION TABLE  
(EACH FLIP-FLOP)**

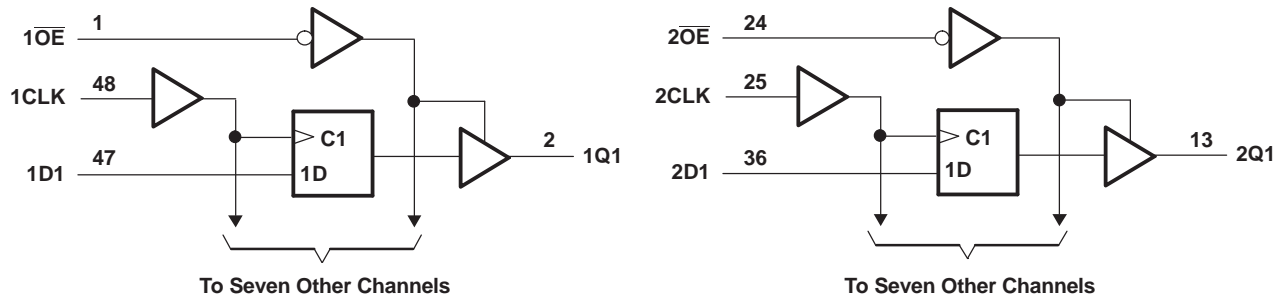
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

# SN54LVTH162374, SN74LVTH162374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS262M—JULY 1993—REVISED NOVEMBER 2006

### LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state		30	mA
$I_O$	Current into any output in the high state <sup>(3)</sup>		30	mA
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		SN54LVTH162374		SN74LVTH162374		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-12		-12	mA
$I_{OL}$	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH162374		SN74LVTH162374		UNIT	
			MIN	TYP <sup>(1)</sup>	MAX	MIN		TYP <sup>(1)</sup>
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$				-1.2		V	
$V_{OH}$	$V_{CC} = 3\text{ V}$ , $I_{OH} = -12\text{ mA}$		2		2		V	
$V_{OL}$	$V_{CC} = 3\text{ V}$ , $I_{OL} = 12\text{ mA}$				0.8		V	
$I_I$	Control inputs	$V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$			10		$\mu\text{A}$	
		$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$			
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$	1		1		
			$V_I = 0$	-5		-5		
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						$\pm 100$	$\mu\text{A}$
$I_{I(\text{hold})}$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75		75		$\mu\text{A}$
			$V_I = 2\text{ V}$	-75		-75		
		$V_{CC} = 3.6\text{ V}$ , <sup>(2)</sup>	$V_I = 0\text{ to }3.6\text{ V}$				500 -750	
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$				5		$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$				-5		$\mu\text{A}$	
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$				$\pm 100$ <sup>(3)</sup>		$\mu\text{A}$	
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$				$\pm 100$ <sup>(3)</sup>		$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19		0.19	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.19	
$\Delta I_{CC}$ <sup>(4)</sup>	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$				0.2		0.2	mA
$C_i$	$V_I = 3\text{ V or }0$				3		3	pF
$C_o$	$V_O = 3\text{ V or }0$				9		9	pF

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH162374				SN74LVTH162374				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	160		160		160		160		MHz
$t_w$	Pulse duration, CLK high or low	3		3.3		3		3		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	2.8		3.2		1.8		2		ns
$t_h$	Hold time, data after CLK $\uparrow$	1.2		0.5		0.8		0.1		ns

# SN54LVTH162374, SN74LVTH162374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS262M–JULY 1993–REVISED NOVEMBER 2006

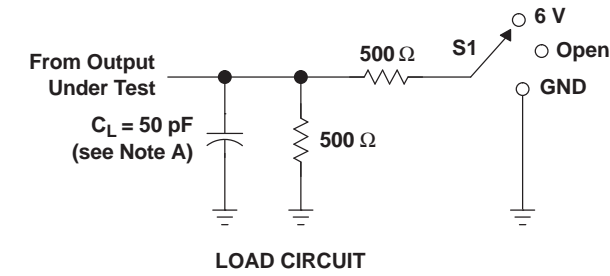
### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

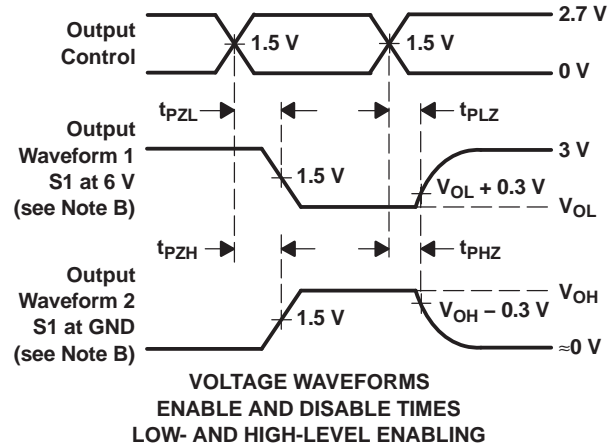
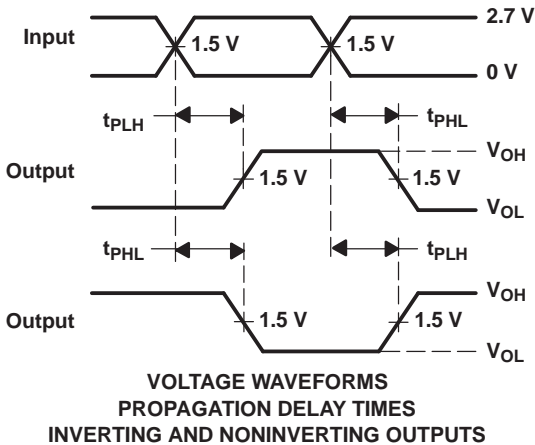
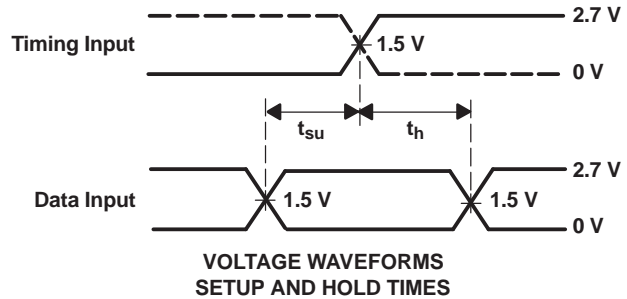
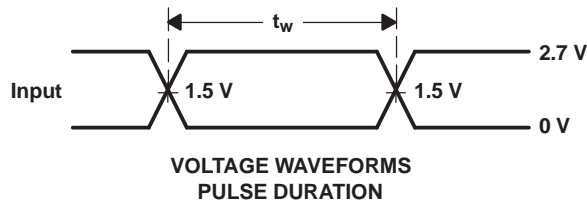
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162374				SN74LVTH162374				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN		MAX
$f_{max}$			160		160		160			160		MHz
$t_{PLH}$	CLK	Q	1.4	6.6	7.4		2	3.4	5.3	6.2		ns
$t_{PHL}$			1.4	5.8	6		2.2	3.3	4.9	5.1		
$t_{PZH}$	$\overline{OE}$	Q	1	6.6	7.4		1.8	3.5	5.6	6.9		ns
$t_{PZL}$			1.4	6	6.8		1.8	3.5	4.9	6		
$t_{PHZ}$	$\overline{OE}$	Q	1	6.6	7.4		2.4	4.2	5.4	5.7		ns
$t_{PLZ}$			1.4	6	6		2	3.8	5	5.1		
$t_{sk(LH)}$								0.5			ns	
$t_{sk(HL)}$								0.5				

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9854201VXA	ACTIVE	CFP	WD	48	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9854201VX A SNV54LVTH16237 4WD	<a href="#">Samples</a>
SN74LVTH162374DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374	<a href="#">Samples</a>
SN74LVTH162374DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374	<a href="#">Samples</a>
SN74LVTH162374DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162374	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVTH162374, SN54LVTH162374-SP, SN74LVTH162374 :**

- Catalog: [SN74LVTH162374](#), [SN54LVTH162374](#)
  
- Military: [SN54LVTH162374](#)
  
- Space: [SN54LVTH162374-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Military - QML certified for Military and Defense Applications
  
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH162374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH162374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

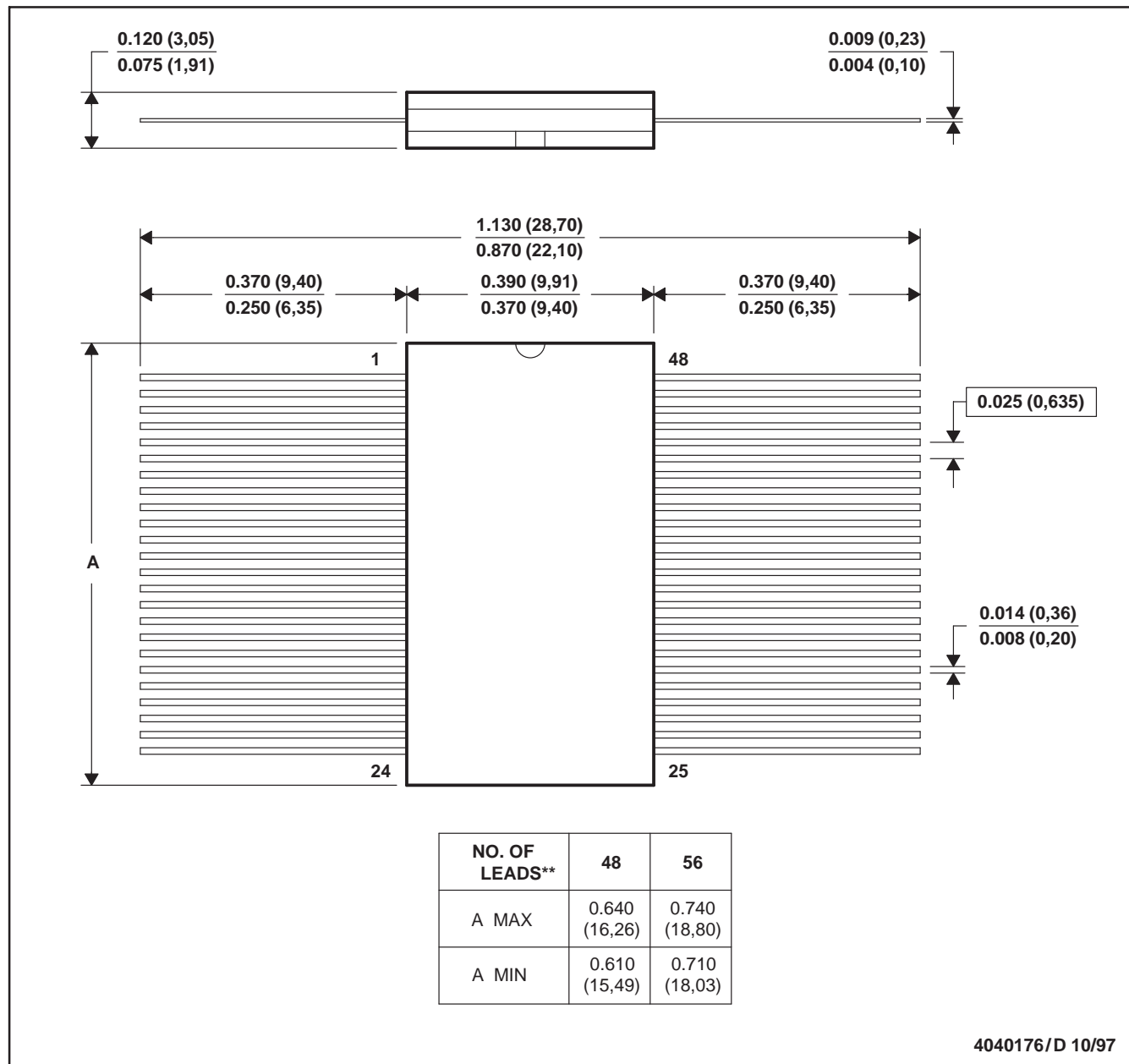

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH162374DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH162374DLR	SSOP	DL	48	1000	367.0	367.0	55.0

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



# EXAMPLE BOARD LAYOUT

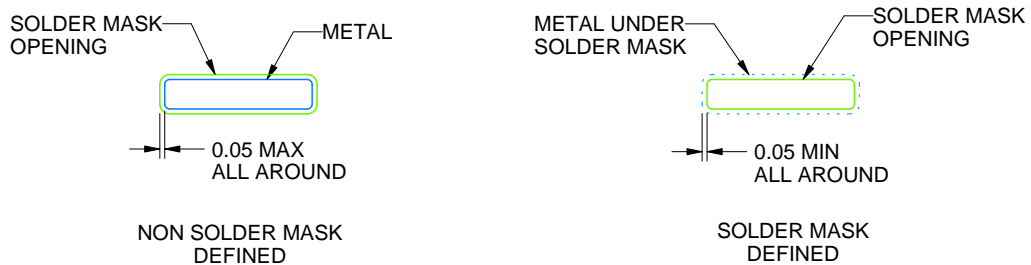
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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