

XC7SET04

Inverter

Rev. 01 — 1 September 2009

Product data sheet

1. General description

XC7SET04 is a high-speed Si-gate CMOS devices. It provides an inverting buffer.

2. Features

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT353-1 and SOT753 package options
- ESD protection:
 - ◆ HBM JESD22-A114E: exceeds 2000 V
 - ◆ MM JESD22-A115-A: exceeds 200 V
 - ◆ CDM JESD22-C101C: exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---|--------|---|----------|
| | Temperature range | Name | Description | Version |
| XC7SET04GW | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 |
| XC7SET04GV | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SC-74A | plastic surface-mounted package; 5 leads | SOT753 |

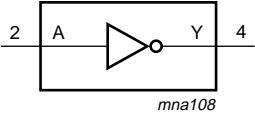
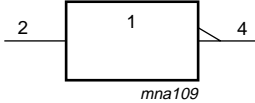
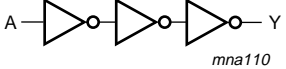
4. Marking

Table 2. Marking codes

| Type number | Marking ^[1] |
|-------------|------------------------|
| XC7SET04GW | gC |
| XC7SET04GV | g04 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

| | | |
|---|---|--|
|  <p>Fig 1. Logic symbol</p> |  <p>Fig 2. IEC logic symbol</p> |  <p>Fig 3. Logic diagram</p> |
|---|---|--|

6. Pinning information

6.1 Pinning

XC7SET04

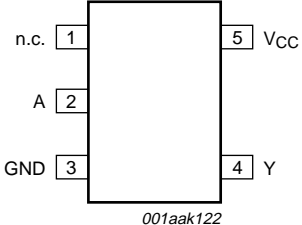


Fig 4. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)

6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| n.c. | 1 | not connected |
| A | 2 | data input |
| GND | 3 | ground (0 V) |
| Y | 4 | data output |
| V _{CC} | 5 | supply voltage |

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

| Input | Output |
|-------|--------|
| A | Y |
| L | H |
| H | L |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|-------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] - | ±20 | mA |
| I_O | output current | -0.5 V < V_O < $V_{CC} + 0.5$ V | - | ±25 | mA |
| I_{CC} | supply current | | - | 75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [2] - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|------------|-----|-----|----------|------|
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | - | - | 20 | ns/V |

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|-----|------|------------------|------|-------------------|------|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $I_O = -50 \mu\text{A}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -8.0 \text{ mA}$ | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $I_O = 50 \mu\text{A}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 8.0 \text{ mA}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I_I | input leakage current | $V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$ | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$ | - | - | 1.0 | - | 10 | - | 40 | μA |
| ΔI_{CC} | additional supply current | per input pin; $V_I = 3.4 \text{ V};$ other inputs at V_{CC} or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$ | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | | - | 1.5 | 10 | - | 10 | - | 10 | pF |

11. Dynamic characteristics

Table 8. Dynamic characteristics
GND = 0 V. For test circuit see Figure 6.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|--|---------------------|-----|-----|------------------|-----|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{pd} | propagation delay | A to Y; see Figure 5 [1] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V [2] | | | | | | | | |
| | | C _L = 15 pF | - | 3.4 | 6.7 | 1.0 | 7.5 | 1.0 | 8.5 | ns |
| | | C _L = 50 pF | - | 4.9 | 7.7 | 1.0 | 8.5 | 1.0 | 10.0 | ns |
| C _{PD} | power dissipation capacitance | per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} | [3] | - | 16 | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] Typical values are measured at V_{CC} = 5.0 V.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;

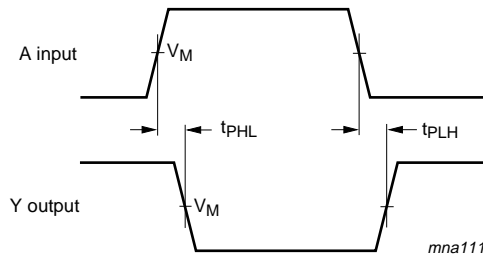
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms

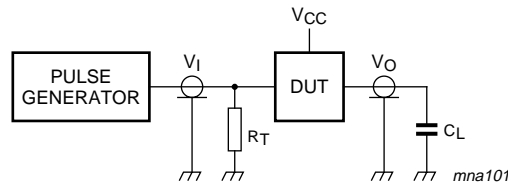


Measurement points are given in [Table 9](#).

Fig 5. Input (A) to output (Y) propagation delays

Table 9. Measurement point

| Type | Input | Input | Output |
|----------|--------------|-------|---------------------|
| | V_I | V_M | V_M |
| XC7SET04 | GND to 3.0 V | 1.5 V | $0.5 \times V_{CC}$ |



Test data is given in [Table 10](#). Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 6. Load circuitry for switching times

Table 10. Test data

| Type | Input | | Load | Test |
|----------|-------|---------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| XC7SET04 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753



Fig 8. Package outline SOT753 (SC-74A)

14. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

15. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| XC7SET04_1 | 20090901 | Product data sheet | - | - |

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16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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