MN195902

Digital Signal Processor for Image CODEC

■ Overview

The MN195902 is a high-speed, programmable digital signal processor based on a vector pipeline architecture for image processing applications. It incorporates many features that make it ideal for highly efficient coding and decoding of still and moving pictures in applications involving the transmission, storage, and retrieval of images.

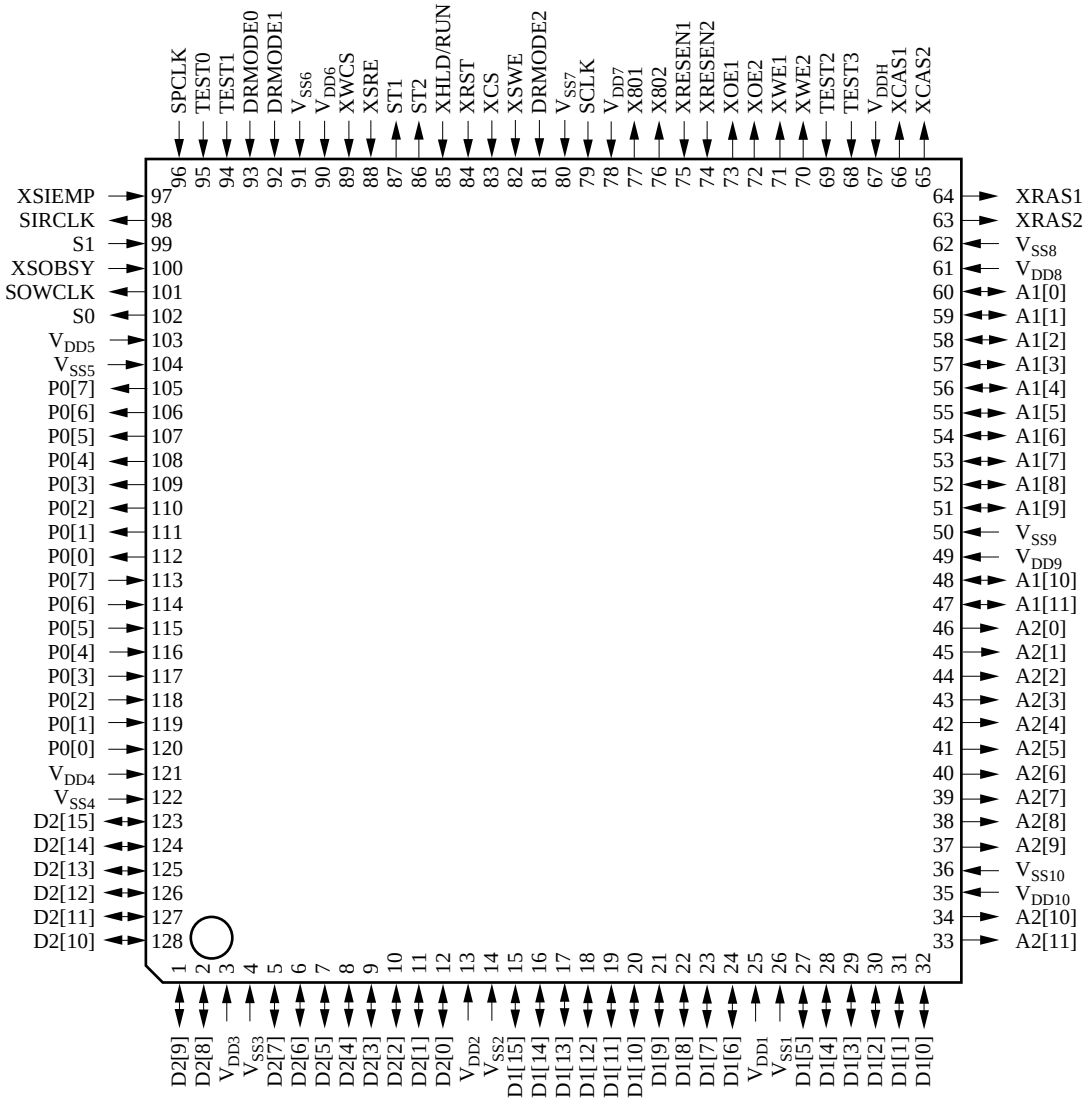
■ Features

- Flexible support for complex processing by simply rewriting the contents of its internal program memory
- Built-in dedicated hardware effective for image CODEC, including
  - Discrete cosine transform (DCT) converter
  - Two-dimensional address generator
- Architecture that links internal memory, a general-purpose arithmetic unit, dedicated arithmetic unit, and other components with a pipeline to better support vector calculations, multiply-and-accumulate, and other key image processing operations
- ITU-T H.261 coding for the QCIF size (176 × 144) with a decoding rate of 15 frames per second or higher

■ Applications

- Image-based communications:
  Moving picture videophones, video conferencing systems, cable television systems, image LANs, remote monitoring systems, etc.
- Image storage and retrieval:
  Electronic still cameras, optical disc files, image databases, etc.
- Multimedia computers

■ Pin Assignment



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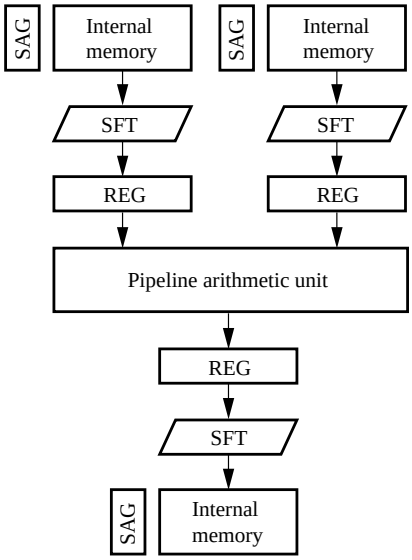
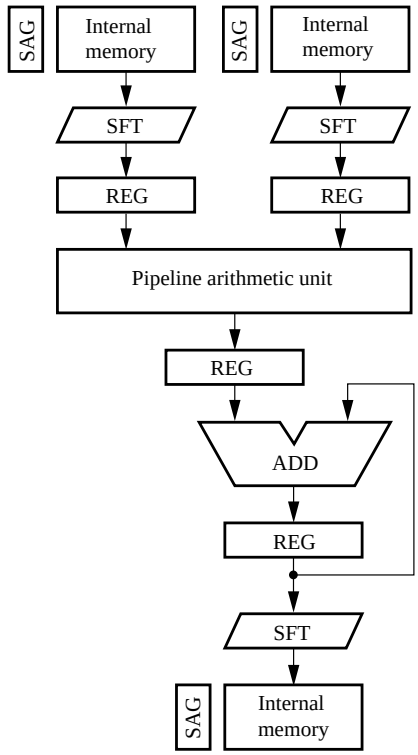
■ Vector Pipeline Processing Examples

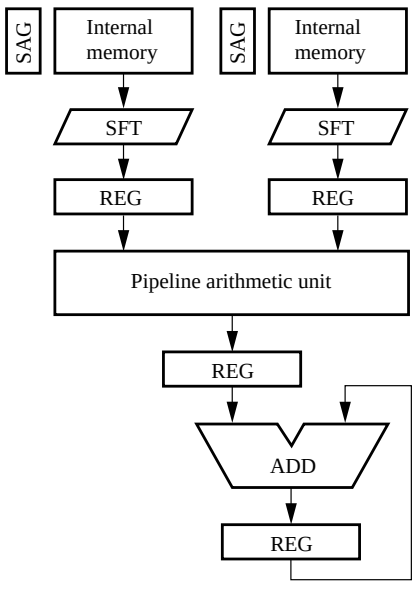
P instruction



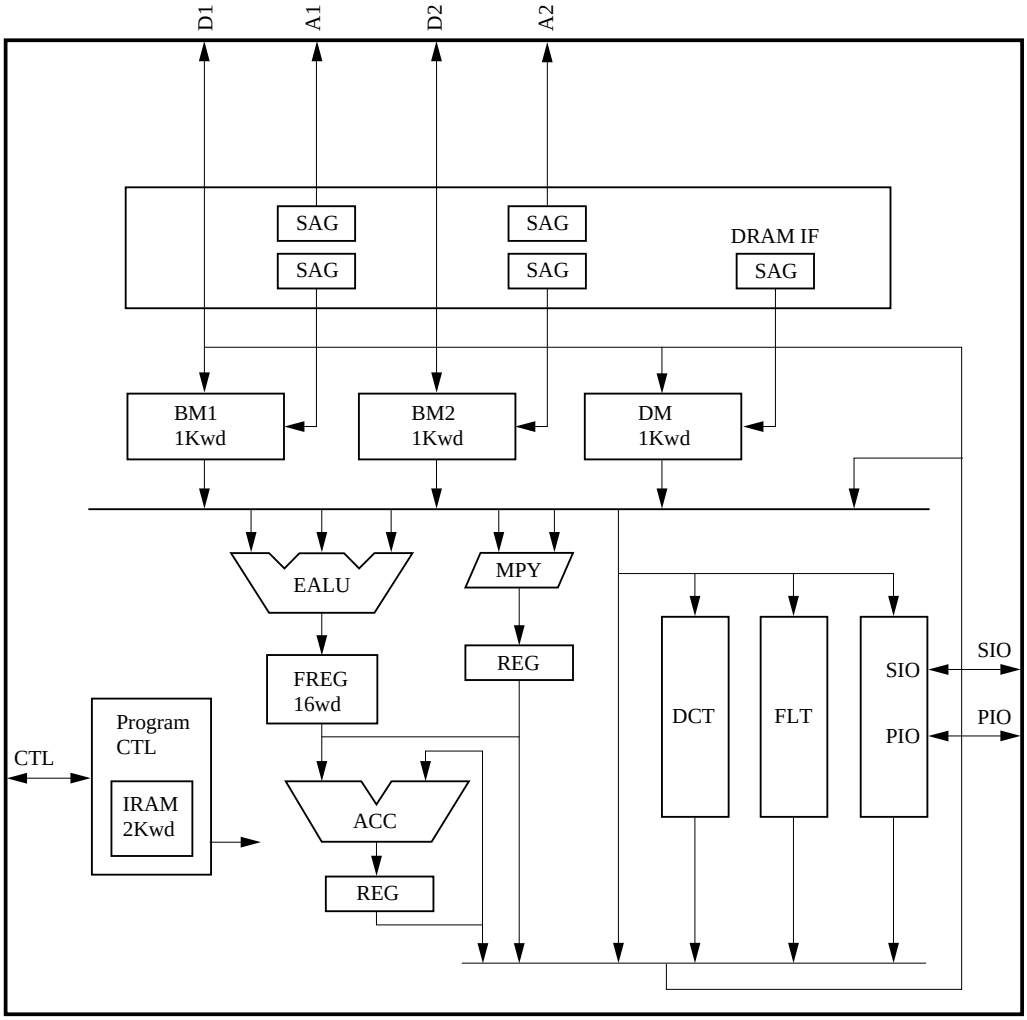
QP instruction



Q instruction



■ Block Diagram

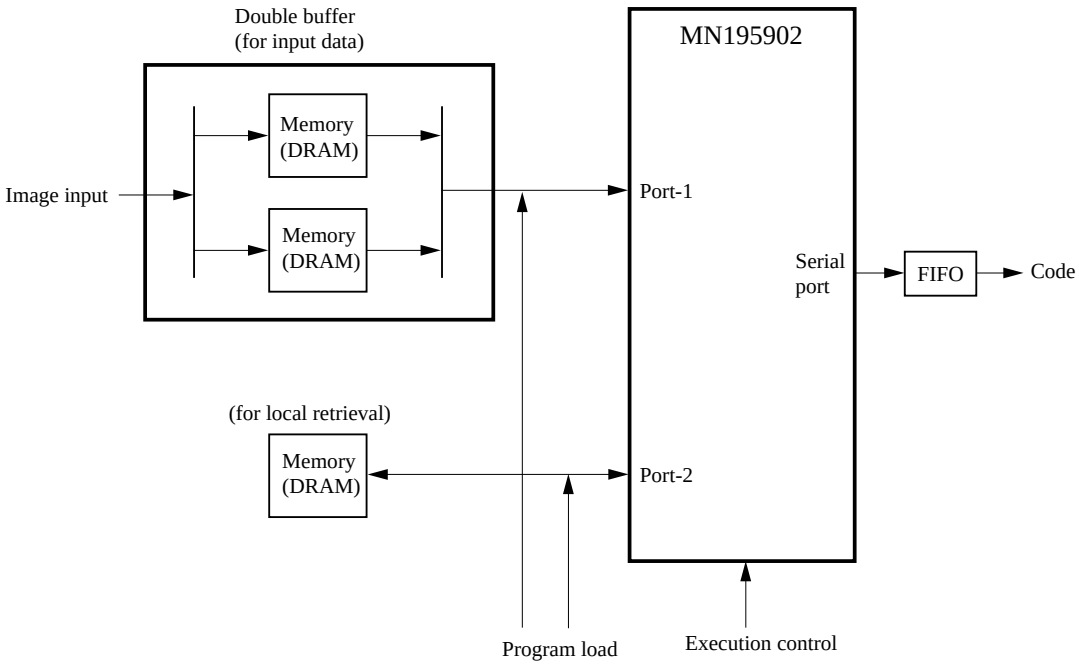


SAG	Two-dimensional address generator	MPY	Multiplier
BM1	Internal memory (1024 × 16 bits)	ACC	Accumulator
BM2	Instruction memory (2048 × 16 bits)	DCT	Discrete cosine transform converter
DM	Instruction memory (2048 × 16 bits)	FLT	Filter
IRAM, IROM	Instruction memory (2048 × 32 bits)	SIO	Serial interface
FREG0 to 15	General-purpose registers	PIO	Parallel interface
EALU	Arithmetic unit		

■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
15 to 24, 27 to 32	D1 (15:0)	I/O/Z	Data bus for data transfers to and from external memory (EM1)
47 to 48, 51 to 60	A1 (11:0)	I/O/Z	Address bus for data transfers to and from external memory (EM1)
71	XWE1	O/Z	External memory write control output (negative logic)
73	XOE1	O/Z	External memory read control output (negative logic)
77	XBO1	O	External memory cycle bus occupation control output (negative logic)
64	XRAS1	O/Z	External memory row address strobe output (negative logic)
66	XCAS1	O/Z	External memory row address strobe output (negative logic)
75	XRFSEN1	I	External memory refresh enable signal (negative logic)
123 to 128, 1, 2, 5 to 12	D2 (15:0)	I/O/Z	Data bus for data transfers to and from external memory (EM2)
33, 34, 37 to 46	A2 (11:0)	O/Z	Address bus for data transfers to and from external memory (EM2)
70	XWE2	O/Z	External memory write control output (negative logic)
72	XOE2	O/Z	External memory read control output (negative logic)
76	XBO2	O	External memory cycle bus occupation control output (negative logic)
63	XRAS2	O/Z	External memory row address strobe output (negative logic)
65	XCAS2	O/Z	External memory row address strobe output (negative logic)
74	XRFSEN2	I	External memory refresh enable signal (negative logic)
79	SCLK	I	System clock input
96	SPCLK	I	Serial port clock input
85	XHLD/RUN	I	Operational mode transition control input
83	XCS	I	Chip select input (negative logic)
82	XSWE	I	Internal memory write enable input for Hold/Slave mode (negative input)
88	XSRE	I	Internal memory read enable input for Hold/Slave mode (negative input)
84	XRST	I	Reset input (negative input)
87	ST1	O	Operating status output
86	ST2	O	Operating status output
102	SO	O/Z	Serial out port data
101	SOWCLK	O/Z	Serial out port external write enable output
100	XSOBSY	I	Serial out port external busy input (negative logic)
99	SI	I	Serial in port data
98	SIRCLK	O/Z	Serial in port external read enable output
97	XSIEMP	I	Serial in port external external empty input (negative logic)
105 to 112	PO (7:0)	O	Parallel out port data bus (PO7 is MSB)
113 to 120	PI (7:0)	I	Parallel in port data bus (PI7 is MSB)
81, 92, 93	DRMODE(2:0)	I	External DRAM mode control inputs
	V_{dd}	I	Power supply pin 3.3[V]
	V_{ddh}	I	Power supply pin 5.0 to V_{dd}[V]
	V_{ss}	I	Power supply pin 0 [V]

■ Application Circuit Example



■ Package Dimensions (Unit: mm)

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