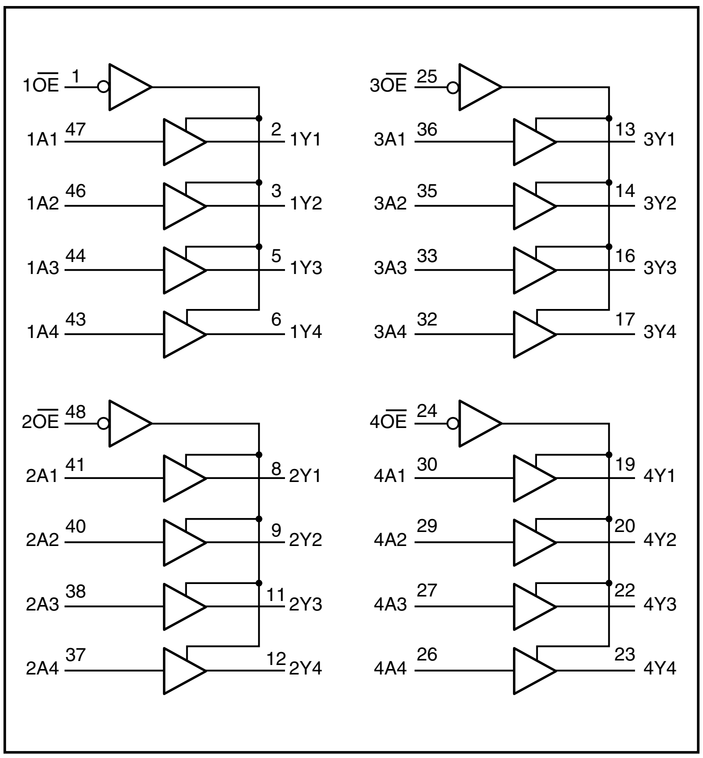
PI74LVTCH16244

3.3V 16-Bit Buffer/Line Driver with 3-State Outputs

Product Features

- Advanced low power CMOS design for 2.7V to 3.6V Vcc operation
- Supports 5V input/output tolerance in mixed signal mode operation
- Function compatible with LVT family of products
- Balanced ±24mA output drive
- Typical V_{OGB} (Output Ground Bounce) <0.8V at V_{CC}=3.3V, T_A=25°C
- I_{off} and Power Up/Down 3-State support live insertion
- Bus Hold on data inputs eliminates the need for external pull-up/down resistors
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD 22
  – 2000V Human-Body Model (A114-B)
  – 200V Machine Model (A115-A)
- Industrial Temperature: –40°C to +85°C
- Available Packages (Pb-free & Green available):
  – 48-pin 240-mil wide plastic TSSOP (A)

Logic Block Diagram



Product Description

The PI74LVTCH16244 is a non-inverting 16-bit buffer and line driver designed for low-voltage 2.7V to 3.6V V_{CC} operation, with the capability of interfacing to the 5V system environment. This buffer/ driver is designed specifically to improve both the performance and density of 3-State memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

The PI74LVTCH16244 has "Bus Hold" which retains the data input's last valid logic state whenever the data input goes to high-impedance, preventing "floating" inputs and eliminating the need for pull-up/down resistors.

When Vcc is between 0 to 1.5V during power up or power down, the device is in the high-impedance state. To ensure the high-impedance state above 1.5V, $\overline{OE}$ should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The device fully supports live-insertion with its I_{off} and power-up/ down 3-state. The I_{off} circuitry disables the outputs when the power is off, preventing the backflow of damaging current through the device. Power-up/down 3-state places the outputs in the high-impedance state during power up or power down, preventing driver conflict.

Maximum Ratings

(Above which the useful life may be impaired.
For user guidelines, not tested.)

Supply voltage range, V_{CC}	–0.5V to +6.5V
Input voltage range, V_I(1)	–0.5V to +6.5V
Voltage range applied to any output in the high-impedance or power-off state, V_O(1)	–0.5V to +6.5V
Voltage range applied to any output in the active state, V_O(1,2)	–0.5V to V_{CC}+0.5V
Input clamp current, I_{IK} (V_I<0)	–50mA
Output clamp current, I_{OK} (V_O<0)	–50mA
Continous Output Current I_O	±50mA
Continous Current through each VCC or GND pin	±100mA
Package thermal impedance, θ_{JA}(3)	104°C/W
Storage Temperature range, T_{stg}	–65°C to 150°C

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. Input negative-voltage and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 6.5V maximum.
3. The package thermal impedance is calculated in accordance with JESD51.

Truth Table(1)

Inputs		Outputs
x$\overline{OE}$	xAx	xYx
L	H	H
L	L	L
H	X	Z

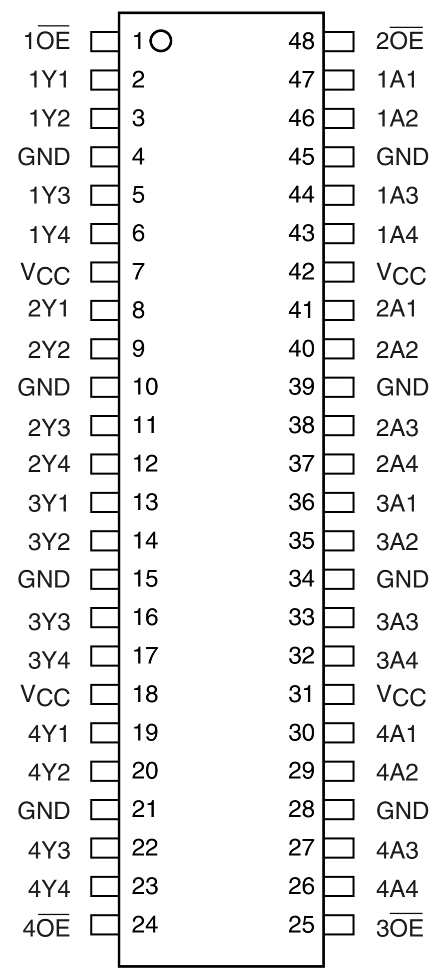
Notes:

1. H = High Signal Level
   L = Low Signal Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Product Pin Description

Pin Name	Description
x$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
V_{CC}	Power

Product Pin Configuration



Recommended Operating Conditions(1)

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	2.7	3.6	V
V_{IH} High-level Input Voltage	V_{CC} = 2.7V to 3.6V	2.0		
V_{IL} Low-level Input Voltage	V_{CC} = 2.7V to 3.6V		0.8	
V_I Input Voltage		0	5.5	
V_O Output Voltage	High or Low State	0	V_{CC}	
	3-State	0	5.5	
I_{OH} High-level output current	V_{CC} = 2.7V		–12	
	V_{CC} = 3.0V to 3.6V		–24	mA
I_OL Low-level output current	V_{CC} = 2.7V		12	
	V_{CC} = 3.0V to 3.6V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate			10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate		150		µs/V
T_A Operating free-air temperature		–40	85	°C

Notes:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C +85°C)

Parameters	Description		Test Conditions		Min.	Max.	Units
V_{IK}	Clamp Diode Voltage		V_{CC} = 2.7V	I_I = –18mA		–1.2V	V
V_{OH}	Output High Voltage		V_{CC} = 2.7V to 3.6V	I_{OH} = –100µA	V_{CC} –0.2V		
			V_{CC} = 2.7V	I_{OH} = –12mA	2.2		
			V_{CC} = 3V	I_{OH} = –12mA	2.4		
				I_{OH} = –24mA	2.2		
V_{OL}	Output Low Voltage		V_{CC} = 2.7V to 3.6V	I_{OL} = 100µA		0.2	
			V_{CC} = 2.7V	I_{OL} = 12mA		0.4	
			V_{CC} = 3V	I_{OL} = 12mA		0.4	
				I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	Control Inputs	V_{CC} = 0V to 3.6V	V_I = 0V to5.5V		±5	µA
		Data Inputs	V_{CC} = 3.6V	V_I = 5.5V		±5	
				V_I = V_{CC}			
				V_I = GND			
$I_{I(HOLD)}$	Data Input Hold Current		V_{CC} = 3V	V_I = 0.8V	75		
				V_I = 2V	–75		
			V_{CC} = 3.6V(1)	V_I = 0 to 3.6V		±500	
I_{OFF}	Power Off Output Leakage Current		V_{CC} = 0V	V_I or V_O = 0V to 5.5V		±5	
I_{OZ}	3-State Output Leakage Current		V_{CC} = 2.7V to 3.6V	V_O = 0V to 5.5V		±5	
I_{OZPU}	Power-Up 3-State Current		V_{CC} = 0V to 1.5V	V_O = 0.5V to 5.5V, $\overline{OE}$ = don't care		±5	
I_{OZPD}	Power-Down 3-State Current		V_{CC} = 1.5V to 0V	V_O = 0.5V to 5.5V, $\overline{OE}$ = don't care		±5	
I_{CC}	Quiescent Power Supply Current		V_{CC} = 2.7V to 3.6V	V_I = V_{CC} or GND; I_O = 0		100	
				3.6V ≤ V_I ≤ 5.5V; I_O = 0			
ΔI_{CC}	Increase in I_{CC}		V_{CC} = 3V to 3.6V	One input at V_{CC} - 0.6V(2) Other inputs at V_{CC} or GND		200	

Notes:

1. This is the maximum bus-hold dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

Parameters	Description	Test Conditions	Typ.(1)	Units
C_I	Input Capacitance	V_{CC} = 3.3V, V_I = V_{CC} or GND	3.7	pF
C_O	Output Capacitance	V_{CC} = 3.3V, V_O = V_{CC} or GND	7	
C_{PD}	Power Dissipation Capacitance (2)	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f =10 MHz	16	

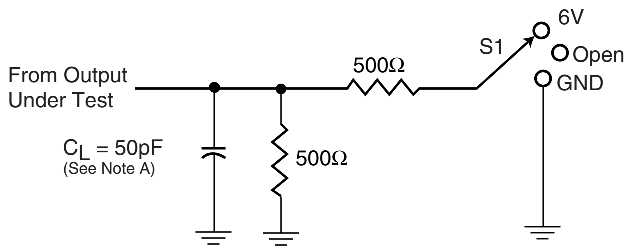
Notes:
1. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle, C_{PD} is related to I_{CCD} dynamic operating current by the expression:
   I_{CCD}= (C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)

Switching Characteristics Over Operating Range

Parameters	Description	From (Input)	To (Output)	V_{CC} = 3.3V ±0.3V, C_L = 50pF, R_L = 500-ohm			V_{CC} = 2.7V, C_L = 50pF, R_L = 500-ohm		Units
				Min.	Typ.(1)	Max.	Min.	Max.	
t_{PLH}	Propagation Delay	A	Y	1.0	2.5	3.4		3.8	ns
t_{PHL}				1.0	2.5	3.4		3.8	
t_{PZH}	Output Enable Time	$\overline{OE}$	Y	1.0	2.9	4.2		5.0	
t_{PZL}				1.0	3.0	4.2		5.0	
t_{PHZ}	Output Disable Time	$\overline{OE}$	Y	1.0	2.5	4.0		4.7	
t_{PLZ}				1.0	2.4	3.9		4.3	
$t_{SK(O)}$	Output to Output Skew(2)					0.5			

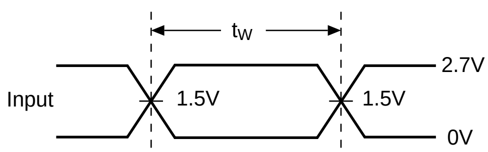
Notes:
1. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C
2. Skew between any two outputs, switching in the same direction.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7V and 3.3V ±0.3V

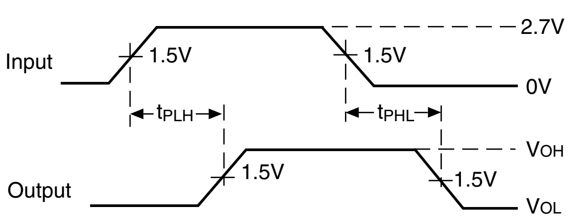


Load Circuit

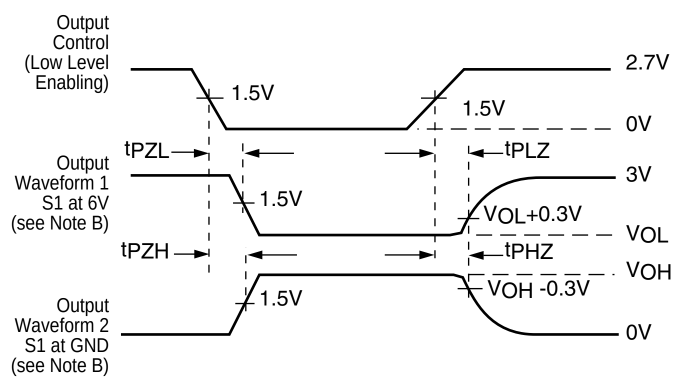
Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

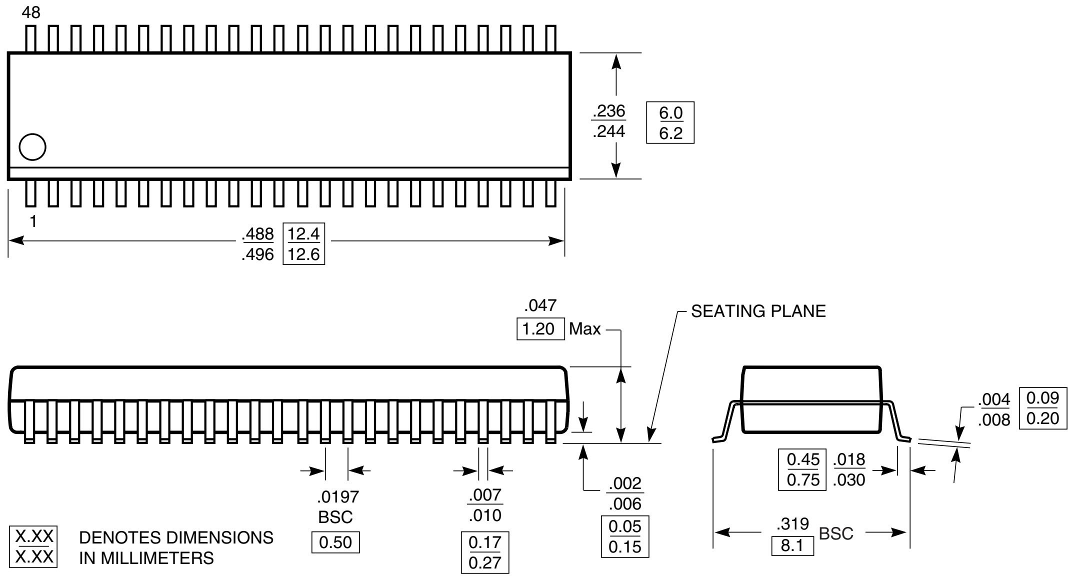
Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_O = 50W, t_R £ 2.5ns, t_F £ 2.5ns.
- The outputs are measured one at a time with one transition per measurement.

Packaging Mechanical: 48-pin TSSOP (A)



Ordering Information

Ordering Code	Package Code	Package Description
PI74LVTCH16244A	A	48-pin, 240-mil wide plastic TSSOP
PI74LVTCH16244AE	A	Pb-free, 48-pin, 240-mil wide plastic TSSOP

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel