

# DATA SHEET

## **74LVC16240A**

**16-bit buffer/line driver; inverting (3-State)**

Product specification  
Supersedes data of 1995 Dec 26  
IC24 Data Handbook

1997 Jul 29

## 16-bit buffer/line driver; inverting (3-State)

74LVC16240A

## FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels

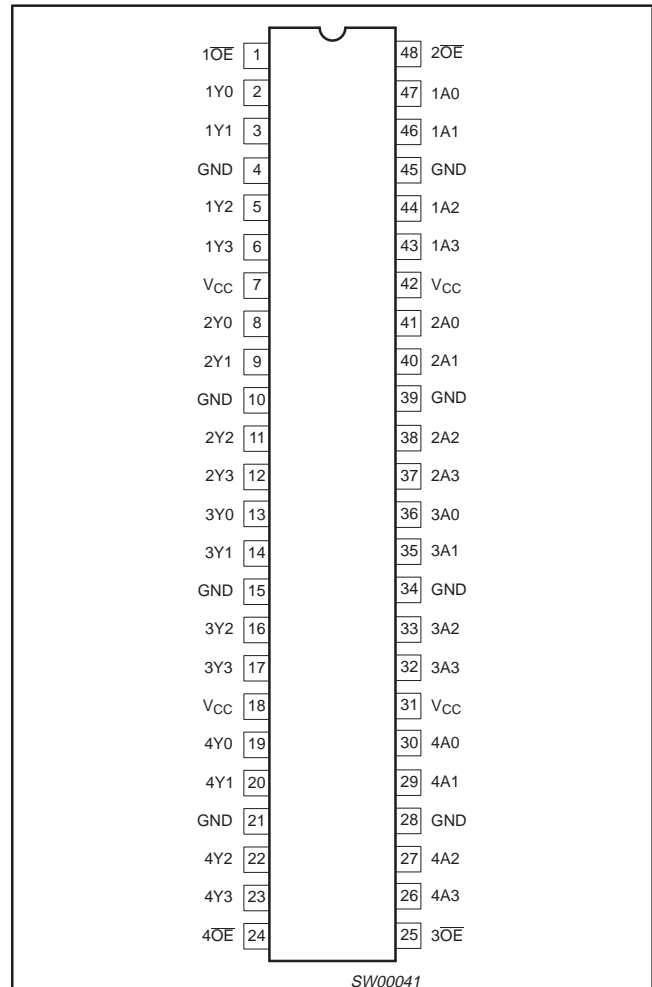
## DESCRIPTION

The 74LVC16240A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC16240A is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The 74LVC16240A is identical to the 74LVC16244A but has inverting outputs.

## PIN CONFIGURATION



## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay 1An to 1Yn; 2An to 2Yn	C <sub>L</sub> = 50pF V <sub>CC</sub> = 3.3V	2.7	ns
C <sub>I</sub>	Input capacitance		5.0	pF
C <sub>PD</sub>	Power dissipation capacitance per buffer	V <sub>CC</sub> = 3.3V	25	pF

## NOTES:

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF;

f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVC16240A DL	VC16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVC16240A DGG	VC16240A DGG	SOT362-1

# 16-bit buffer/line driver; inverting (3-State)

# 74LVC16240A

## PIN DESCRIPTION

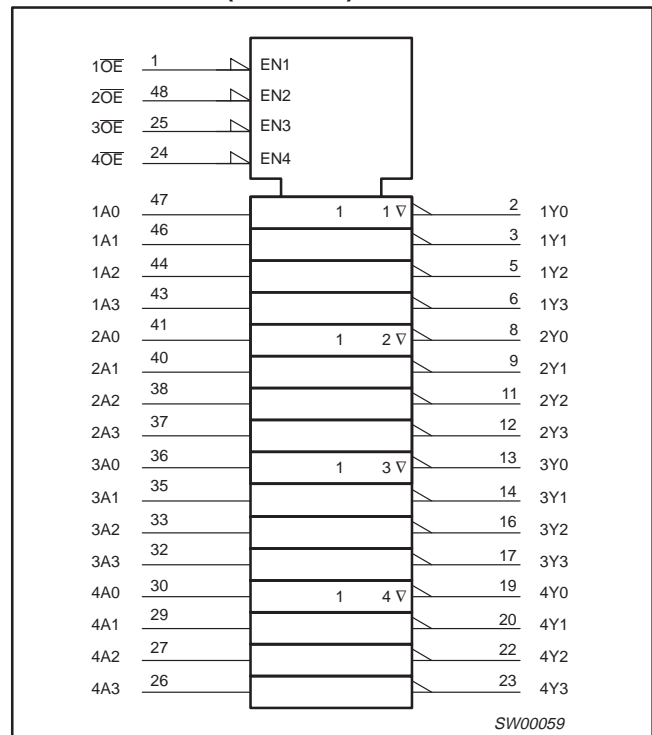
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	4OE	Output enable input (active LOW)
25	3OE	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	2OE	Output enable input (active LOW)

## FUNCTION TABLE

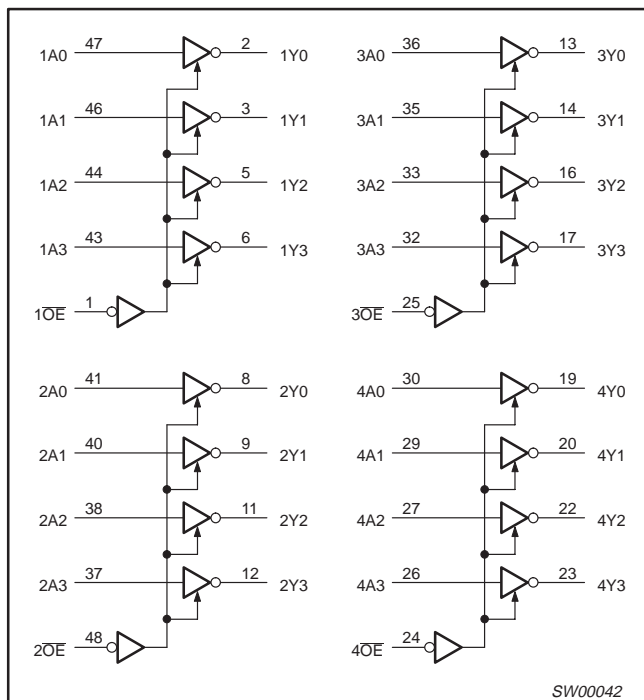
INPUTS		OUTPUT
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

## LOGIC SYMBOL (IEEE/IEC)



## LOGIC SYMBOL



## 16-bit buffer/line driver; inverting (3-State)

74LVC16240A

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
$V_{CC}$	DC supply voltage (for low-voltage applications)		1.2	3.6	V
$V_I$	DC Input voltage range		0	5.5	V
$V_O$	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
$V_O$	DC output voltage range; output 3-State		0	5.5	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage		-0.5	+6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-	-50	mA
$V_I$	DC input voltage	Note 2	-0.5	+6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	-0.5	$V_{CC} + 0.5$	V
$V_O$	DC output voltage; output 3-State	Note 2	-0.5	6.5	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	-	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	Storage temperature range		-65	+150	°C
$P_{tot}$	Power dissipation per package - SO package - SSOP and TSSOP package	Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K		500 500	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 16-bit buffer/line driver; inverting (3-State)

74LVC16240A

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100µA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		GND	0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		± 0.1	± 5	µA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	± 5	µA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	± 10	µA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	20	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	µA

**NOTES:**1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.**AC CHARACTERISTICS**GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V <sub>CC</sub> = 3.3V ± 0.3V			V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 1.2V	
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	TYP	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation delay 1An to 1Yn; 2An to 2Yn	1, 3	1.5	2.8	4.7	1.5	5.7	12	ns
t <sub>PZH</sub> t <sub>PZL</sub>	3-State output enable time 1OE to 1Yn; 2OE to 2Yn	2, 3	1.5	3.5	5.4	1.5	6.4	18	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	3-State output disable time 1OE to 1Yn; 2OE to 2Yn	2, 3	1.5	3.9	5.1	1.5	6.1	11	ns

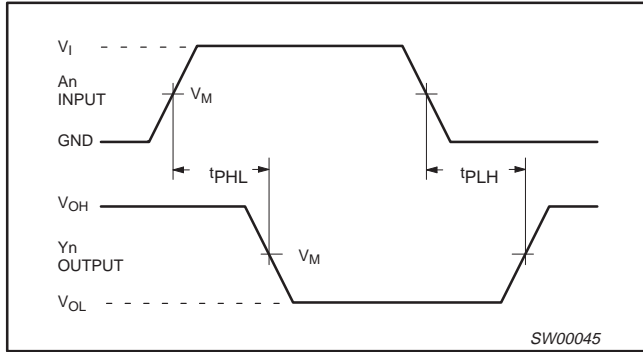
**NOTE:**1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

# 16-bit buffer/line driver; inverting (3-State)

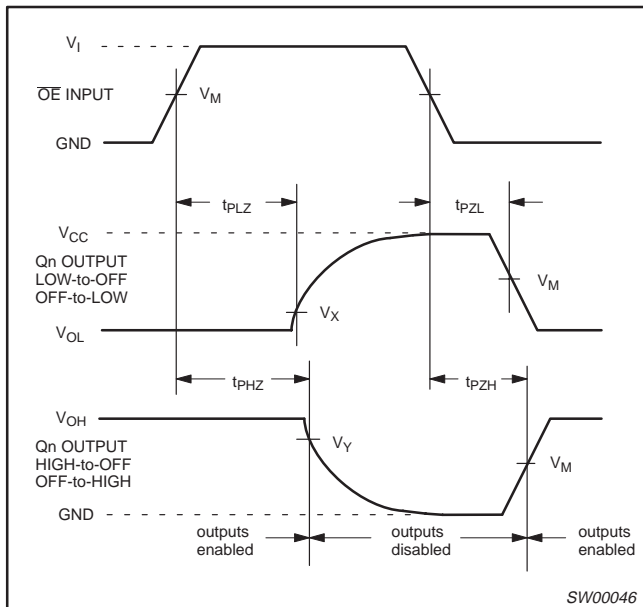
# 74LVC16240A

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7V$



Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

## TEST CIRCUIT

**Test Circuit for 3-State Outputs**

SWITCH POSITION	
TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 * V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_{IN}$
$< 2.7V$	$V_{CC}$
$2.7 - 3.6V$	$2.7V$

**DEFINITIONS**  
 $R_L$  = Load resistor  
 $C_L$  = Load capacitance includes jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

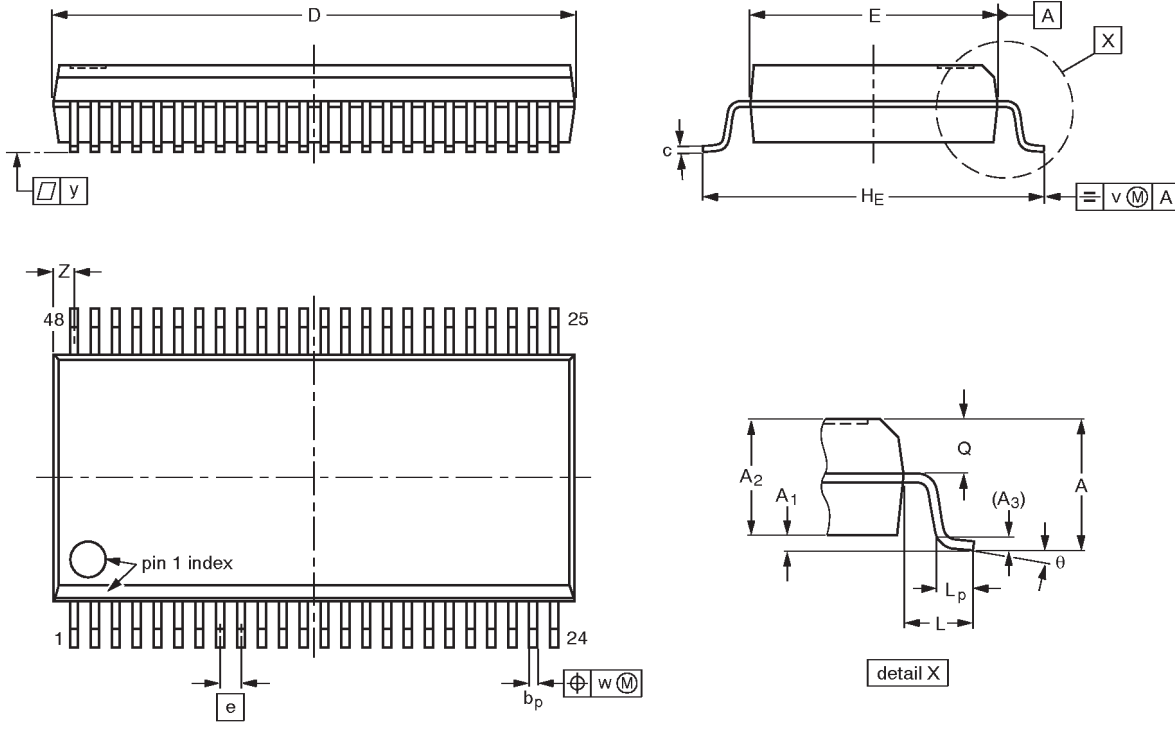
Waveform 3. Load circuitry for switching times

16-bit buffer/line driver; inverting (3-State)

74LVC16240A

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

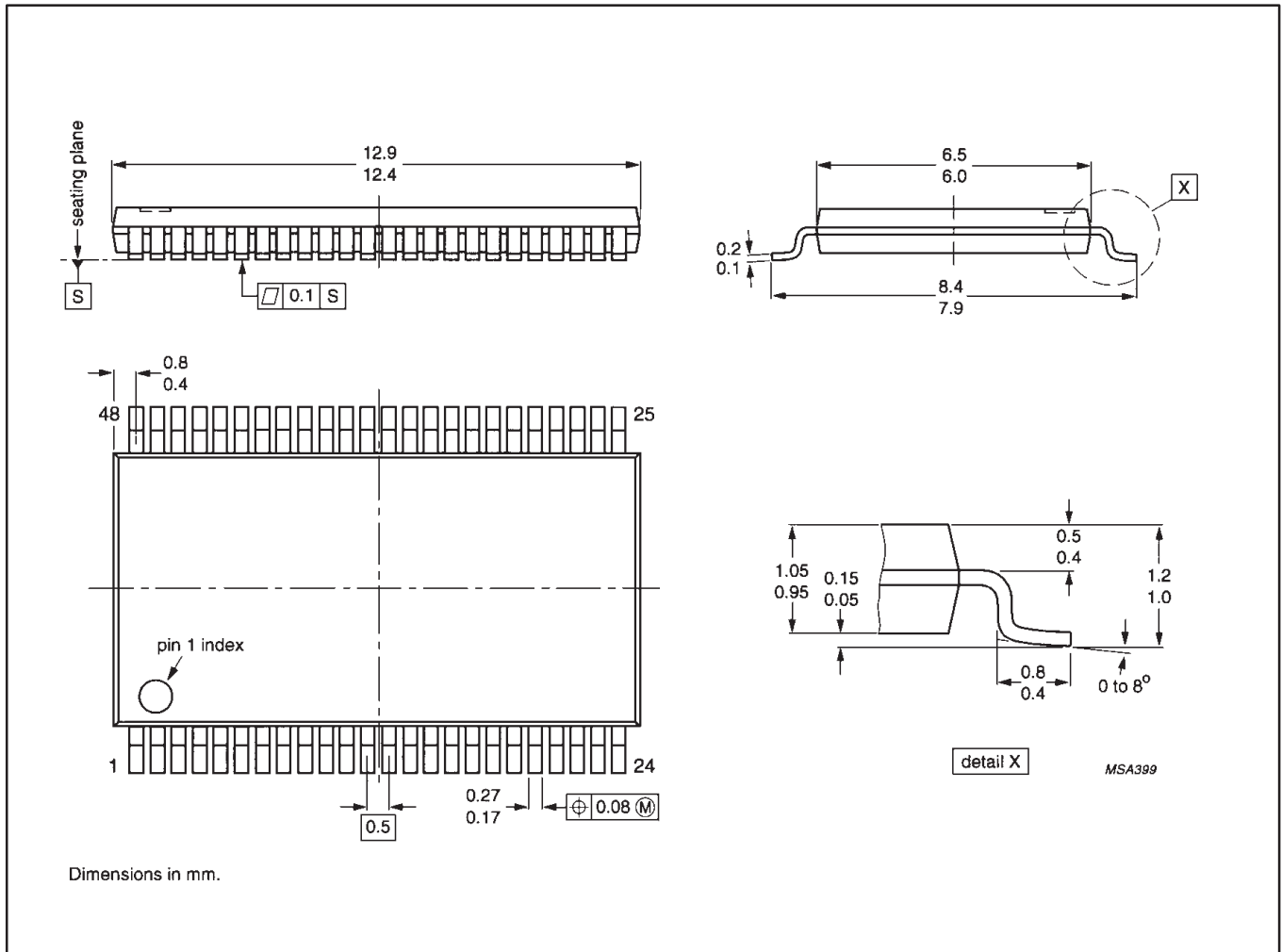
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

# 16-bit buffer/line driver; inverting (3-State)

# 74LVC16240A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1





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16-bit buffer/line driver; inverting (3-State)

74LVC16240A

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**NOTES**

## 16-bit buffer/line driver; inverting (3-State)

74LVC16240A

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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