Description

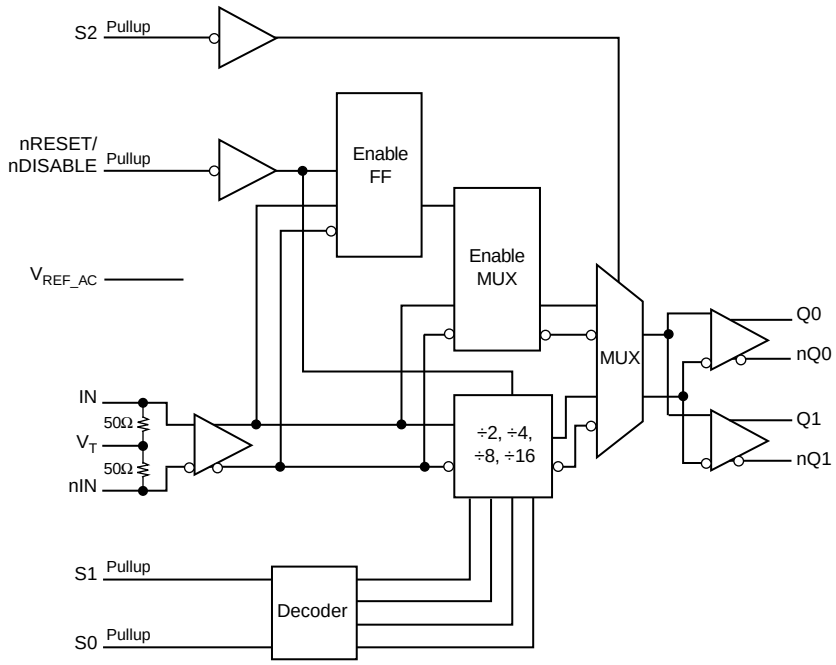
The 8S89876I is a high speed Differential-to-LVDS Buffer/Divider w/Internal Termination. The 8S89876I has a selectable ÷1, ÷2, ÷4, ÷8, ÷16 output divider. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components.

The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

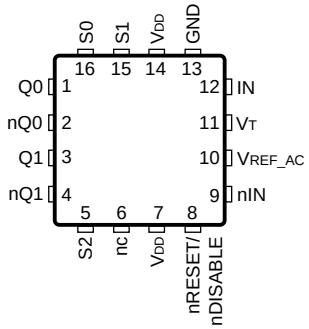
Features

- Two LVDS outputs
- Frequency divide select options: ÷1, ÷2, ÷4, ÷8, ÷16
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Input Frequency: 2.5GHz (maximum)
- Additive phase jitter, RMS: 0.07ps (typical)
- Output skew: 25ps (maximum)
- Part-to-part skew: 280ps (maximum)
- Propagation Delay: 1.1ns (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- Pin compatible with the obsolete device 889876AK

Block Diagram



Pin Assignment



8S89876I

16-Lead VFQFN
3mm x 3mm x 0.9mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. Divide by 1, 2, 4, 8, or 16. Unused output pairs must be terminated with 100Ω across the differential pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. Divide by 1, 2, 4, 8, or 16. Unused output pairs must be terminated with 100Ω across the differential pair. LVDS interface levels.
5, 15, 16	S2, S1, S0	Input	Pullup	Select pins. Internal 25kΩ pullup resistor. Logic HIGH if left disconnected (÷16 mode). Input threshold is V_{DD}/2. LVCMOS/LVTTL interface levels.
6	nc	Unused		No connect.
7, 14	V_{DD}	Power		Power supply pins.
8	nRESET/ nDISABLE	Input	Pullup	When LOW, resets the divider (÷2, ÷4, ÷8 or ÷16 mode). When HIGH, outputs are active. LVTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. R_T = 50Ω termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. Equal to V_{DD} – 1.35V (approx.). Maximum sink/source current is 2mA.
11	V_T	Input		Termination center-tap input. Leave pin floating.
12	IN	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to V_T.
13	GND	Power		Power supply ground.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37.5		kΩ

Function Tables

Table 3A. Control Input Function Table

Input	Outputs	
nRESET/nDISABLE	**Q0, Q1**	**nQ0, nQ1**
0	Disabled; LOW	Disabled; HIGH
1(default)	Enabled	Enabled

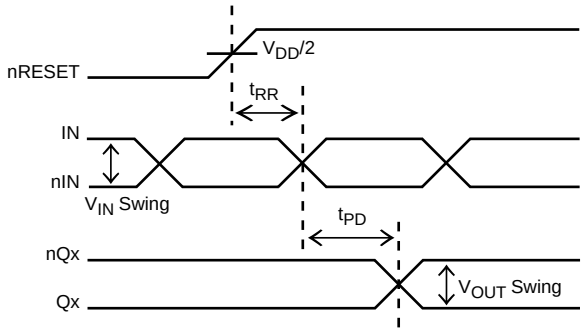


Figure 1. nRESET Timing Diagram

Table 3B. Truth Table

Inputs				Outputs
nRESET/nDISABLE	**S2**	**S1**	**S0**	**Q0, nQ0, Q1, nQ1**
1	0	X	X	Reference Clock (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16 (default)
0	X	X	X	Qx = LOW, nQx = HIGH; Clock disabled

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_{OUT} (NOTE) Continuos Current Surge Current	 50mA 100mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: I_{OUT} refers to output current supplied by the IDT device only.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage			2.97	3.3	3.63	V
I_{DD}	Power Supply Current					72	mA
R_{IN}	Differential Input Resistance	(IN, nIN)		80	100	120	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{DD} - 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		1.8	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN}	Input Current; NOTE 2	(IN, nIN)				45	mA
V_{REF_AC}	Bias Voltage			V_{DD} - 1.45	V_{DD} – 1.35	V_{DD} - 1.25	V

NOTE 1: Refer to Parameter Measurement Information, Input Voltage Swing Diagram
NOTE 2: Guaranteed by design.

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.63V	-125		20	µA
I_{IL}	Input Low Current	V_{DD} = 3.63V, V_{IN} = 0V			-300	µA

Table 4C. LVDS DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OUT}	Output Voltage Swing		247		454	mV
V_{OH}	Output High Voltage		1.35		1.85	V
V_{OL}	Output Low Voltage		1.1		1.5	V
V_{OCM}	Output Common Mode Voltage		1.205		1.475	V
ΔV_{OCM}	Change in Common Mode Voltage				50	mV

AC Electrical Characteristics

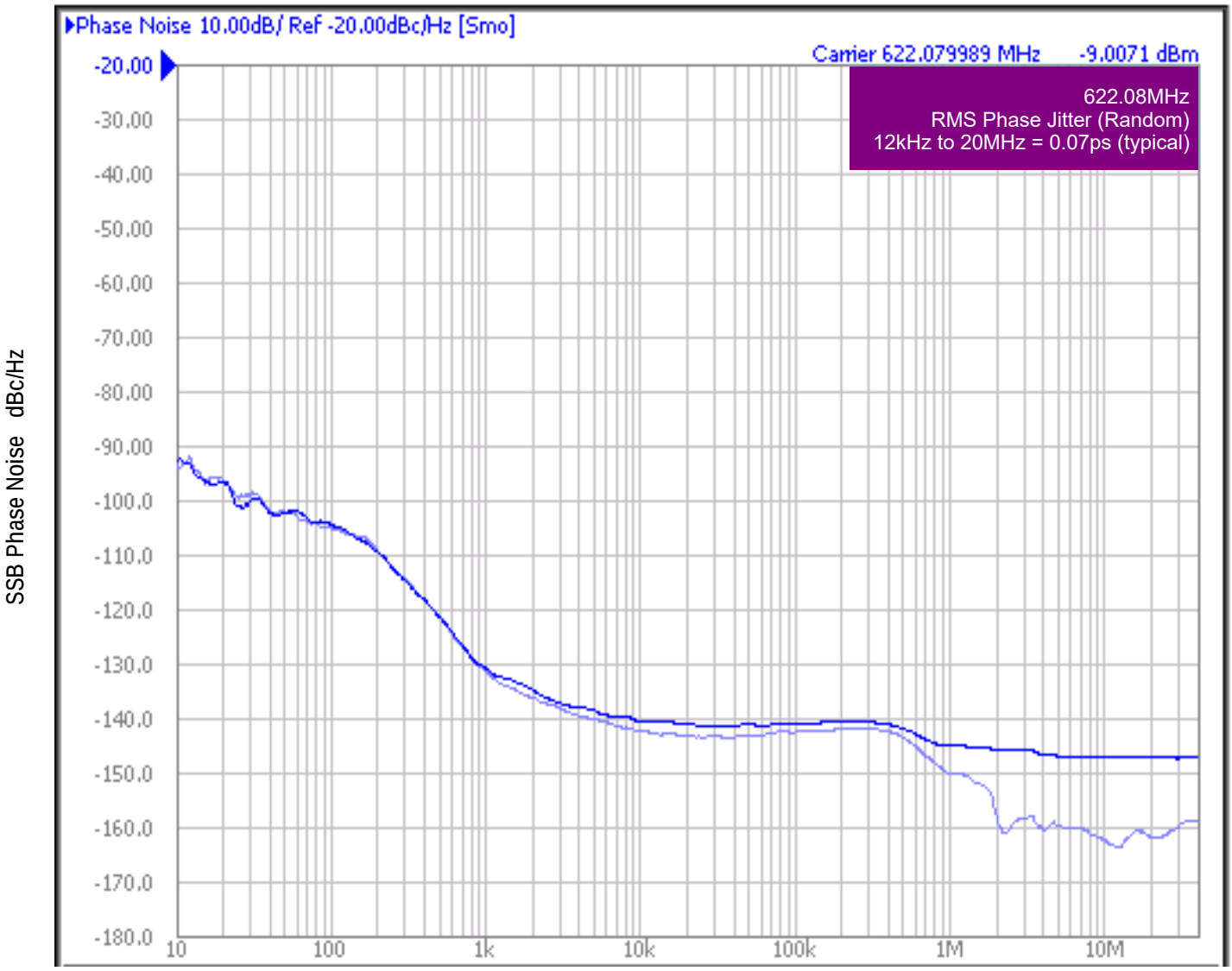
Table 5. AC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency					2.5	GHz
t_{PD}	Propagation Delay; NOTE 1	IN-to-Q		0.46		1.1	ns
*t*sk(o)	Output Skew; NOTE 2, 3					25	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					280	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		622.08MHz, Integration Range: 12kHz - 20MHz		0.07		ps
t_{RR}	Reset Recovery Time			600			ps
t_R / t_F	Output Rise/Fall Time			40	150	250	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters characterized at ≤ 1.7GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

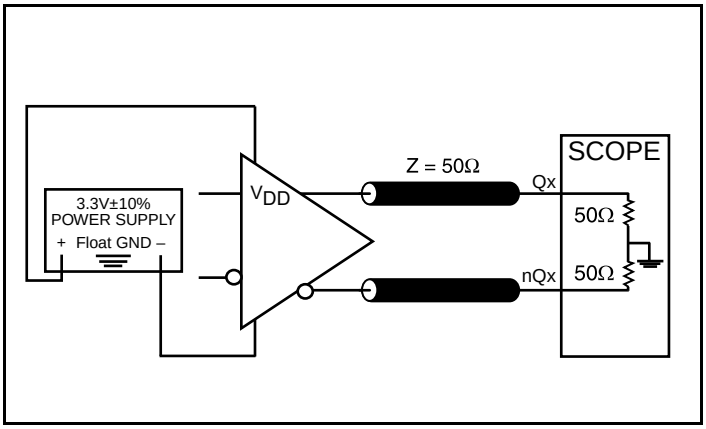
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



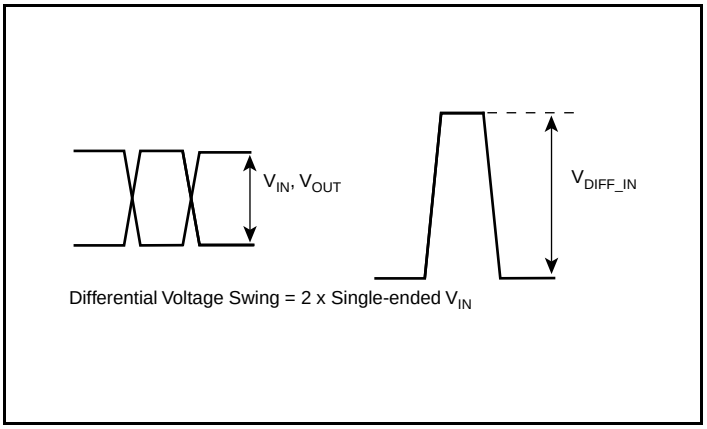
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “Rohde & Schwarz SMA 100A Signal Generator, 91Hz – 6GHz as external input with a balun was used to drive the input clock IN, nIN”.

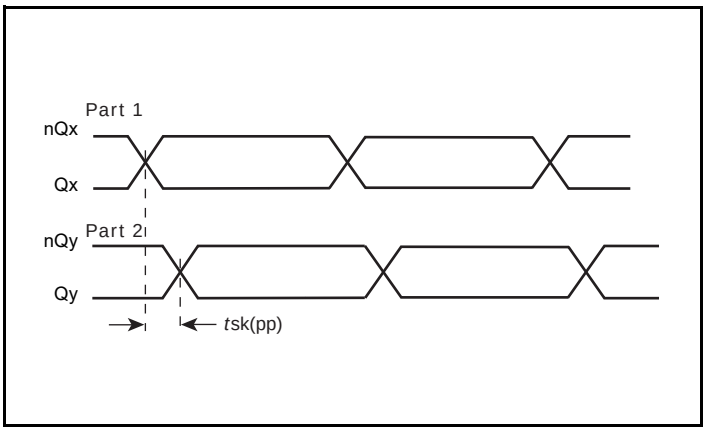
Parameter Measurement Information



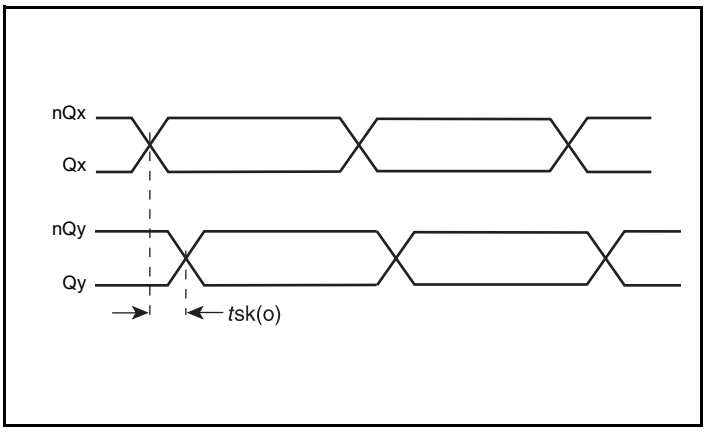
LVDS Output Load AC Test Circuit



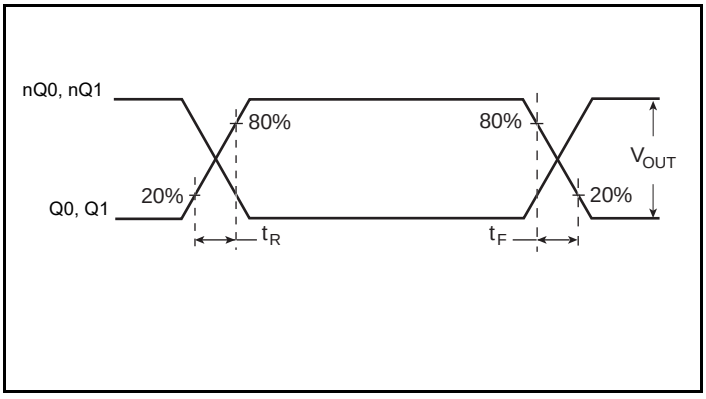
Single-Ended & Differential Input/Output Voltage Swing



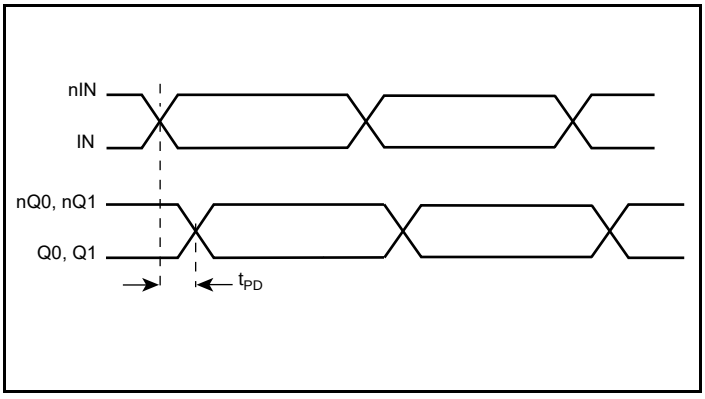
Part-to-Part Skew



Output Skew

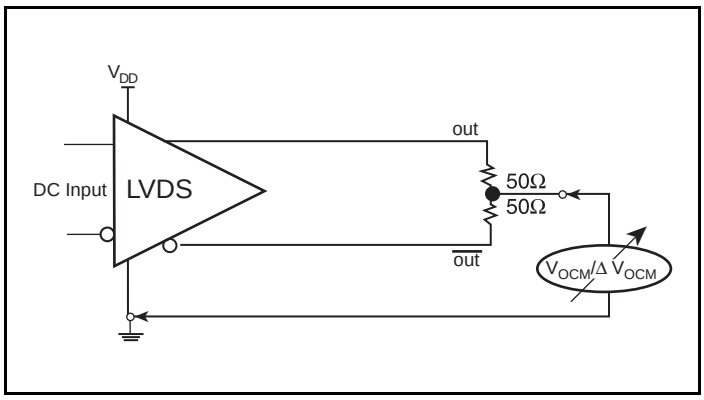


Output Rise/Fall Time

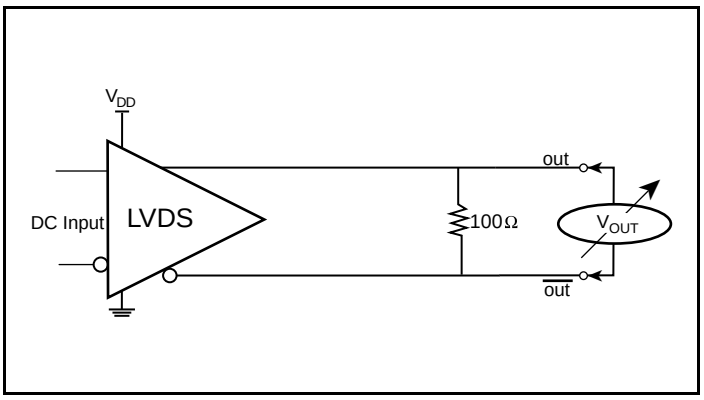


Propagation Delay

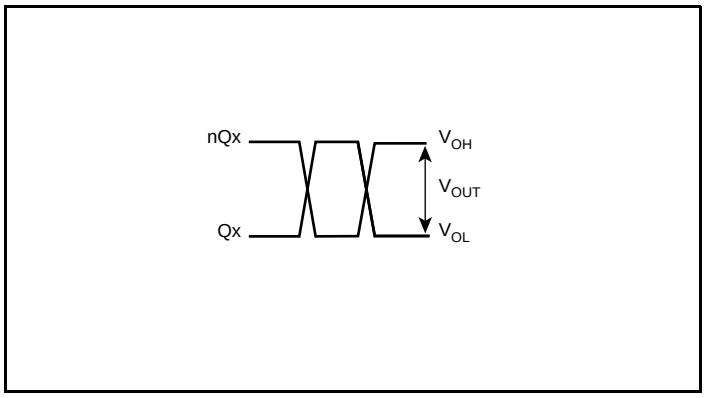
Parameter Measurement Information, continued



LVDS Output Common Mode Voltage



LVDS Output Voltage Swing



LVDS Output Voltage Level

Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML, and other differential signals. The differential signal must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

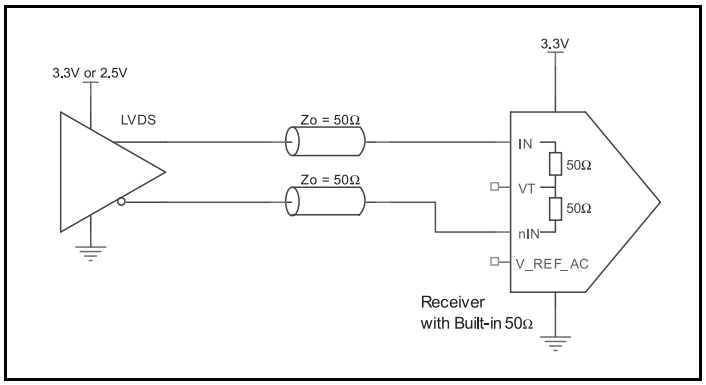


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

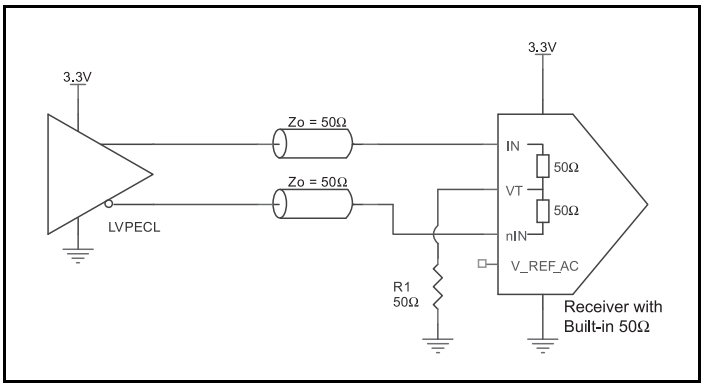


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

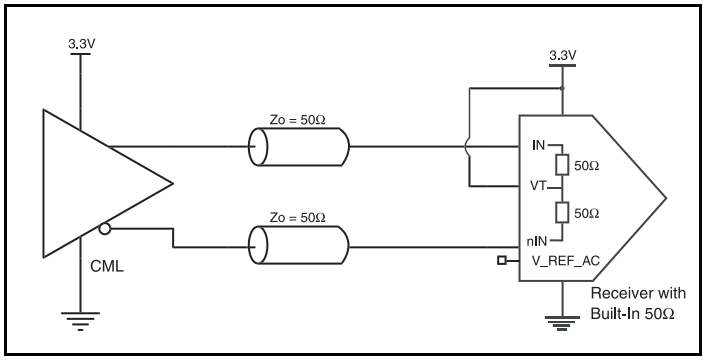


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

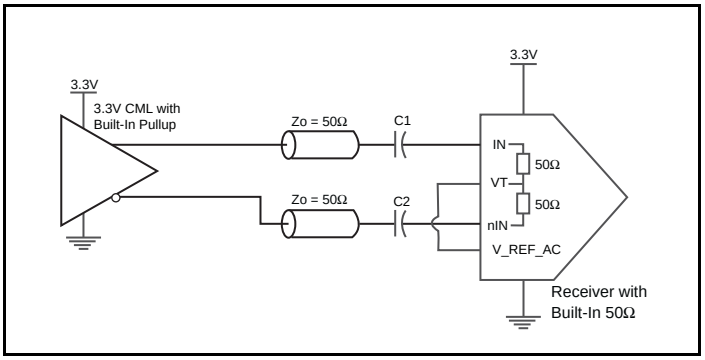


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 3 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

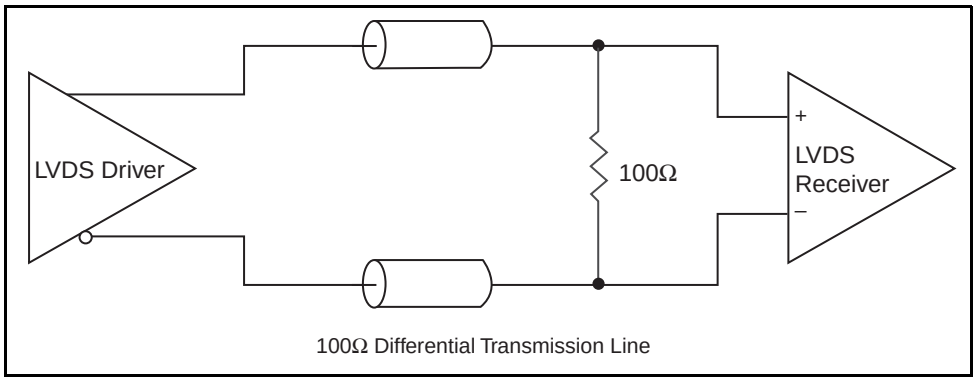


Figure 3. Typical LVDS Driver Termination

Recommendations for Unused Input Pins

Inputs:

LVCMOS Select Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

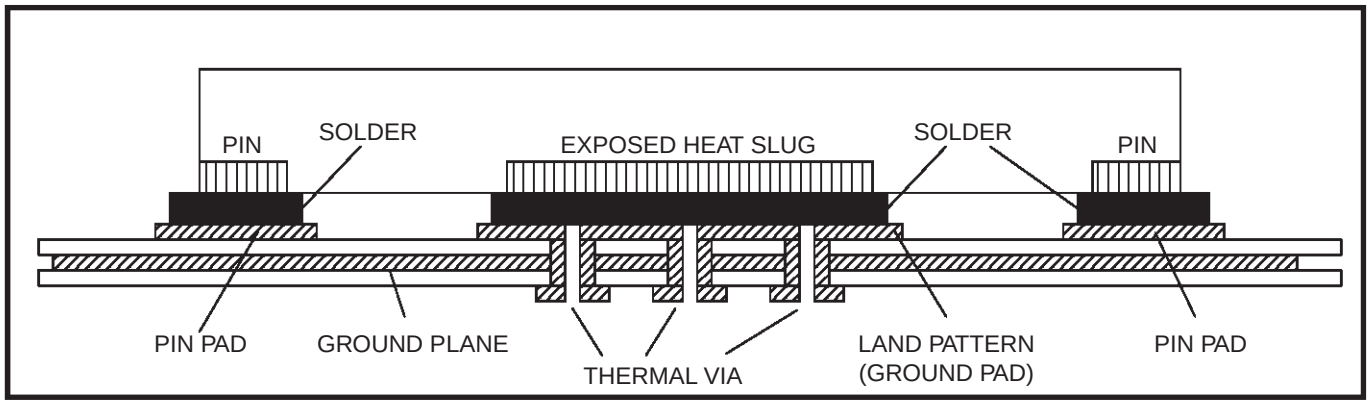


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89876I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89876I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.63V * 72mA = **261.4mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = (V_{IN\_MAX})^2 / R_{IN\_MIN} = (1.2V)^2 / 80\Omega$ = **18mW**

Total Power$_{MAX}$ (3.63V, with all outputs switching) = 261.4mW + 18mW + 18mW = 2**79.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.279W * 74.7°C/W = 105.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 8S89876I is: 504

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89876BKILF	876B	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
8S89876BKILFT	876B	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

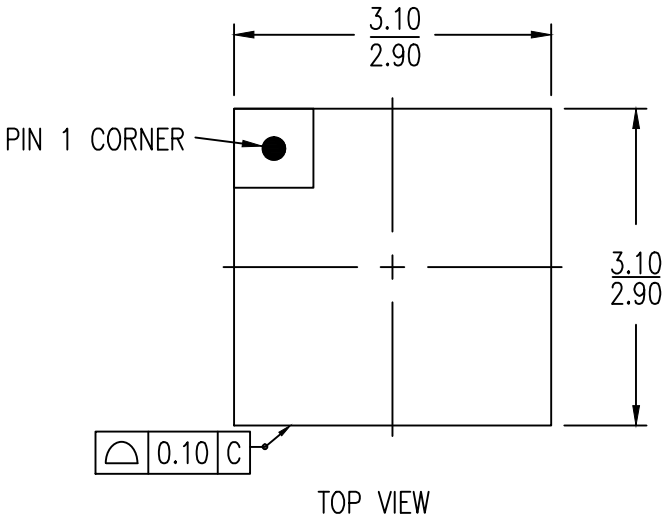
Revision History

Revision Date	Description of Change
January 11, 2018	▪ Updated the package outline drawings; however, no mechanical changes
February 9, 2016	▪ Removed ICS from part number where needed. ▪ Ordering Information - removed quantity from tape and reel. Removed LF note below table. ▪ Updated header and footer.

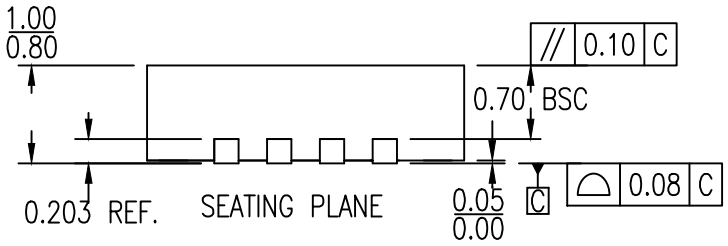
Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

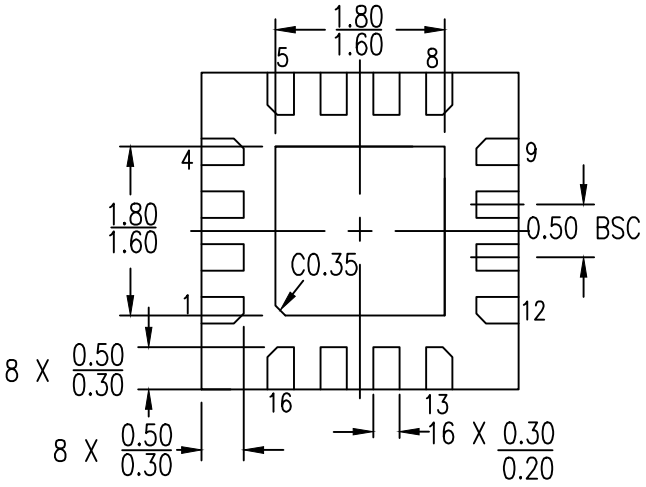
Tech Support
www.idt.com/go/support



TOP VIEW

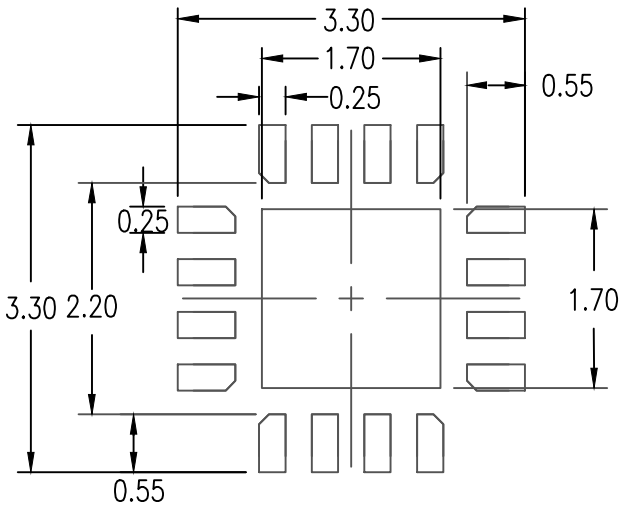


SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Aug 15, 2017	Rev 03	Update Epad Range