8-channel analog multiplexer/demultiplexer with injection-current effect control Rev. 4 — 15 May 2023 Pro

Product data sheet

1. General description

The 74HC4851; 74HCT4851 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7A.

The 74HC4851; 74HCT4851 are 8-channel analog multiplexers/demultiplexers with three digital select inputs (S0 to S2), an active-LOW enable input (\overline{E}), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The devices feature injection-current effect control, which has excellent value in automotive applications where voltages in excess of the supply voltage are common.

With \overline{E} LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With \overline{E} HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

2. Features and benefits

- Injection-current cross coupling < 1 mV/mA
- Wide supply voltage range from 2.0 V to 6.0 V for 74HC4851
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- Low ON-state resistance:
 - 400 Ω (typical) at V_{CC} = 2.0 V
 - 215 Ω (typical) at V_{CC} = 3.0 V
 - 120 Ω (typical) at V_{CC} = 3.3 V
 - 76 Ω (typical) at V_{CC} = 4.5 V
 - 59 Ω (typical) at V_{CC} = 6.0 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

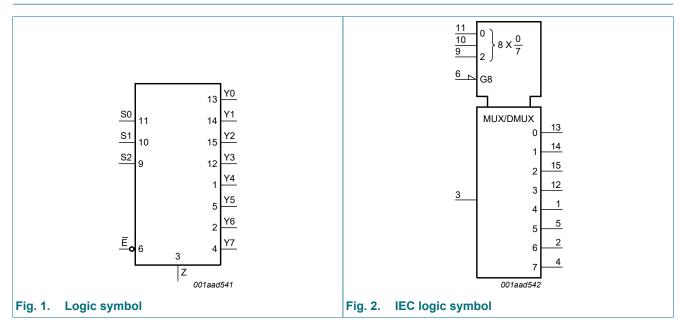
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
 - Signal gating



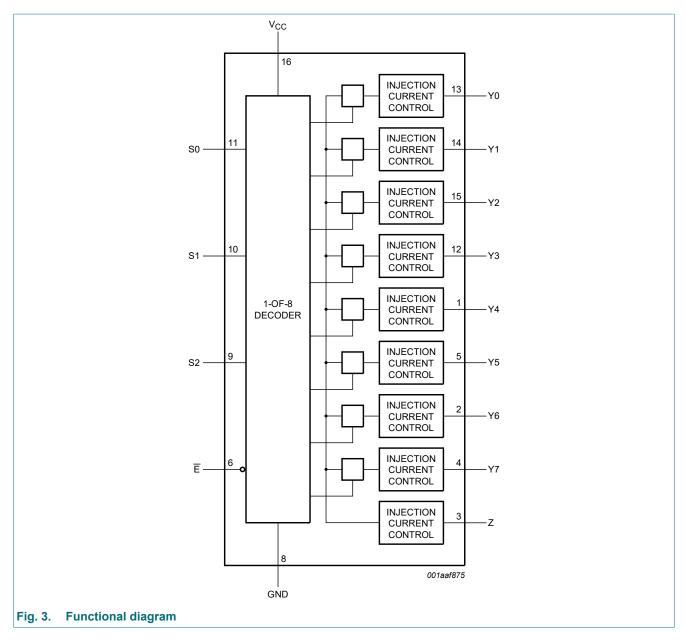
4. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<u>74HC4851D</u> 74HCT4851D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
<u>74HC4851PW</u> 74HCT4851PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
<u>74HC4851BQ</u> 74HCT4851BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	<u>SOT763-1</u>

5. Functional diagram

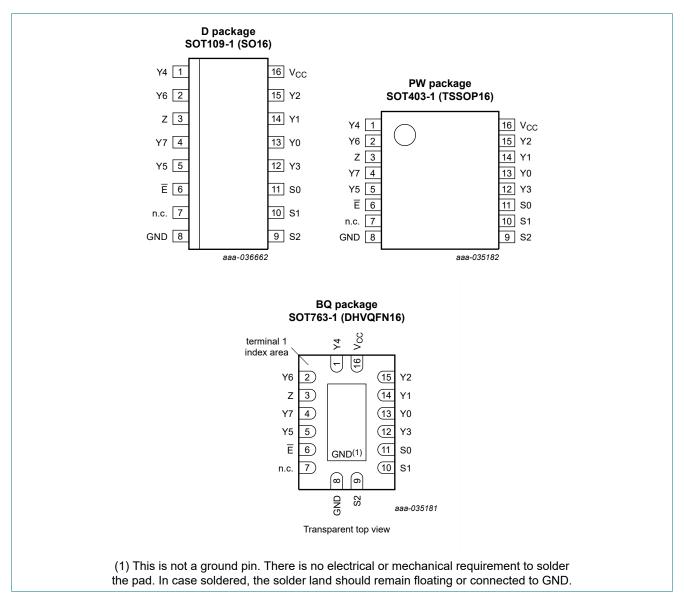


8-channel analog multiplexer/demultiplexer with injection-current effect control



6. Pinning information





6.2. Pin description

Symbol	Pin	Description
Y4, Y6, Y7, Y5, Y3, Y0, Y1, Y2	1, 2, 4, 5, 12, 13, 14, 15	independent input/output
Z	3	common input/output
E	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground (0 V)
S2, S1, S0	9, 10, 11	select input
V _{cc}	16	supply voltage

74HC_HCT4851

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7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Channel ON
E	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	Н	Y1 to Z
L	L	Н	L	Y2 to Z
L	L	Н	Н	Y3 to Z
L	Н	L	L	Y4 to Z
L	Н	L	Н	Y5 to Z
L	Н	Н	L	Y6 to Z
L	Н	Н	Н	Y7 to Z
Н	Х	Х	Х	-

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-0.5	V _{CC} + 0.5	V
V _{SW}	switch voltage	[2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	$V_{\rm I}$ < -0.5 V or $V_{\rm I}$ > $V_{\rm CC}$ + 0.5 V	-	±20	mA
I _{SK}	switch clamping current	V_{SW} < -0.5 V or V_{SW} > V_{CC} + 0.5 V	-	±20	mA
I _{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \ ^{\circ}C \ to +125 \ ^{\circ}C$ [3]	-	500	mW

[1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.

[2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.

[3] For SOT109-1 (SO16) package: Ptot derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C. For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

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9. Recommended operating conditions

Symbol	Parameter	Conditions	7	4HC485	51	74	4HCT48	51	Unit
			Min	Тур	Мах	Min	Тур	Max	
V _{CC}	supply voltage		2.0	-	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _{SW}	switch voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	6.0	1000	-	-	-	ns/V
		V _{CC} = 3.0 V	-	6.0	800	-	-	-	ns/V
		V _{CC} = 3.3 V	-	6.0	800	-	-	-	ns/V
		V _{CC} = 4.5 V	-	6.0	500	-	6.0	500	ns/V
1		V _{CC} = 6.0 V	-	6.0	400	-	-	-	ns/V

Table 5. Recommended operating conditions

10. Static characteristics

Table 6. R_{ON} resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Мах	Min	Max	Min	Max	
74HC485	51									
R _{ON(peak)}	ON resistance	$V_{I} = V_{CC}$ to GND; $\overline{E} = V_{IL}$								
	(peak)	V _{CC} = 2.0 V; I _{SW} = 2 mA	-	400	650	-	670	-	700	Ω
		V _{CC} = 3.0 V; I _{SW} ≤ 2 mA	-	215	330	-	360	-	380	Ω
		V _{CC} = 3.3 V; I _{SW} ≤ 2 mA	-	120	270	-	305	-	345	Ω
		V _{CC} = 4.5 V; I _{SW} ≤ 2 mA	-	76	210	-	240	-	270	Ω
		V _{CC} = 6.0 V; I _{SW} ≤ 2 mA	-	59	195	-	220	-	250	Ω
ΔR _{ON}	ON resistance	$V_{I} = 0.5 \times V_{CC}; \overline{E} = V_{IL}$								
	mismatch between	V _{CC} = 2.0 V; I _{SW} = 2 mA	-	4	10	-	15	-	20	Ω
	channels	V _{CC} = 3.0 V; I _{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V _{CC} = 3.3 V; I _{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V _{CC} = 4.5 V; I _{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V _{CC} = 6.0 V; I _{SW} ≤ 2 mA	-	3	9	-	13	-	18	Ω
74HCT48	351									
R _{ON(peak)}	ON resistance	$V_{I} = V_{CC}$ to GND; $\overline{E} = V_{IL}$								
	(peak)	V _{CC} = 4.5 V; I _{SW} ≤ 2 mA	-	76	210	-	240	-	270	Ω
ΔR _{ON}	ON resistance	$V_{I} = 0.5 \times V_{CC}; \overline{E} = V_{IL}$								
	mismatch between channels	V _{CC} = 4.5 V; I _{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω

Table 7. Injection current coupling

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see Fig. 7.

								•		
Symbol	Parameter	Conditions		1	74HC4851	1	7	4HCT485	1	Unit
				Min	Typ [1]	Max	Min	Typ [1]	Max	1
T _{amb} = -4	40 °C to +125 °C	;								-
ΔV _O	output voltage variation	I _{SW} ≤ 1 mA; R _S ≤ 3.9 kΩ	[2] [3]							
		V _{CC} = 3.3 V		-	0.05	1	-	-	-	mV
		V _{CC} = 5.0 V		-	0.03	1	-	0.03	1	mV
		I _{SW} ≤ 10 mA; R _S ≤ 3.9 kΩ								
		V _{CC} = 3.3 V		-	0.55	5	-	-	-	mV
		V _{CC} = 5.0 V		-	0.27	5	-	0.27	5	mV
		I _{SW} ≤ 1 mA; R _S ≤ 20 kΩ								
		V _{CC} = 3.3 V		-	0.04	2	-	-	-	mV
		V _{CC} = 5.0 V		-	0.03	2	-	0.03	2	mV
		I _{SW} ≤ 10 mA; R _S ≤ 20 kΩ								
		V _{CC} = 3.3 V		-	0.56	20	-	-	-	mV
		V _{CC} = 5.0 V		-	0.48	20	-	0.48	20	mV

Typical values are measured at T_{amb} = 25 °C. [1]

[2] [3] ΔV_0 here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.

 I_{SW} = total current injected into all disabled channels.

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V);

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Мах	Min	Мах	Min	Max	
74HC48	51	·								
V _{IH}	HIGH-level	control inputs								
	input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 3.3 V	2.3	-	-	2.3	-	2.3	-	V
		V _{CC} = 4.5 V	3.15	-	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	-	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	control inputs								
	input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 3.3 V	-	-	1.0	-	1.0	-	1.0	V
		V _{CC} = 4.5 V	-	-	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	-	1.8	-	1.8	V

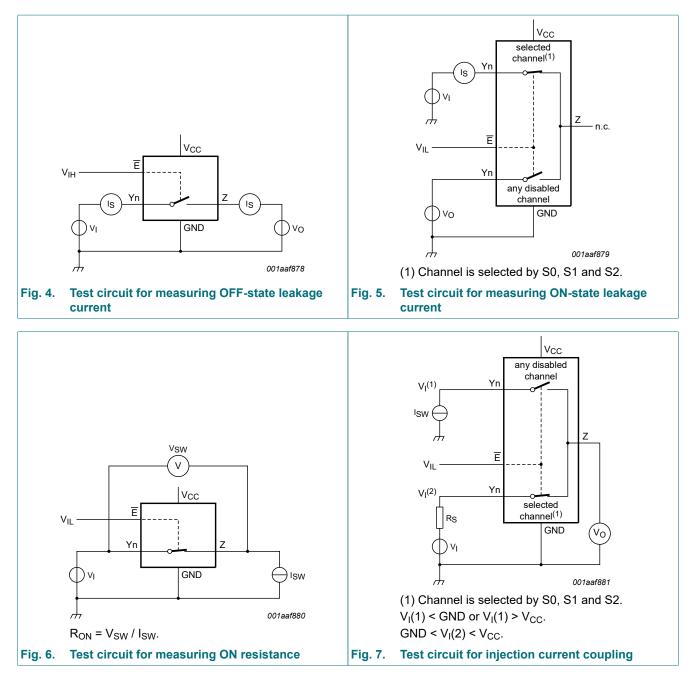
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Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	-
lı	input leakage current	control inputs; V _I = GND or V _{CC} ; V _{CC} = 6.0 V	-	-	±0.1	-	±0.1	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	$\label{eq:constraint} \begin{split} \overline{E} &= V_{IH}; V_{I} = GND \text{ or } V_{CC}; \\ V_{O} &= V_{CC} \text{ or } GND; V_{CC} = 6.0 \; V; \\ see \; \overline{Fig. 4} \end{split}$								
		per channel	-	-	±0.1	-	±0.5	-	±1.0	μA
		all channels	-	-	±0.2	-	±2.0	-	±4.0	μA
I _{S(ON)}	ON-state leakage current	$ E = V_{IL}; V_I = GND \text{ or } V_{CC}; $	-	-	±0.1	-	±0.5	-	±1.0	μA
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	5.0	-	20.0	μA
CI	input capacitance	S0, S1, S2 and E	-	2	10	-	10	-	10	pF
C _{sw}	switch	Z; OFF-state	-	15	40	-	40	-	40	pF
	capacitance	Yn; OFF-state	-	3	15	-	15	-	15	pF
74HCT4	HCT4851					1	1	1		
V _{IH}	HIGH-level input voltage	control inputs; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	control inputs;		-	0.8	-	0.8	-	0.8	V
I _I	input leakage current	control inputs; V _I = GND or V _{CC} ; V _{CC} = 5.5 V	-	-	±0.1	-	±0.1	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	$\overline{E} = V_{IH}; V_I = GND \text{ or } V_{CC};$ $V_O = V_{CC} \text{ or } GND; V_{CC} = 5.5 \text{ V};$ see Fig. 4								
		per channel	-	-	±0.1	-	±0.5	-	±1.0	μA
		all channels	-	-	±0.2	-	±2.0	-	±4.0	μA
I _{S(ON)}	ON-state leakage current	$E = V_{IL}; V_I = GND \text{ or } V_{CC};$ $V_O = V_{CC} \text{ or } GND; V_{CC} = 5.5 \text{ V};$ see Fig. 5	-	-	±0.1	-	±0.5	-	±1.0	μA
I _{CC}	supply current $V_I = GND \text{ or } V_{CC}; V_{CC} = 5.5 V$		-	-	2.0	-	5.0	-	20.0	μA
ΔI _{CC}	additional supply current	itional control inputs; $V_1 = V_{CC} - 2.1 V$; ply other inputs at V_{CC} or GND;		-	300	-	370	-	370	μA
CI	input capacitance	S0, S1, S2 and Ē	-	2	10	-	10	-	10	pF
C _{sw}	switch	Z; OFF-state	-	15	40	-	40	-	40	pF
	capacitance	Yn; OFF-state	-	3	15	-	15	-	15	pF

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11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 12.

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Мах	Min	Max	Min	Max	
74HC48	51	·								
t _{pd}	propagation	Z to Yn, Yn to Z; see Fig. 8 [1]								
	delay	V _{CC} = 2.0 V	-	10.0	25	-	29	-	32	ns
		V _{CC} = 3.0 V	-	6.0	15.5	-	17.5	-	19.5	ns
		V _{CC} = 3.3 V	-	5.0	14.5	-	16.5	-	18.5	ns
		V _{CC} = 4.5 V	-	4.0	11.5	-	12.5	-	13.5	ns
		V _{CC} = 6.0 V	-	3.0	10	-	11	-	12	ns
		Sn to Z, Sn to Yn; see Fig. 9 [1]								
		V _{CC} = 2.0 V	-	18.0	32	-	35	-	40	ns
		V _{CC} = 3.0 V	-	9.5	17.5	-	20	-	23	ns
		V _{CC} = 3.3 V	-	8.5	16.5	-	19	-	22	ns
		V _{CC} = 4.5 V	-	6.5	13	-	15	-	17	ns
		V _{CC} = 6.0 V	-	5.0	12.5	-	14.5	-	16.5	ns
t _{en}	enable time	\overline{E} to Z, \overline{E} to Yn; see <u>Fig. 10</u> [2]								
		V _{CC} = 2.0 V	-	-	95	-	105	-	115	ns
		V _{CC} = 3.0 V	-	-	90	-	100	-	110	ns
		V _{CC} = 3.3 V	-	-	85	-	95	-	105	ns
		V _{CC} = 4.5 V	-	-	80	-	90	-	100	ns
		V _{CC} = 6.0 V	-	-	78	-	80	-	80	ns
t _{dis}	disable time	\overline{E} to Z, \overline{E} to Yn; see <u>Fig. 10</u> [3]								
		V _{CC} = 2.0 V	-	-	99	-	105	-	115	ns
		V _{CC} = 3.0 V	-	-	90	-	100	-	110	ns
		V _{CC} = 3.3 V	-	-	85	-	95	-	105	ns
		V _{CC} = 4.5 V	-	-	80	-	90	-	100	ns
		V _{CC} = 6.0 V	-	-	78	-	80	-	80	ns
C _{PD}	power	per channel; see <u>Fig. 11</u> [4]								
	dissipation	V _{CC} = 3.3 V	-	28	-	-	-	-	-	pF
	capacitance	V _{CC} = 5.0 V	-	33	-	-	-	-	-	pF

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Symbol	Parameter	Conditions			25 °C			°C to 5 °C		°C to 5 °C	Unit
				Min	Тур	Мах	Min	Мах	Min	Max	
74HCT4	851										
t _{pd}	propagation	Z to Yn, Yn to Z; see Fig. 8	[1]								
	delay	V _{CC} = 4.5 V		1.6	3.7	11.5	1.1	12.5	1.1	13.5	ns
		Sn to Z, Sn to Yn; see Fig. 9	[1]								
		V _{CC} = 4.5 V		3.2	8.0	13	2.3	15	2.3	17	ns
t _{en}	enable time	Ē to Z, Ē to Yn; see Fig. 10	[2]								
		V _{CC} = 4.5 V		4.2	8.6	25	3.0	30	3.0	35	ns
t _{dis}	disable time	Ē to Z, Ē to Yn; see Fig. 10	[3]								
		V _{CC} = 4.5 V		28.5	64.7	80	28.2	90	28	100	ns
C _{PD}	power	per channel; see Fig. 11	[4]								
	dissipation capacitance	V _{CC} = 5.0 V		-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} + \sum \{(C_{L} + C_{sw}) \times V_{CC}^{2} \times f_{o}\} \text{ where:}$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

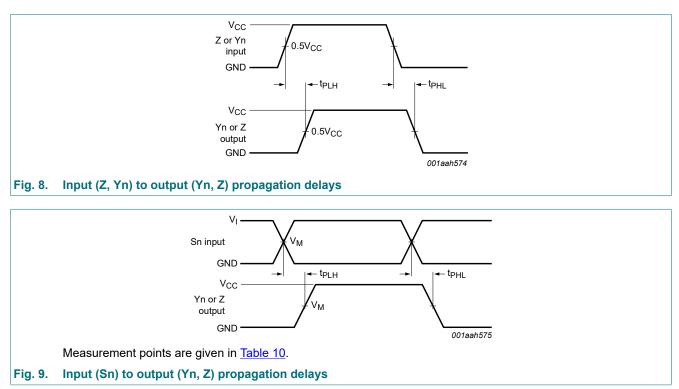
 $\sum \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\} = sum of outputs;$

 C_L = output load capacitance in pF;

 C_{sw} = switch capacitance in pF;

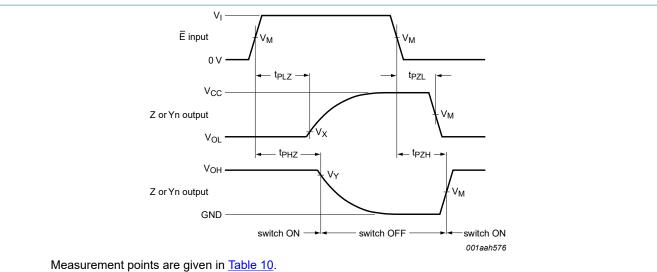
 V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit



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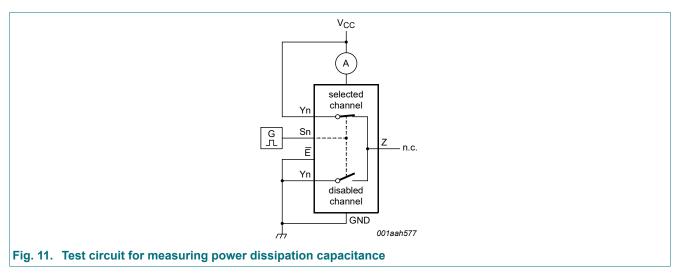


Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. Enable and disable times

Table 10. Measurement points

Туре	Input		Output						
	V _M	VI	V _M	V _X	V _Y				
74HC4851	$0.5 \times V_{CC}$	V _{CC}	0.5 × V _{CC}	V _{OL} + 0.1 × (V _{CC} - V _{OL})	0.9 × V _{OH}				
74HCT4851	1.3 V	3.0 V	$0.5 \times V_{CC}$	V_{OL} + 0.1 × (V_{CC} - V_{OL})	0.9 × V _{OH}				



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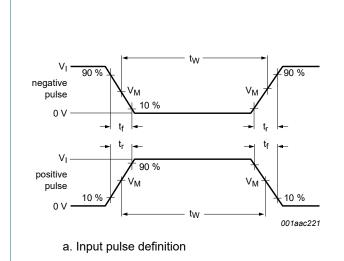
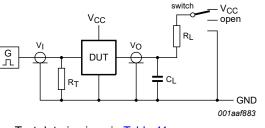


Fig. 12. Test circuit for measuring switching times



Test data is given in Table 11.

Definitions for test circuit:

R_L = load resistance;

 C_L = load capacitance including jig and probe capacitance;

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

b. Test circuit

Test	Input			Output		S1 position
	Control E, Sn	Switch Yn (Z)	t _r , t _f	Switch Z (Y	′n)	
	V _I [1]	VI	_	CL	RL	
t _{PHL,} t _{PLH}	V _{CC}	V _{CC}	6 ns	50 pF	-	open
t _{PHZ} , t _{PZH}	V _{CC}	V _{CC}	6 ns	50 pF	10 kΩ	GND
t _{PLZ} , t _{PZL}	V _{CC}	V _{CC}	6 ns	50 pF	10 kΩ	V _{CC}
C _{PD}	V _{CC}	V _{CC}	6 ns	0 pF	-	open

[1] For 74HCT4851: input voltage $V_1 = 3.0 V$.

74HC_HCT4851

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12. Package outline

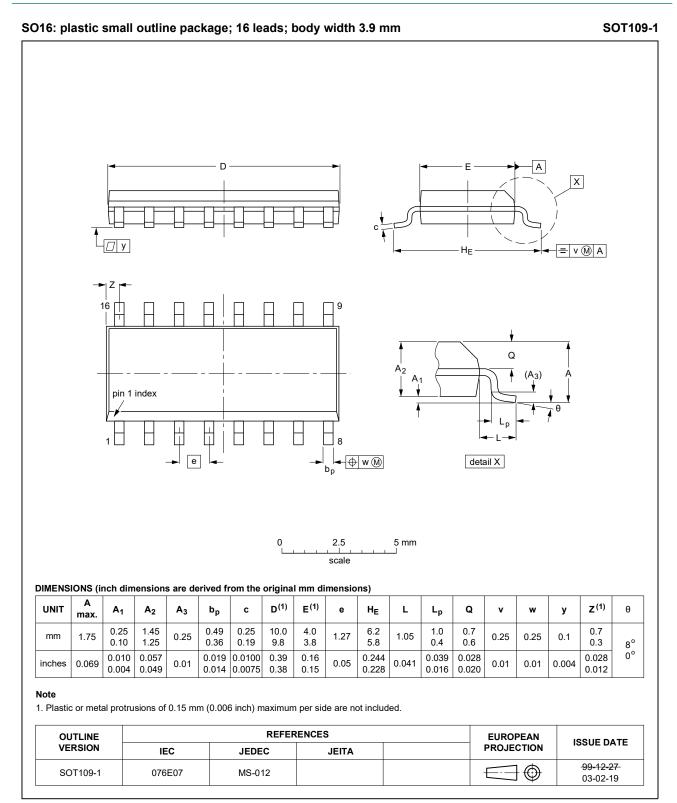


Fig. 13. Package outline SOT109-1 (SO16)

74HC_HCT4851

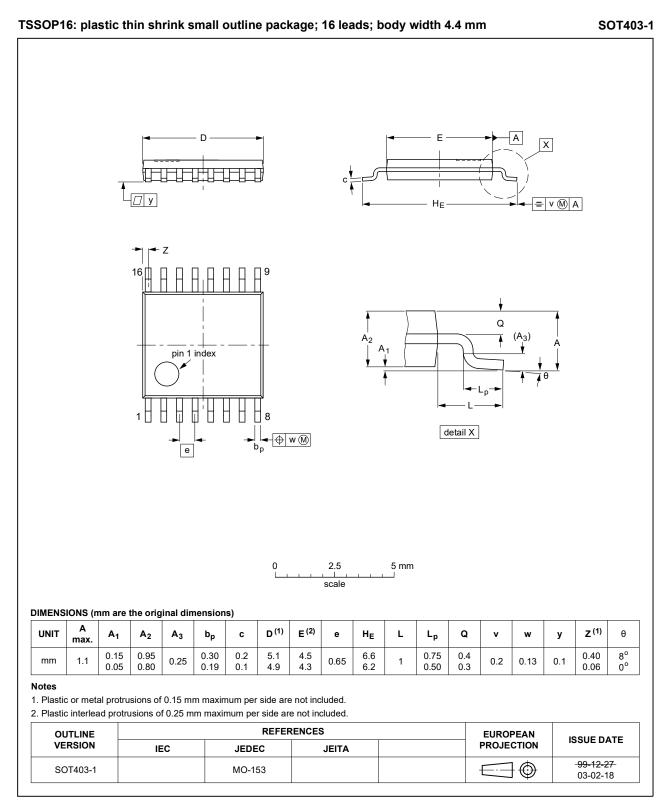
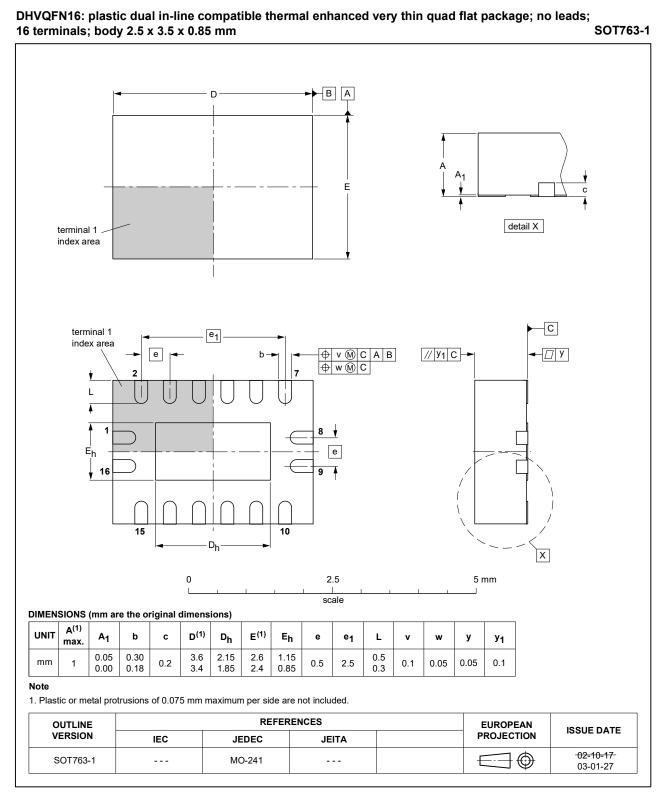


Fig. 14. Package outline SOT403-1 (TSSOP16)

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Product data sheet

13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4851 v.4	20230515	Product data sheet	-	74HC_HCT4851 v.3
Modifications:	<u>Section 8</u> : De	erating values for P _{tot} total p	power dissipation	updated.
74HC_HCT4851 v.3	20180824	Product data sheet	-	74HC_HCT4851 v.2
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT4851 v.2	20080902	Product data sheet	-	74HC4851 v.1
Modifications:	• 74HCT4851	device added.		
74HC4851 v.1	20070309	Product data sheet	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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