

# TC74AC74P

## 1. Functional Description

- Dual D-Type Flip-Flop with Preset and Clear

## 2. General

The TC74AC74P is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

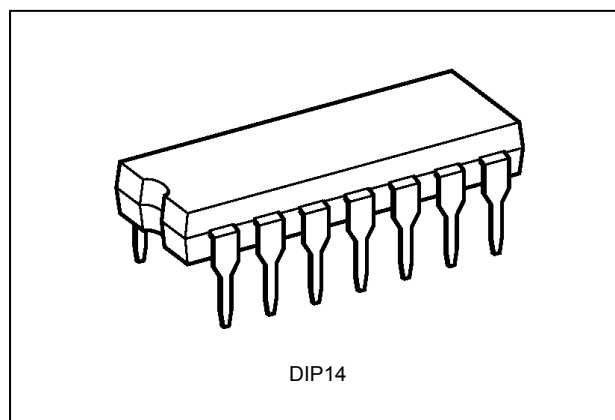
$\overline{\text{CLR}}$  and  $\overline{\text{PR}}$  are independent of the CK and are accomplished by setting the appropriate input to an "L" level.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) High speed:  $f_{\text{MAX}} = 200 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5.0 \text{ V}$
- (2) Low power dissipation:  $I_{\text{CC}} = 4.0 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- (3) High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- (4) Output current:  $|I_{\text{OH}}|/I_{\text{OL}} = 24 \text{ mA}$  (min) ( $V_{\text{CC}} = 4.5 \text{ V}$ )
- (5) Balanced propagation delays:  $t_{\text{PLH}} \approx t_{\text{PHL}}$
- (6) Wide operating voltage range:  $V_{\text{CC(opr)}} = 2.0 \text{ V}$  to  $5.5 \text{ V}$
- (7) Pin and function compatible with 74F74.

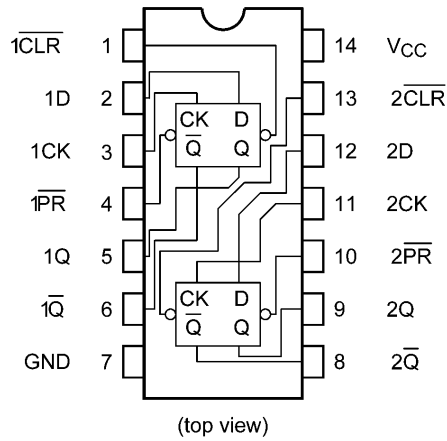
## 4. Packaging



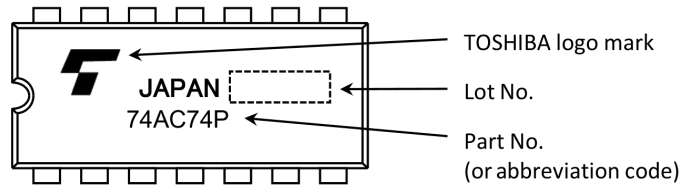
Start of commercial production

1986-05

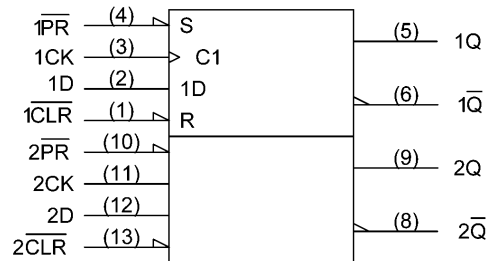
### 5. Pin Assignment



### 6. Marking



### 7. IEC Logic Symbol

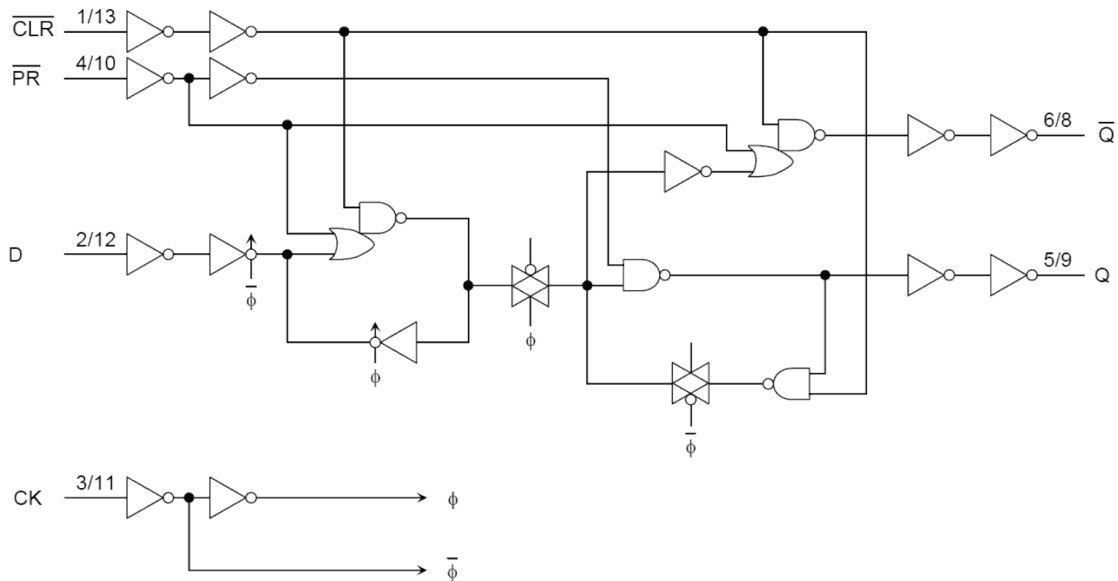


### 8. Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q <sub>n</sub>	Q̄ <sub>n</sub>	No Change

X: Don't care

### 9. System Diagram



### 10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
Output diode current	$I_{OK}$		$\pm 50$	mA
Output current	$I_{OUT}$		$\pm 50$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 100$	mA
Power dissipation	$P_D$	(Note 1)	500	mW
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  shall be applied until 300 mW.

### 11. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage	$V_{IN}$		0 to $V_{CC}$	V
Output voltage	$V_{OUT}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 85	$^{\circ}C$
Input rise and fall times	$dt/dv$	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5.0 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

### 12. Electrical Characteristics

#### 12.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			3.0	2.10	—	—		
			5.5	3.85	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			3.0	—	—	0.90		
			5.5	—	—	1.65		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	V	
				3.0	2.9	3.0		—
				4.5	4.4	4.5		
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—		—
		$I_{OH} = -24\text{ mA}$	4.5	3.94	—	—		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	V	
				3.0	—	0.0		0.1
				4.5	—	0.0		
			$I_{OL} = 12\text{ mA}$	3.0	—	—		0.36
				$I_{OL} = 24\text{ mA}$	4.5	—		—
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.1$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	$\mu\text{A}$	

#### 12.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Note	$V_{CC}$ (V)	Min	Max	Unit		
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V		
				3.0	2.10	—			
				5.5	3.85	—			
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V		
				3.0	—	0.90			
				5.5	—	1.65			
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$		2.0	1.9	V		
					3.0	2.9		—	
					4.5	4.4			
			$I_{OH} = -4\text{ mA}$		3.0	2.48		—	
			$I_{OH} = -24\text{ mA}$		4.5	3.80		—	
		$I_{OH} = -75\text{ mA}$ (Note 1)	5.5	3.85	—				
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$		2.0	—	V		
					3.0	—		0.1	
					4.5	—			0.1
			$I_{OL} = 12\text{ mA}$		3.0	—		0.44	
					$I_{OL} = 24\text{ mA}$	4.5		—	0.44
					$I_{OL} = 75\text{ mA}$ (Note 1)	5.5		—	1.65
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		5.5	—	$\pm 1.0$	$\mu\text{A}$		
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	40.0	$\mu\text{A}$		

Note 1: This spec indicates the capability of driving  $50\text{ }\Omega$  transmission lines.

One output should be tested within a 10 ms maximum duration.

### 12.3. Timing Requirements (Unless otherwise specified, $T_a = 25^\circ\text{C}$ , Input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	7.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum pulse width (CLR, PR)	$t_{w(L)}$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	7.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time	$t_s$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	3.5	
Minimum hold time	$t_h$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	1.0	ns
			$5.0 \pm 0.5$	1.0	
Minimum removal time (CLR, PR)	$t_{rem}$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	4.0	ns
			$5.0 \pm 0.5$	2.0	

### 12.4. Timing Requirements (Unless otherwise specified, $T_a = -40$ to $85^\circ\text{C}$ , Input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	7.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum pulse width (CLR, PR)	$t_{w(L)}$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	7.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time	$t_s$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	3.5	
Minimum hold time	$t_h$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	1.0	ns
			$5.0 \pm 0.5$	1.0	
Minimum removal time (CLR, PR)	$t_{rem}$	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	$3.3 \pm 0.3$	4.0	ns
			$5.0 \pm 0.5$	2.0	

### 12.5. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ , Input: $t_r = t_f = 3\text{ ns}$ )

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit
Propagation delay time (CK-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$		$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	$3.3 \pm 0.3$	—	8.2	13.9	ns
				$5.0 \pm 0.5$	—	6.1	8.7	
Propagation delay time (CLR, PR-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$		$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	$3.3 \pm 0.3$	—	8.0	13.1	ns
				$5.0 \pm 0.5$	—	5.7	8.2	
Maximum clock frequency	$f_{MAX}$		$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	$3.3 \pm 0.3$	60	120	—	MHz
				$5.0 \pm 0.5$	100	160	—	
Input capacitance	$C_{IN}$		—	—	5	10	pF	
Power dissipation capacitance	$C_{PD}$	(Note 1)	—	—	77	—	pF	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

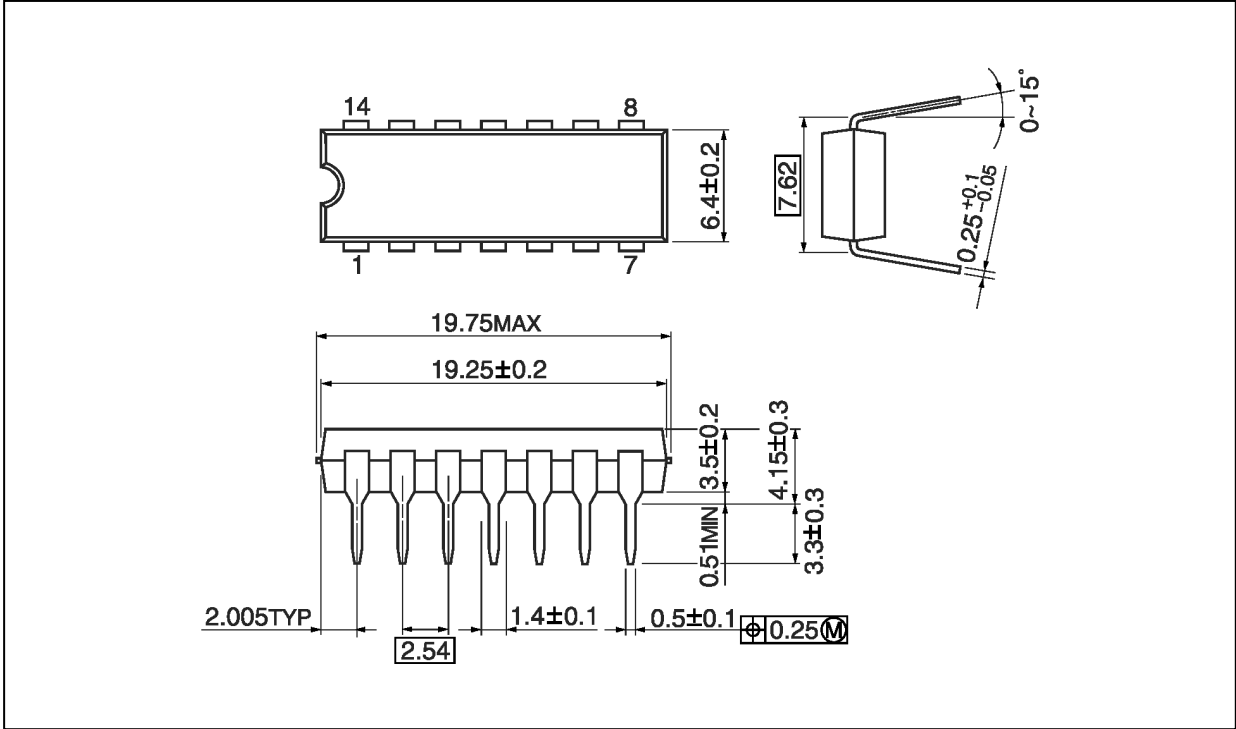
### 12.6. AC Characteristics

(Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit
Propagation delay time (CK-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	$3.3 \pm 0.3$	1.0	16.0	ns
			$5.0 \pm 0.5$	1.0	10.0	
Propagation delay time (CLR, PR-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	$3.3 \pm 0.3$	1.0	15.0	ns
			$5.0 \pm 0.5$	1.0	9.4	
Maximum clock frequency	$f_{MAX}$	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	$3.3 \pm 0.3$	60	—	MHz
			$5.0 \pm 0.5$	100	—	
Input capacitance	$C_{IN}$	—	—	—	10	pF

Package Dimensions

Unit: mm



Weight: 0.96 g (typ.)

Package Name(s)
Nickname: DIP14

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