



## SY100EP14AU

2.5V/3.3V 1:5 LVPECL/LVECL/HSTL 2GHz  
Clock Driver With 2:1 Differential Input MUX

### General Description

The SY100EP14AU is a high-speed, 2GHz differential PECL/ECL 1:5 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 25ps over temperature and supply voltage. The wide supply voltage operation allows this fanout buffer to operate in 2.5V and 3.3V systems. A  $V_{BB}$  reference is included for single-supply or AC-coupled PECL/ECL input applications, thus eliminating resistor networks. When interfacing to a single-ended or AC-coupled PECL/ECL input signal, connect the  $V_{BB}$  pin to the unused /CLK pin, and bypass the pin to  $V_{CC}$  through a 0.01 $\mu$ F capacitor.

The SY100EP14AU features a 2:1 input MUX, making it an ideal solution for redundant clock switchover applications. If only one input pair is used, the other pair may be left floating. In addition, this device includes a synchronous enable pin that forces the outputs into a fixed logic state. Enable or disable state is initiated only after the outputs are in a LOW state, thus eliminating the possibility of a "runt" clock pulse.

The SY100EP14AU I/O are fully differential and 100K ECL compatible. Differential 10K ECL logic can interface directly into the SY100EP14AU inputs.

The SY100EP14AU is part of Micrel's high-speed clock synchronization family. For applications that require a different I/O combination, consult the Micrel website at [www.micrel.com](http://www.micrel.com), and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

### Features

- Guaranteed AC parameters over temp/voltage:
  - >2GHz  $f_{MAX}$
  - <25ps within-device skew
  - <250ps tr/ff time
  - <550ps prop delay
- 2:1 Differential MUX input
- Unique, patented MUX input isolation design minimizes adjacent channel crosstalk
- Flexible supply voltage: 2.5V/3.3V
- Wide operating temperature range: -40°C to +85°C
- $V_{BB}$  reference for single-ended or AC-coupled PECL inputs
- 100K ECL compatible outputs
- Inputs accept PECL/LVPECL/ECL/HSTL logic
- 75K $\Omega$  internal input pull-down resistors
- Available in a 20-Pin TSSOP package

### Applications

- SONET Clock and Data distribution
- Fibre Channel Clock and Data distribution
- Ethernet Clock and Data distribution

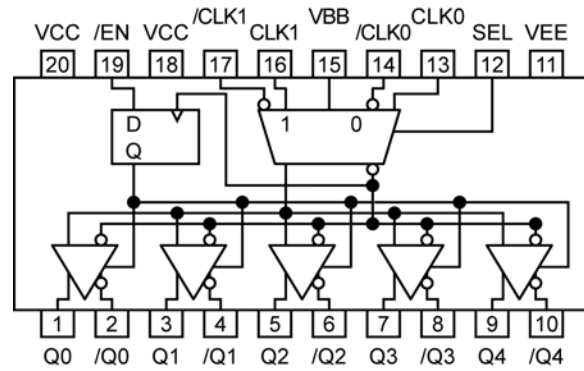
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EP14AUKG	K4-20-1	Industrial	XEP14AU with Pb-Free bar line indicator	NiPdAu Pb-free
SY100EP14AUKGTR <sup>(2)</sup>	K4-20-1	Industrial	XEP14AU with Pb-Free bar line indicator	NiPdAu Pb-free

**Note:**

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.
2. Tape and Reel.

## Pin Configuration



20-Pin TSSOP

## Pin Description

Pin Number	Pin Name	Pin Function
13, 14 16, 17	CLK0, /CLK0 CLK1, /CLK1	LVPECL, LVECL, HSTL Clock or Data Inputs. Internal 75k $\Omega$ pull-down resistors on CLK0, CLK1, and internal 75k $\Omega$ pull-up and 75k $\Omega$ pull-down resistors on /CLK0, /CLK1. For single-ended applications, connect signal into CLK0 and/or CLK1 inputs. /CLK0, /CLK1 default condition is $V_{CC}/2$ when left floating. CLK0, CLK1 default condition is LOW when left floating.
1, 2, 3, 4 5, 6, 7, 8 9, 10	Q0, /Q0, Q1, /Q1 Q2, /Q2, Q3, /Q3 Q4, /Q4	LVPECL/LVECL Differential Outputs: Terminate with 50 $\Omega$ to $V_{CC}-2V$ . For single-ended applications, /Q0 to /Q4 terminate the unused output with 50 $\Omega$ to $V_{CC}-2V$ .
19	/EN	LVPECL/LVECL compatible synchronous enable: When /EN goes HIGH, the Q <sub>OUT</sub> will go LOW and /Q <sub>OUT</sub> will go HIGH on the next LOW input clock transition. Includes a 75k $\Omega$ pull-down. Default state is LOW when left floating. The internal latch is clocked on the falling edge of the input clock (CLK0, CLK1).
12	SEL	LVPECL/LVECL compatible 2:1 MUX input signal select: When SEL is LOW, CLK0 input pair is selected. When SEL is HIGH, CLK1 input pair is selected. Includes a 75k $\Omega$ pull-down. Default state is LOW and CLK0 is selected.
15	VBB	Output Reference Voltage: Equal to $V_{CC}-1.4V$ (approx.), and used for single-ended input signals or AC-coupled applications. For single-ended LVPECL and LVECL applications, bypass with a 0.01 $\mu F$ to $V_{CC}$ . Max. sink/source current is 0.5mA.
18, 20	VCC	Positive Power Supply: Bypass with 0.1 $\mu F$ //0.01 $\mu F$ low ESR capacitors.
11	VEE	Negative Power Supply: LVPECL applications, connect to GND.

## Truth Table

CLK0	CLK1	CLK_SEL	/EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L

**Note:**

1. On next negative transition of CLK0 or CLK1.

## Function Table

CLK_SEL	Active Input
0	CLK0, /CLK0
1	CLK1, /CLK1

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{CC} - V_{EE}$ )	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	
$V_{CC} = 0V$ , $V_{IN}$ not more negative than $V_{EE}$	-4.0V to 0V
$V_{EE} = 0V$ , $V_{IN}$ not more positive than $V_{CC}$	0V to +4.0V
Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 20sec.)	+260°C
$I_{BB}$ ( $V_{BB}$ Sink/Source Current) <sup>(3)</sup>	± 0.5mA
Storage Temperature ( $T_s$ )	-65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{IN}$ )	+2.375V to +3.60V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Thermal Resistance ( $\theta_{JA}$ )	
Still Air, single-layer PCB	115°C/W
Still Air, multi-layer PCB	75°C/W
500lfpm, multi-layer PCB	65°C/W
Package Thermal Resistance ( $\theta_{JC}$ )	21°C/W

**DC Electrical Characteristics<sup>(4)</sup>**

-40°C ≤  $T_A$  ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage (LVPECL)		2.37	3.3	3.6	V
$V_{EE}$	Power Supply Voltage (LVECL)	$V_{CC} = 0V$	-3.6	-3.3	-2.37	V
$I_{CC}$	Power Supply Current			45	65	mA
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{IH}$	-	-	150	μA
$I_{IL}$	Input LOW Current D	$V_{IN} = V_{IL}$	0.5	-	-	μA
$I_{IL}$	Input LOW Current /D	$V_{IN} = V_{IL}$	-150	-	-	μA
$C_{IN}$	Input Capacitance (TSSOP)	$T_A = +25°C$	-	0.75	-	pF

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect devices reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for inputs of same package only.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium is established.

**(100KEP) LVPECL DC Electrical Characteristics<sup>(1)</sup>**

$V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ;  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IL}$	Input LOW Voltage <sup>(2)</sup> (Single-ended)		555	–	875	mV
$V_{IH}$	Input HIGH Voltage <sup>(2)</sup> (Single-ended)		1335	–	1620	mV
$V_{OL}$	Output LOW Voltage	$50\Omega$ to $V_{CC} - 2V$	555	700	900	mV
$V_{OH}$	Output HIGH Voltage	$50\Omega$ to $V_{CC} - 2V$	1355	1480	1605	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range <sup>(3)</sup>		1.2	–	$V_{CC}$	V

**(100KEP) LVPECL DC Electrical Characteristics<sup>(1)</sup>**

$V_{CC} = 3.3V \pm 10\%$ ,  $V_{EE} = 0V$ ;  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IL}$	Input LOW Voltage <sup>(2)</sup> (Single-ended)		1355	–	1675	mV
$V_{IH}$	Input HIGH Voltage <sup>(2)</sup> (Single-ended)		2135	–	2420	mV
$V_{OL}$	Output LOW Voltage	$50\Omega$ to $V_{CC} - 2V$	1355	1500	1700	mV
$V_{OH}$	Output HIGH Voltage	$50\Omega$ to $V_{CC} - 2V$	2155	2280	2405	mV
$V_{BB}$	Reference Voltage <sup>(2)</sup>	$V_{CC} = 3.3V$	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range <sup>(3)</sup>		1.2	–	$V_{CC}$	V

**(100KEP) LVECL DC Electrical Characteristics<sup>(1)</sup>**

$V_{EE} = -2.37V$  to  $-3.6V$ ,  $V_{CC} = 0V$ ;  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IL}$	Input LOW Voltage (Single-ended)		-1945	–	-1625	mV
$V_{IH}$	Input HIGH Voltage (Single-ended)		-1165	–	-880	mV
$V_{OL}$	Output LOW Voltage	$50\Omega$ to $V_{CC} - 2V$	-1945	-1800	-1600	mV
$V_{OH}$	Output HIGH Voltage	$50\Omega$ to $V_{CC} - 2V$	-1145	-1020	-895	mV
$V_{BB}$	Output Reference Voltage <sup>(2)</sup>		-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range <sup>(3)</sup>		$V_{EE} + 1.2$		0.0	V

**Notes:**

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with  $V_{CC}$ .
- Single-ended input operation is limited  $V_{EE} \leq -3.0V$  in ECL/LVECL mode.  $V_{BB}$  reference varies 1:1 with  $V_{CC}$ .
- $V_{IHCMR}(\min)$  varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}(\max)$  varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## HSTL Input DC Electrical Characteristics

$V_{CC} = 2.37V$  to  $3.6V$ ,  $V_{EE} = 0V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		1200	–	–	mV
$V_{IL}$	Input LOW Voltage		–	–	400	mV
$V_X$	Input Crossover Voltage		680	–	900	mV

## AC Electrical Characteristics

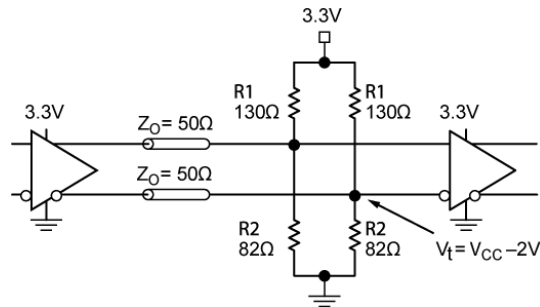
LVPECL:  $V_{CC} = 2.37V$  to  $2.625V$ ,  $V_{EE} = 0V$ ; LVECL:  $V_{EE} = -2.37V$  to  $-3.6V$ ,  $V_{CC} = 0V$ ;  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Frequency <sup>(1)</sup>		2	–	–	GHz
$t_{PD}$	Propagation Delay to Output (Differential input)		300	425	550	ps
$t_{PD}$	Propagation Delay to Output IN (Single-ended input)	$T_A = +25^{\circ}C$	–	400	–	ps
$t_{SKEW}^{(2)}$	Within-Device Skew (Diff.)		–	15	25	ps
	Part-to-Part Skew (Diff.)		–	100	175	ps
$t_s$	Set-Up Time <sup>(3)</sup> /EN to CLK		75	-85	–	ps
$t_H$	Hold Time <sup>(3)</sup> CLK to /EN		250	95	–	ps
$t_{JITTER}$	Random Jitter (rms) <sup>(4)</sup>		–	0.15	0.3	ps
$t_{JITTER}$	Crosstalk-Induced Jitter (rms) <sup>(5)</sup>		–	–	0.7	ps
$V_{PP}$	Minimum Input Swing		150	800	1200	mV
$t_R, t_F$	Rise and Fall Time	20% to 80%	80	160	250	ps

### Notes:

- $f_{MAX}$  is defined as the maximum toggle frequency. Measured with 750mV input signal, 50% duty cycle, all loading with 50Ω to  $V_{CC}-2V$ .
- Skew is measured between outputs under identical transitions.
- Set-up and hold times apply to synchronous applications that intend to enable/disable before then ext clock cycle. For asynchronous applications, set-up and hold time does not apply.
- Integration range: 12kHz to 20MHz at 1GHz fc.
- Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

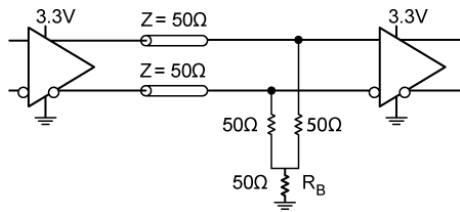
## Termination Recommendations



**Figure 1. Parallel Termination- Thevenin Equivalent**

**Note:**

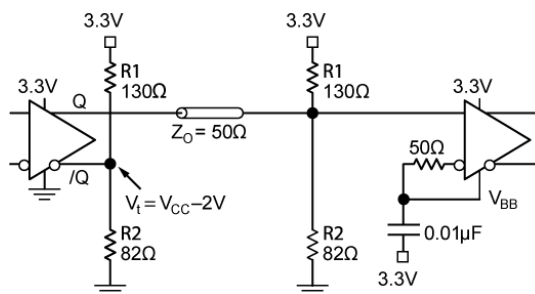
For 2.5V systems: R1= 250Ω, R2= 62.5Ω



**Figure 2. Three-Resistor "Y-Termination"**

**Notes:**

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3.  $R_B$  resistor sets the DC bias voltage, equal to  $V_T$ . For 3.3V systems  $R_B=50\Omega$ .

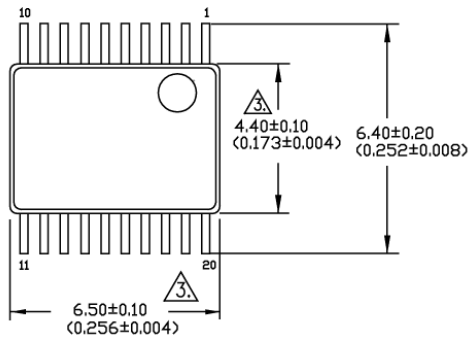


**Figure 3. Terminating Unused I/O**

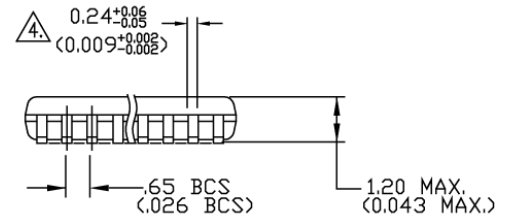
**Notes:**

1. Unused output (/Q) must be terminated to balance the output.
2. Micrel's differential I/O logic devices include a  $V_{BB}$  reference pin.
3. Connect unused input through 50Ω to  $V_{BB}$ . Bypass with a 0.01μF capacitor to  $V_{CC}$ , not GND.
4. For 2.5V systems: R1= 250Ω, R2= 62.5Ω.

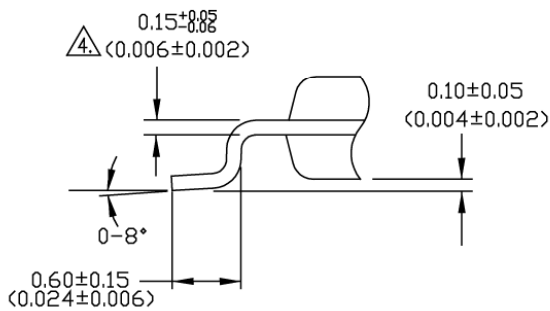
### Package Information



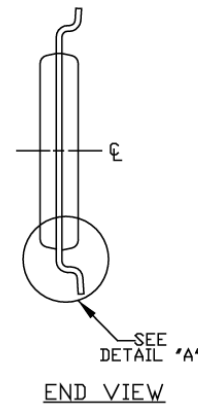
TOP VIEW



SIDE VIEW



DETAIL 'A'  
(VIEW ROTATED 90° C.W.)



END VIEW

**NOTES:**

1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254 [0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

**20-Pin TSSOP (K4-20-1)**

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