Integrated Circuit Systems, Inc.

ICS854054
4:1
DIFFERENTIAL-TO-LVDS CLOCK MULTIPLEXER

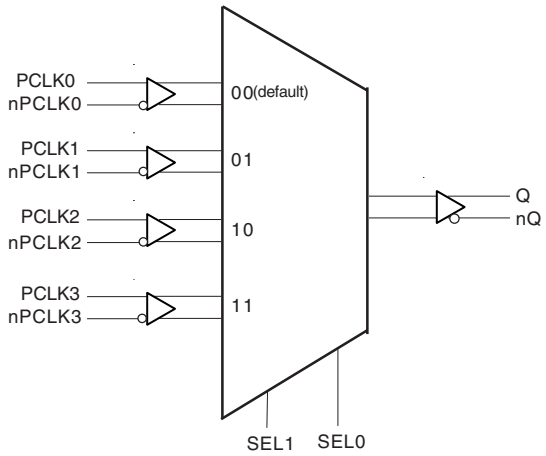
GENERAL DESCRIPTION

The ICS854054 is a 4:1 Differential-to-LVDS Clock Multiplexer which can operate up to 2.8GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS854054 has 4 selectable differential clock inputs. The PCLK, nPCLK input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects PCLK0, nPCLK0).

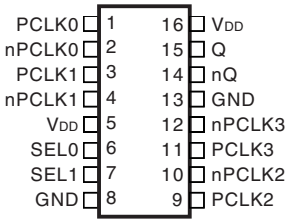
FEATURES

- High speed 4:1 differential multiplexer
- One differential LVDS output
- Four selectable differential clock inputs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2.8GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Part-to-part skew: 375ps (maximum)
- Propagation delay: 700ps (maximum)
- Supply voltage range: 3.135V to 3.465V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS854054
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential clock input.
2	nPCLK0	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK1	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
5, 16	V_{DD}	Power		Positive supply pins.
6, 7	SEL0, SEL1	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
8, 13	GND	Power		Power supply ground.
9	PCLK2	Input	Pulldown	Non-inverting differential clock input.
10	nPCLK2	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential clock input.
12	nPCLK3	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
14, 15	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Pulldown Resistor			75		kΩ
$R_{VDD/2}$	Pullup/Pulldown Resistors			50		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs	
SEL1	SEL0	Q	nQ
0	0	PCLK0	nPCLK0
0	1	PCLK1	nPCLK1
1	0	PCLK2	nPCLK2
1	1	PCLK3	nPCLK3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	5.5V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				90	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0:PCLK3	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLK0:nPCLK3	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0:PCLK3	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0:nPCLK3	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKx or nPCLKx is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	450	525	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

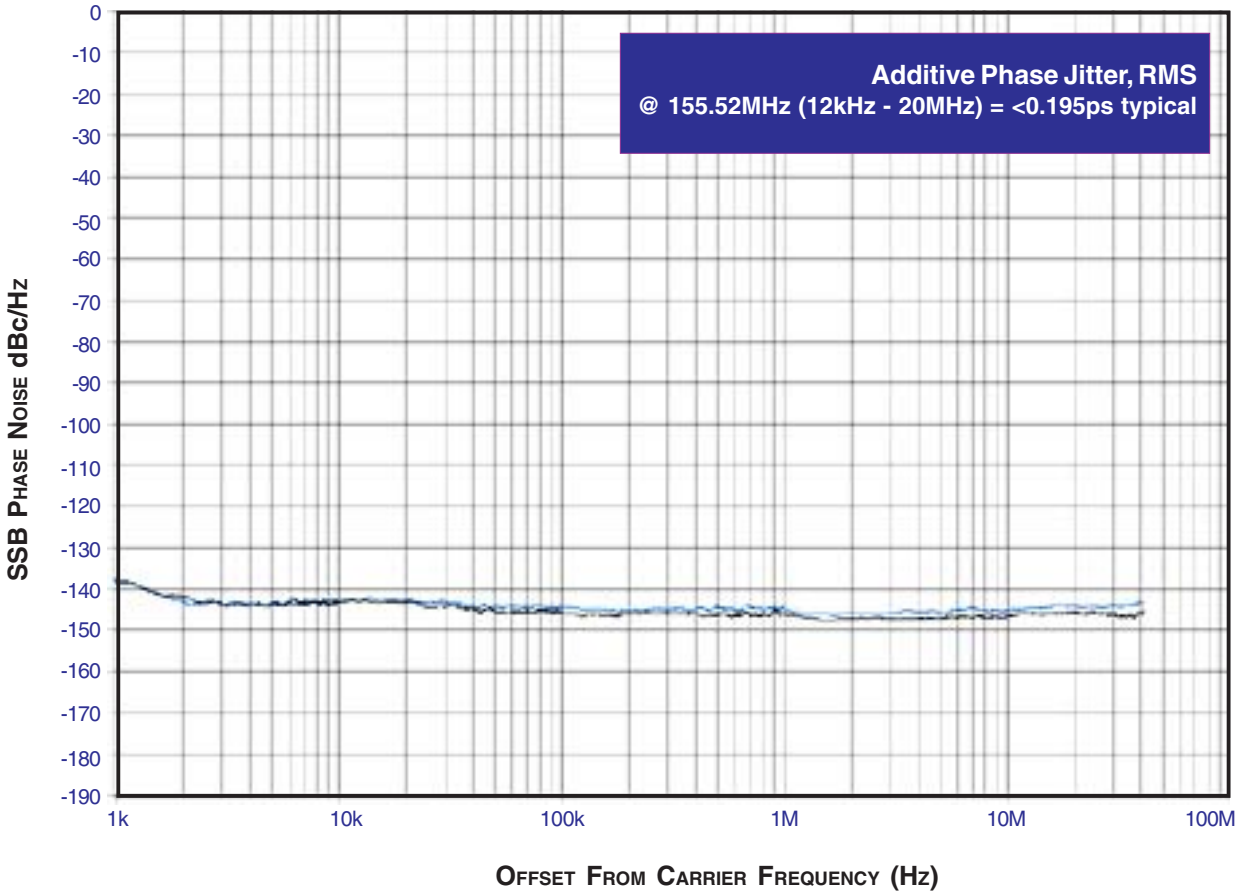
TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.135V TO 3.465V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				2.8	GHz
t_{PD}	Propagation Delay; NOTE 1		325		700	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52 MHz, (12kHz - 20MHz)		0.195		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				375	ps
*t*sk(i)	Input Skew				90	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		250	ps
$MUX_{ISOLATION}$	MUX Isolation	155.52MHz, Input Peak-to-Peak = 800mV		-50		dB

All parameters measured up to 1.5MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

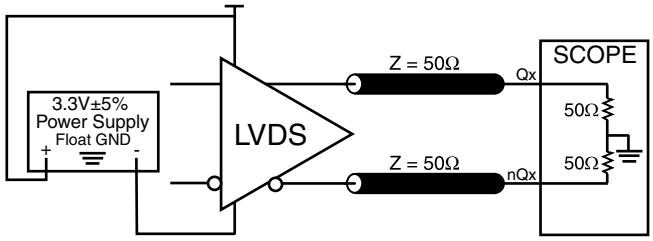
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

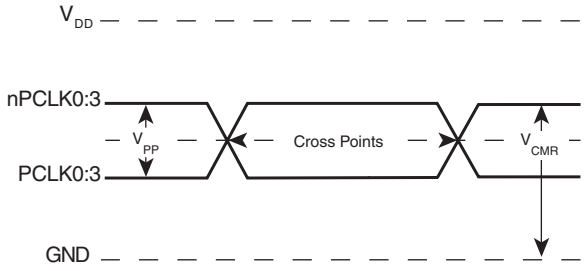


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

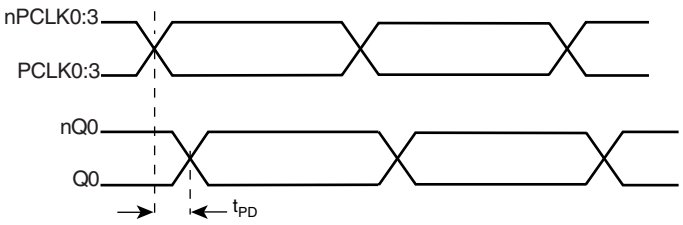
PARAMETER MEASUREMENT INFORMATION



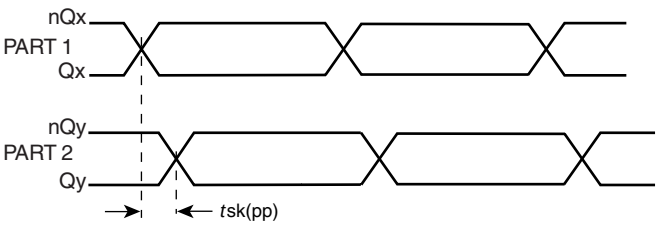
3.3V OUTPUT LOAD AC TEST CIRCUIT



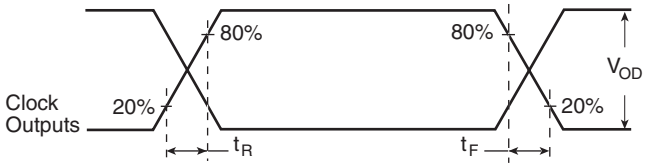
DIFFERENTIAL INPUT LEVEL



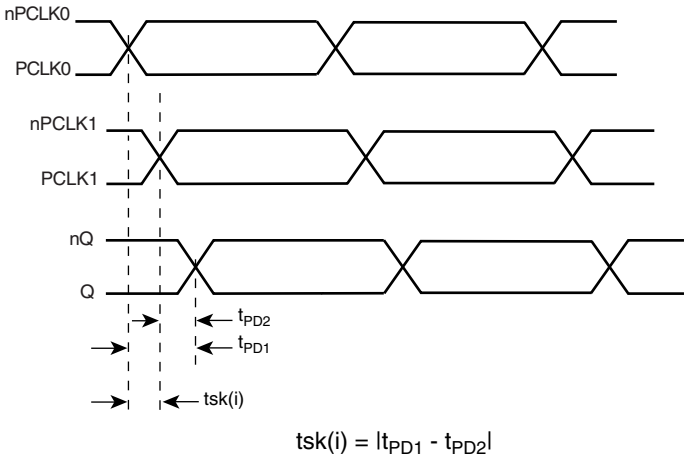
PROPAGATION DELAY



PART-TO-PART SKEW

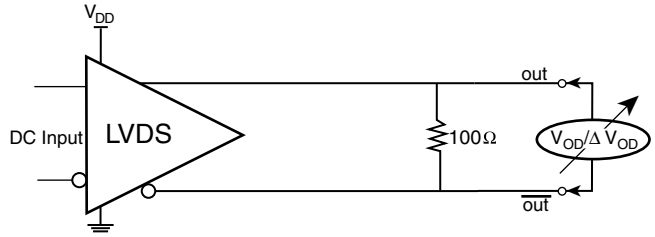


OUTPUT RISE/FALL TIME

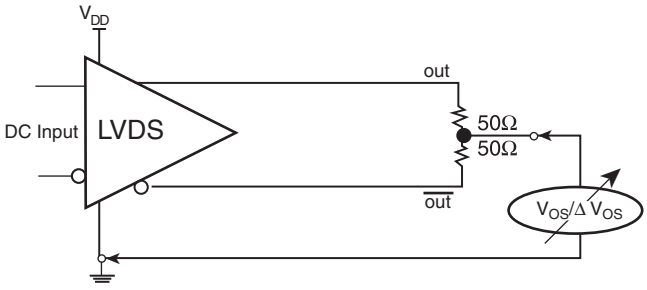


$$tsk(i) = |t_{PD1} - t_{PD2}|$$

INPUT SKEW



DIFFERENTIAL OUTPUT VOLTAGE



OFFSET VOLTAGE

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

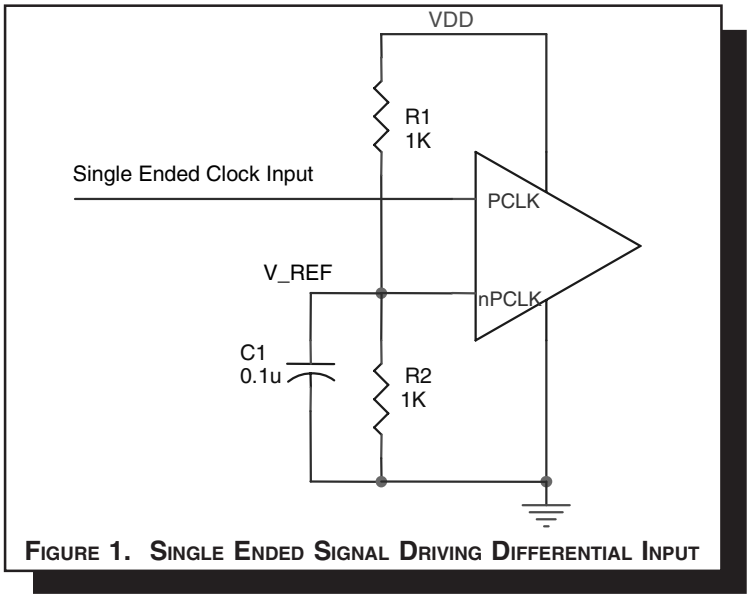


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from PCLK to ground.

SELECT PINS:

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resister can be used.

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

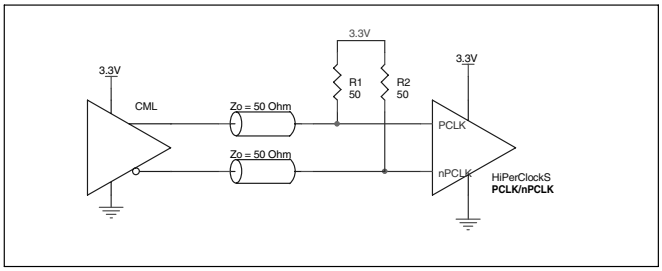


FIGURE 2A. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER

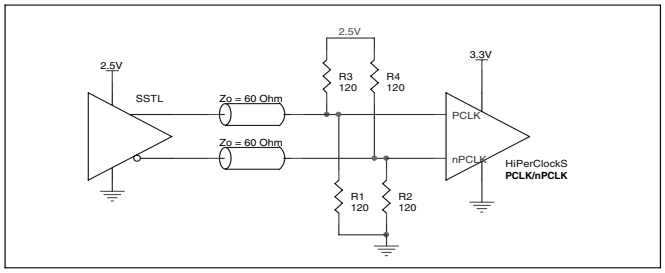


FIGURE 2B. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN SSTL IN DRIVER

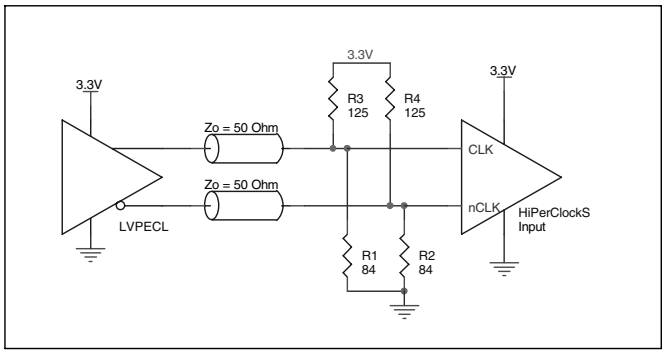


FIGURE 2C. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

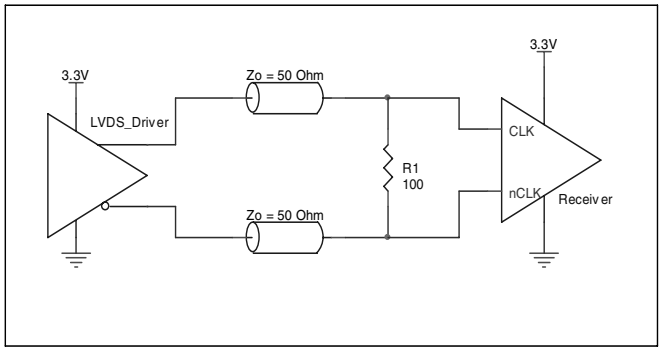


FIGURE 2D. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

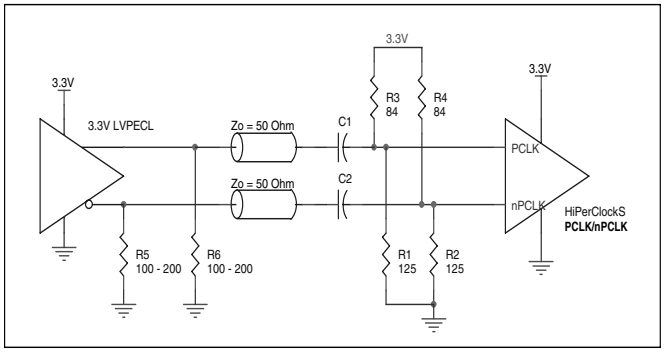


FIGURE 2E. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

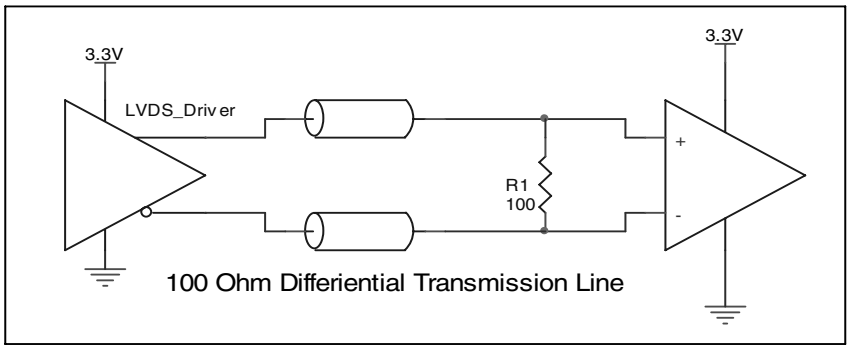


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS854054. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854054 is the sum of the core power.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 90mA = **311.85mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 81.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.312W * 81.8°C/W = 110.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS854054 is: 361

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

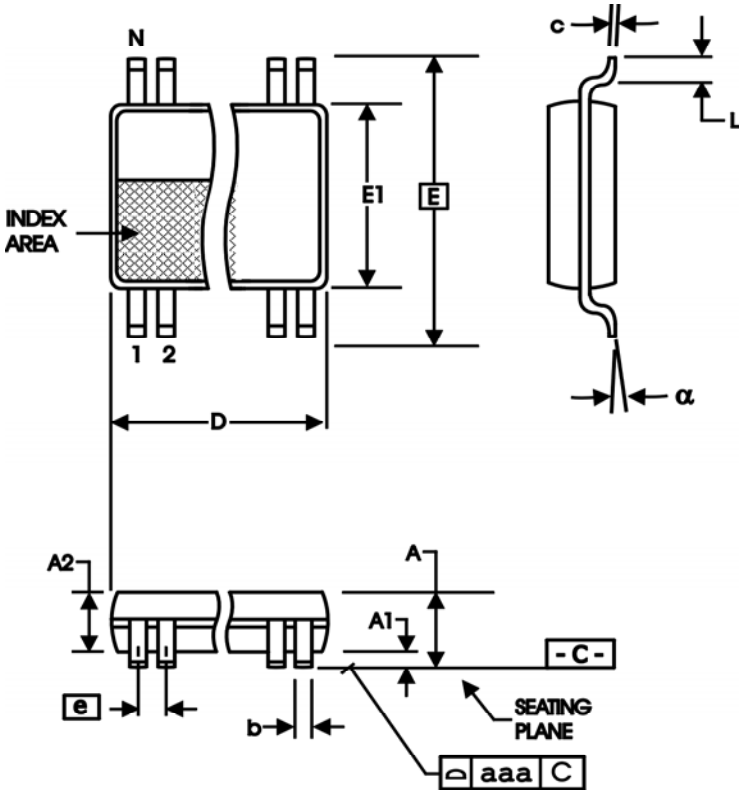


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854054AG	854054AG	16 Lead TSSOP	tube	-40°C to 85°C
ICS854054AGT	854054AG	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS854054AGLF	TBD	16 Lead TSSOP	tube	-40°C to 85°C
ICS854054AGLFT	TBD	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.